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S1D13A04 LCD/USB Companion Chip

Hardware Functional Specification

Document Number: X37A-A-001-07.6

NOTICE

Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13A04 LCD/USB Companion Chip. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 Overview Description

The S1D13A04 is an LCD/USB solution designed for seamless connection to a wide variety of microprocessors. The S1D13A04 integrates a USB slave controller and an LCD graphics controller with an embedded 160K byte SRAM display buffer. The LCD controller, based on the popular S1D13706, supports all standard panel types including the Sharp HR-TFT family of products. In addition to the S1D13706 feature set, the S1D13A04 includes a Hardware Acceleration Engine to greatly improve screen drawing functions. The USB controller provides revision 1.1 compliance for applications requiring a USB client.This high level of integration provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring USB client support, such as Mobile Communications devices and Palm-size PCs.

The S1D13A04 utilizes a guaranteed low-latency CPU architecture that provides support for microprocessors without READY/WAIT# handshaking signals. The 32-bit internal data path, write buffer and the Hardware Acceleration Engine provide high performance bandwidth into display memory allowing for fast display updates. ‘Direct’ support for the Sharp HR-TFT removes the requirement of an external Timing Control IC.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13A04 also provides support for “Picture-in-Picture Plus” (a variable size Overlay window).

The S1D13A04, with its integrated USB client, provides impressive support for Palm OS® handhelds. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

2 Features

2.1 Integrated Frame Buffer

- Embedded 160k byte SRAM display buffer.

2.2 CPU Interface

- Direct support of the following interfaces:
  Generic MPU bus interface with programmable ready (WAIT#).
  Hitachi SH-4 / SH-3.
  Motorola M68K.
  Motorola MC68EZ328/MC68VZ328 DragonBall.
  Motorola “REDCAP2” - no WAIT# signal.
- “Fixed” low-latency CPU access times.
- Registers are memory-mapped - M/R# input selects between memory and register address space.
- The complete 160k byte display buffer is directly and contiguously available through the 18-bit address bus.

2.3 Display Support

- Single-panel, single drive passive displays.
  - 4/8-bit monochrome LCD interface.
  - 4/8/16-bit color LCD interface.
- Active Matrix TFT interface.
  - 9/12/18-bit interface.
- ‘Direct’ support for 18-bit Sharp HR-TFT LCD or compatible interface.

2.4 Display Modes

- 1/2/4/8/16 bit-per-pixel (bpp) color depths.
- Up to 64 gray shades on monochrome passive LCD panels.
- Up to 64K colors on passive panels.
- Up to 64K colors on active matrix LCD panels.
- Example resolutions:
  320x240 at a color depth of 16 bpp
  320x320 at a color depth of 8 bpp
  160x160 at a color depth of 16 bpp (2 pages)
  160x240 at a color depth of 16 bpp

2.5 Display Features

- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image.
- Virtual display support: displays images larger than the panel size through the use of panning and scrolling.
- Picture-in-Picture Plus (PIP^{+}): displays a variable size window overlaid over background image.
- Pixel Doubling: independent control of both horizontal and vertical pixel doubling.
  - example usage: 160x160 8 bpp can be expanded to 320x320 8 bpp without any additional memory.
- Double Buffering/Multi-pages: provides smooth animation and instantaneous screen updates.

2.6 Clock Source

- Three independent clock inputs: CLKI, CLKI2 and USBCLK.
- Flexible clock source selection:
  - internal Bus Clock (BCLK) selected from CLKI or CLKI/2 (CNF6)
  - internal Memory Clock (MCLK) selected from BCLK or BCLK divide ratio (REG[04h)
  - internal Pixel Clock (PCLK) selected from CLKI, CLKI2, MCLK, or BCLK. PCLK can also be divided down from source (REG[08h])
- Single clock input possible if USB support not required.

2.7 USB Device

- USB Client, revision 1.1 compliant.
- Dedicated clock input: USBCLK.

2.8 2D Acceleration

- 2D BitBLT engine including:

Write BitBLT	Transparent Write BitBLT
Move BitBLT	Transparent Move BitBLT
Solid Fill BitBLT	Read BitBLT
Pattern Fill BitBLT	Color Expansion BitBLT
Move BitBLT with Color Expansion	

2.9 Miscellaneous

- Software Video Invert.
- Software initiated Power Save mode.
- General Purpose Input/Output pins are available.
- IO Operates at 3.3 volts ± 10%.
- Core operates at 2.0 volts ± 10% or 2.5 volts ± 10%.
- 121-pin PFBGA package.
- 128-pin TQFP15 package.

3 Typical System Implementation Diagrams

3.1 Typical System Diagrams.

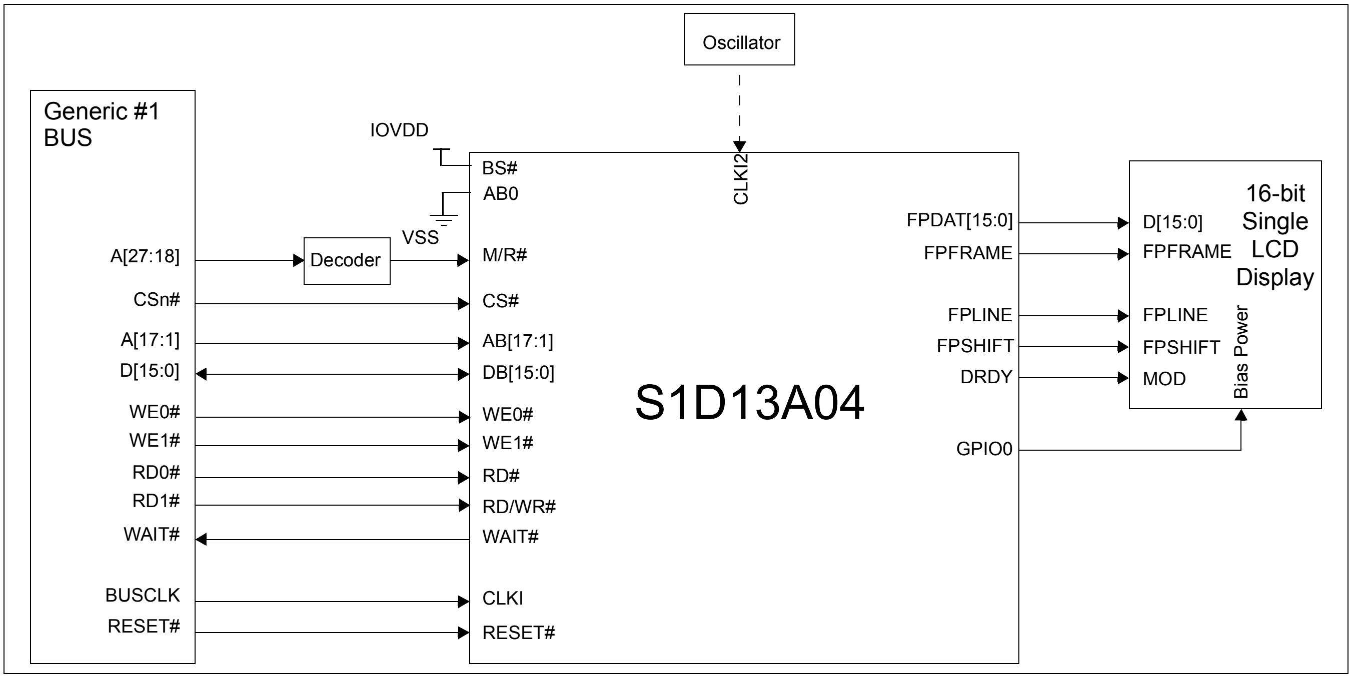


Figure 3-1: Typical System Diagram (Generic #1 Bus)

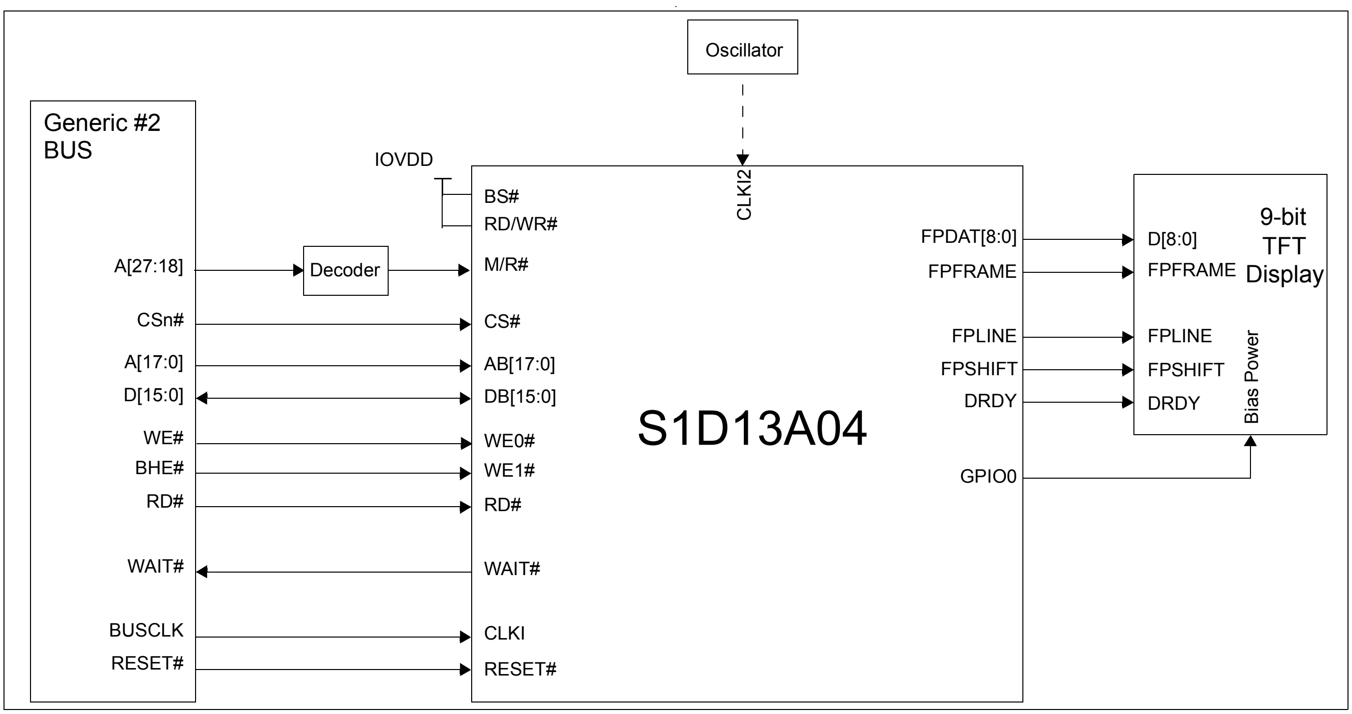


Figure 3-2: Typical System Diagram (Generic #2 Bus)

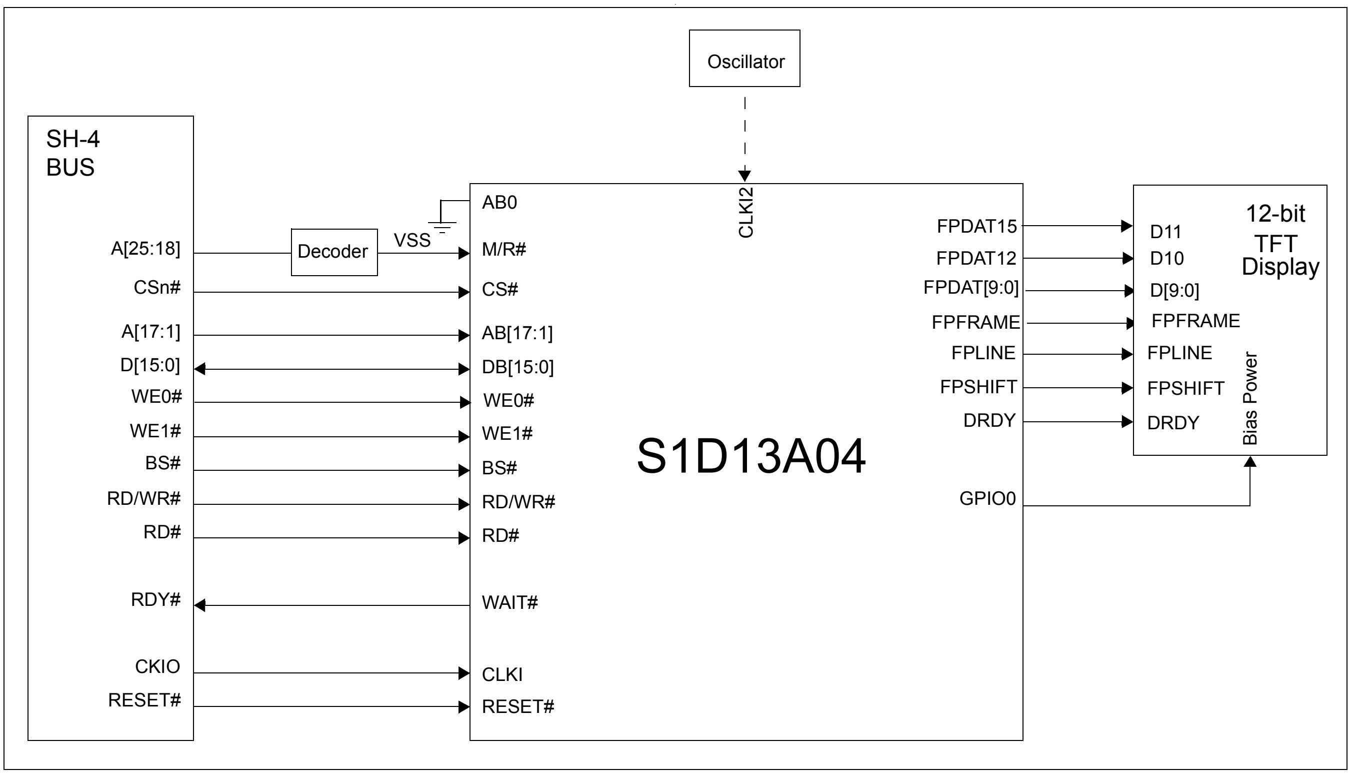


Figure 3-3: Typical System Diagram (Hitachi SH-4 Bus)

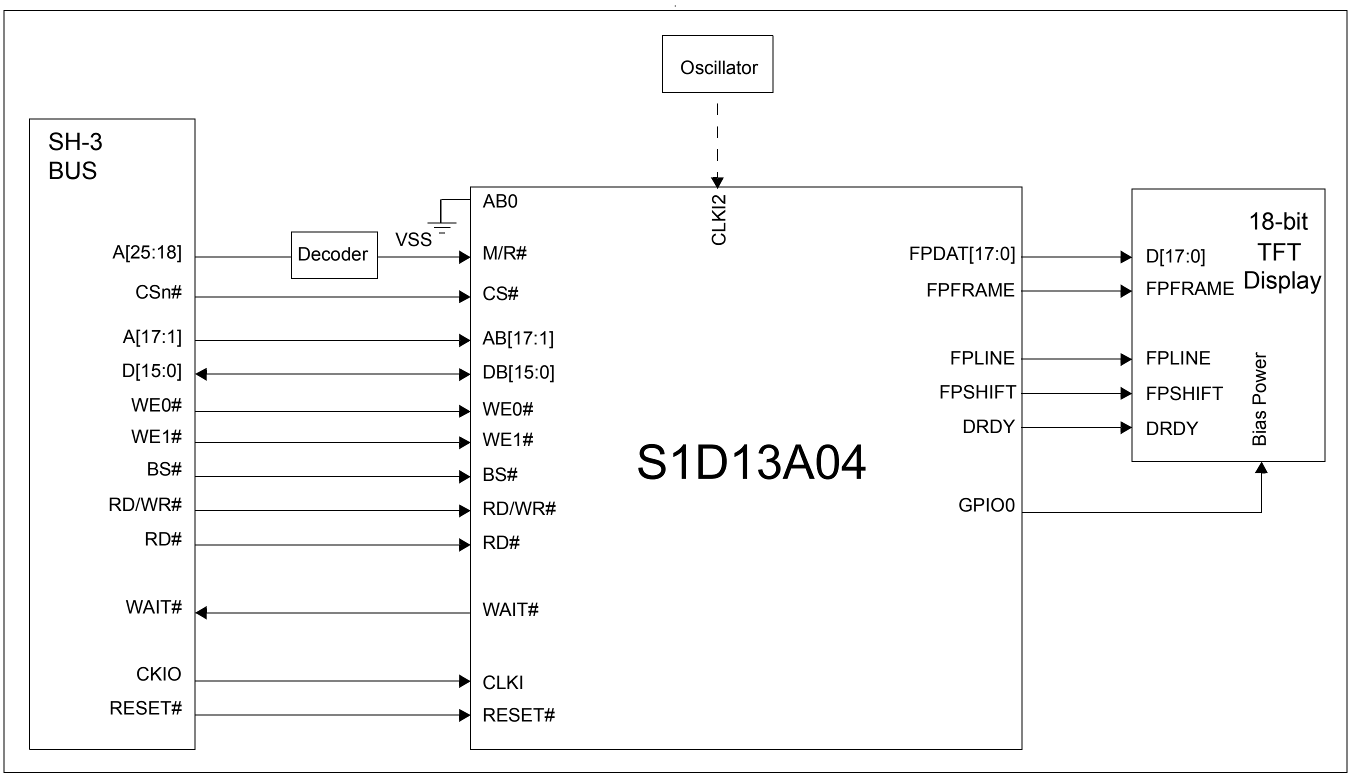


Figure 3-4: Typical System Diagram (Hitachi SH-3 Bus)

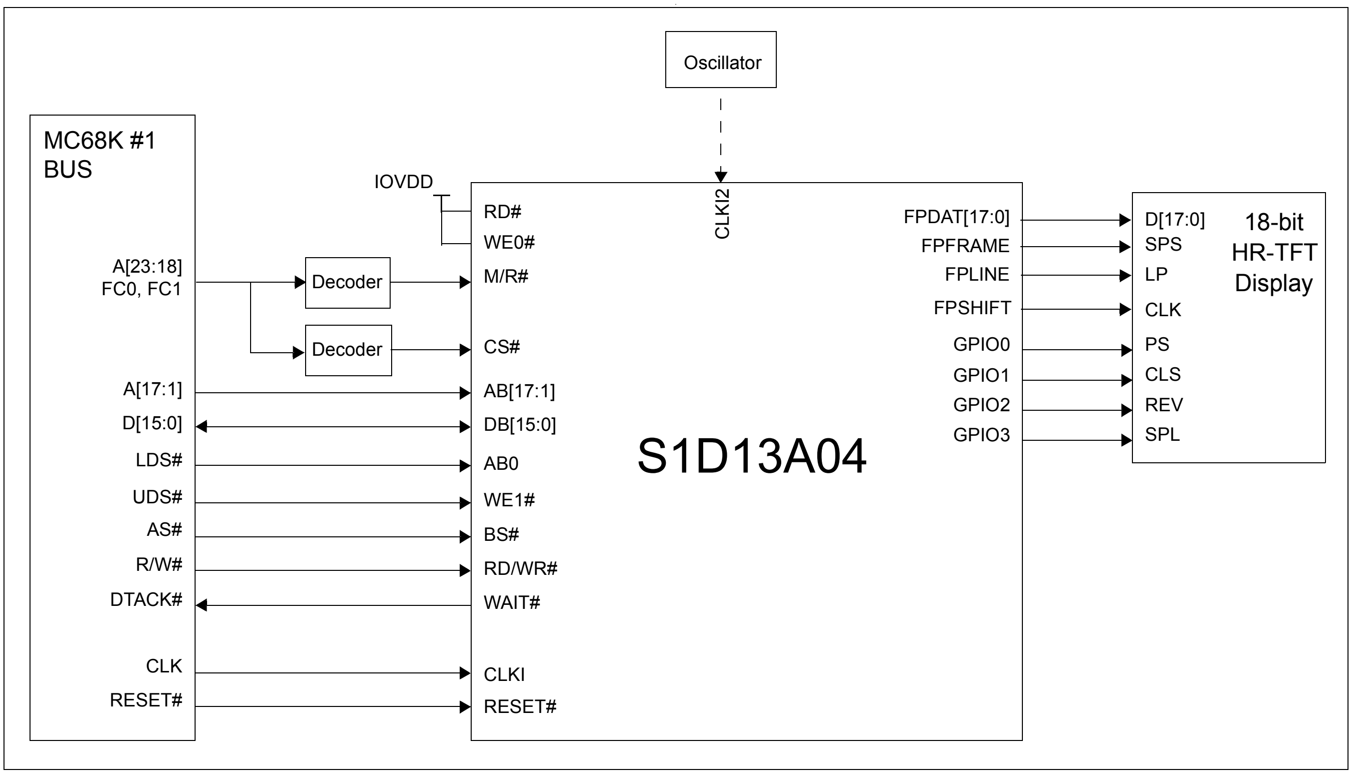


Figure 3-5: Typical System Diagram (MC68K # 1, Motorola 16-Bit 68000)

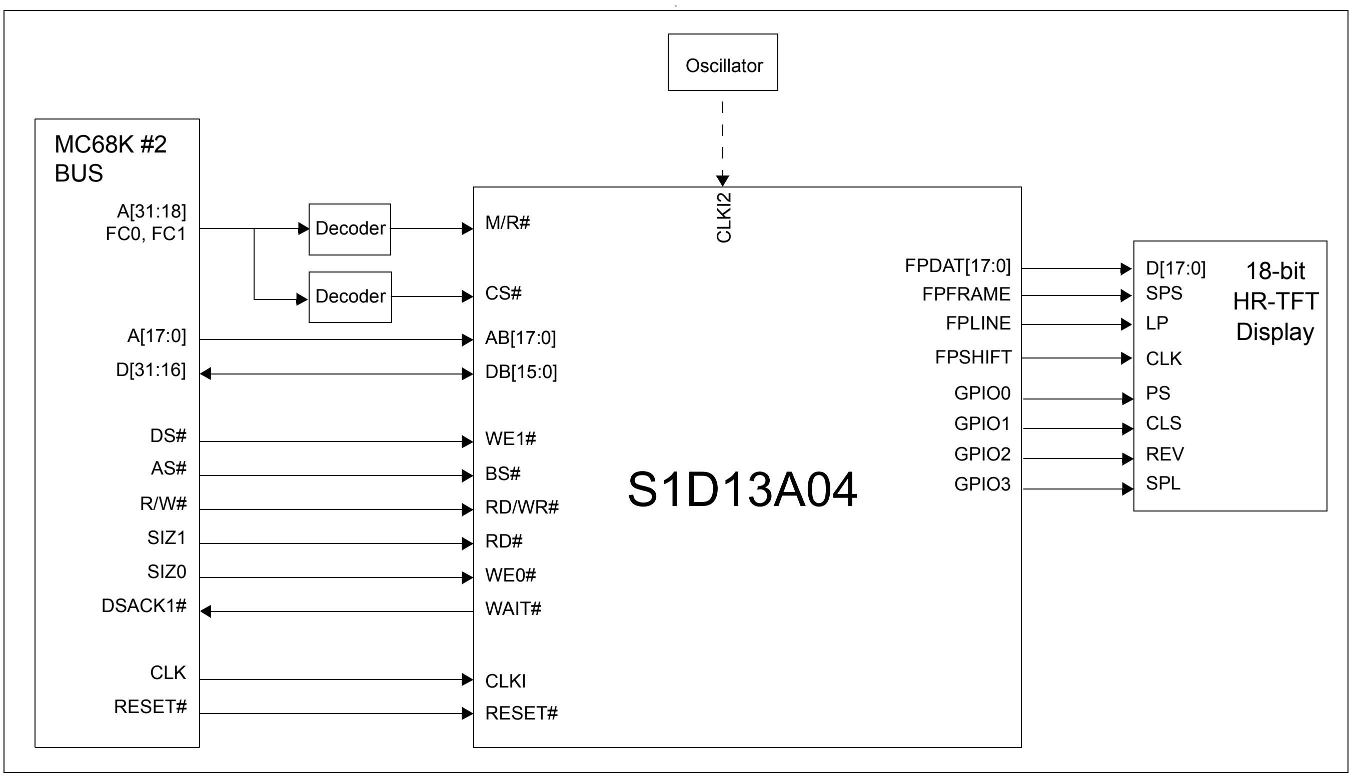


Figure 3-6: Typical System Diagram (MC68K #2, Motorola 32-Bit 68030)

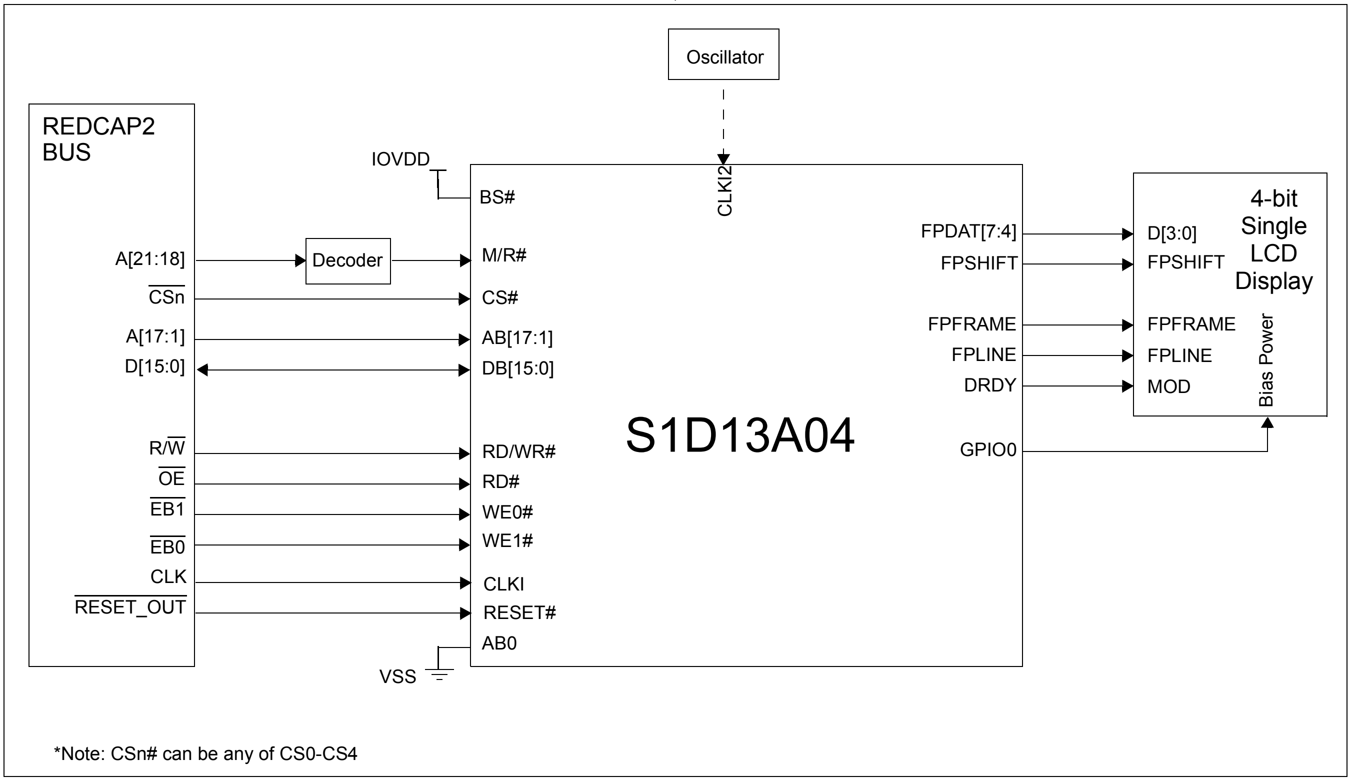


Figure 3-7: Typical System Diagram (Motorola REDCAP2 Bus)

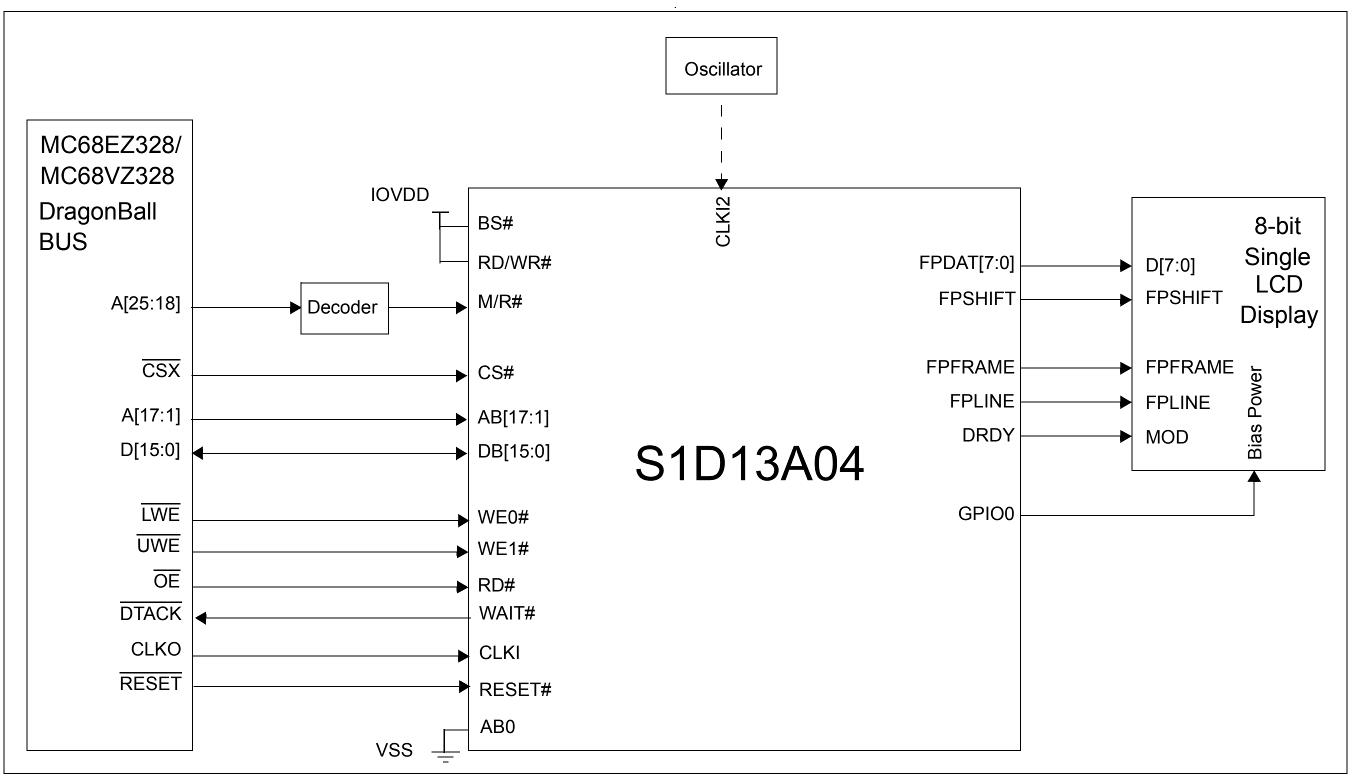


Figure 3-8: Typical System Diagram (Motorola MC68EZ328/MC68VZ328 "DragonBall" Bus)

3.2 USB Interface

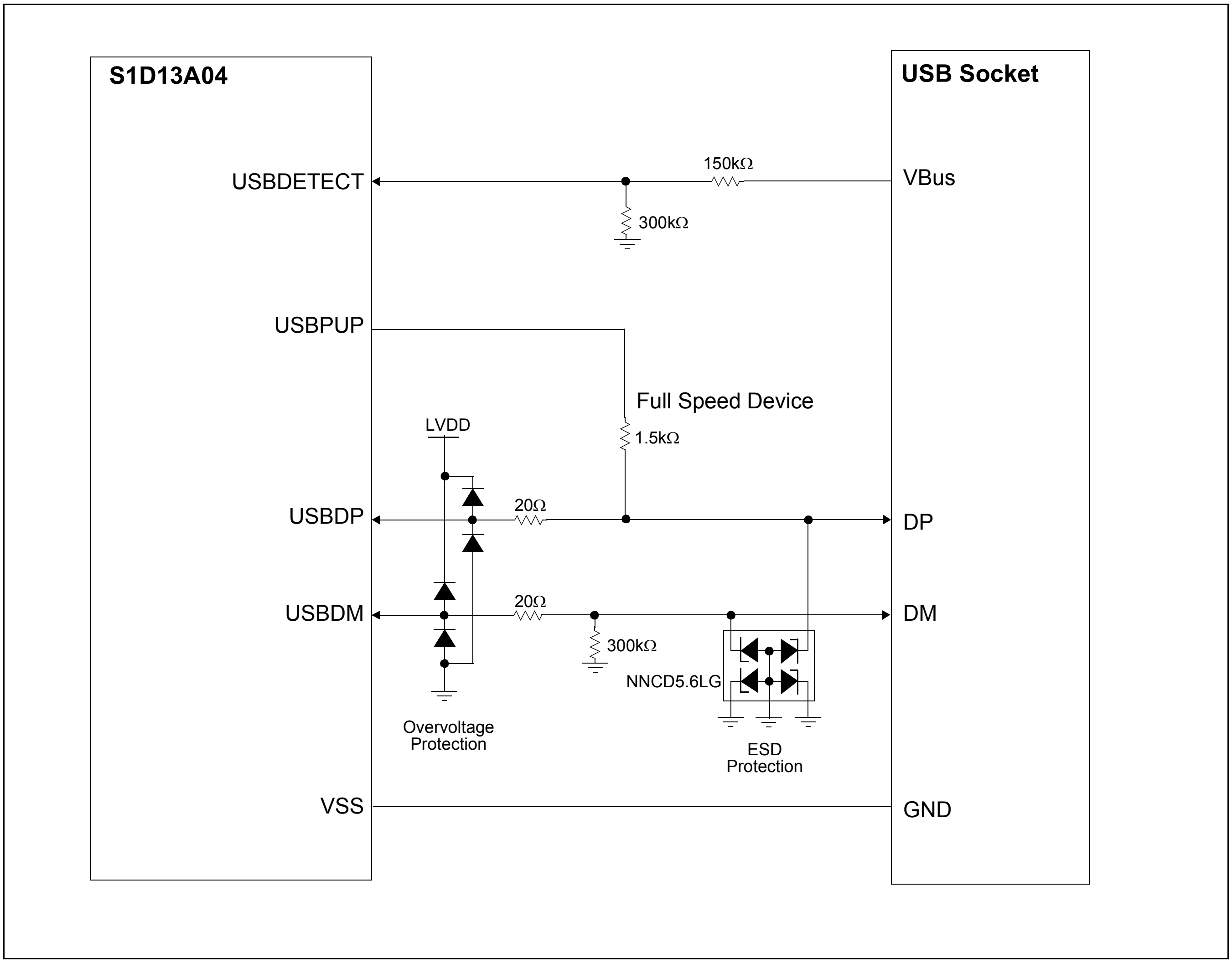


Figure 3-9: USB Typical Implementation

4 Pins

4.1 Pinout Diagram - PFBGA - 121-pin

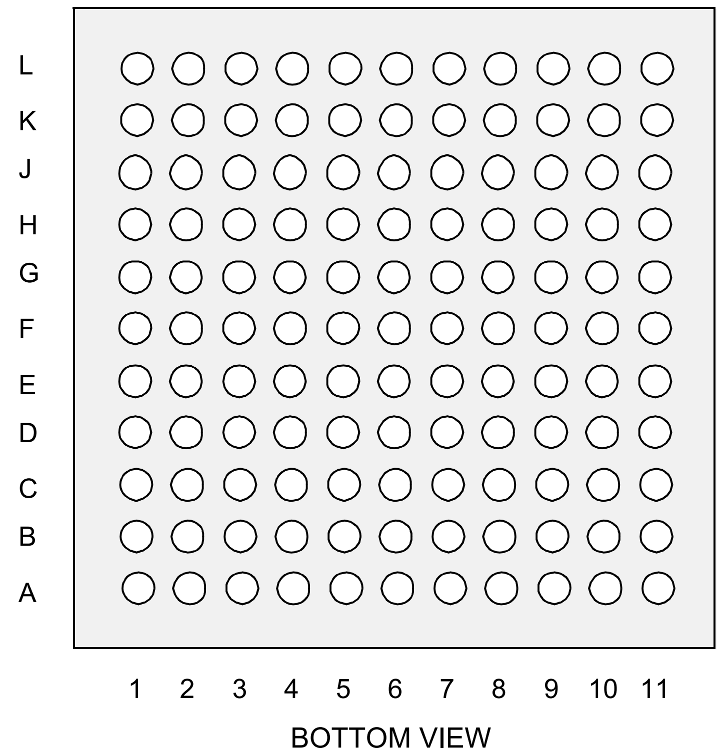


Figure 4-1: Pinout Diagram - PFBGA 121-pin

Table 4-1: PFBGA 121-pin Mapping

L	NC	IOVDD	DB7	DB3	DB0	GPIO7	GPIO3	GPIO0	IOVDD	COREVDD	NC
K	NC	VSS	DB8	DB4	DB1	GPIO6	GPIO2	IRQ	DRDY	VSS	NC
J	NC	DB9	DB6	DB5	DB2	NC	GPIO1	USBCLK	FPFRAME	COREVDD	NC
H	DB12	DB11	DB10	DB13	NC	IOVDD	GPIO4	NC	FPLINE	FPSHIFT	FPDAT0
G	WAIT#	DB15	DB14	IOVDD	VSS	GPIO5	FPDAT5	FPDAT1	FPDAT2	FPDAT3	FPDAT4
F	RESET#	VSS	RD/WR#	WE1#	CLKI	NC	FPDAT8	FPDAT6	VSS	FPDAT7	IOVDD
E	RD#	BS#	M/R#	CS#	WE0#	AB13	TESTEN	FPDAT9	FPDAT12	FPDAT11	FPDAT10
D	AB0	AB1	AB2	AB8	AB12	AB17	CNF3	FPDAT13	FPDAT16	FPDAT15	FPDAT14
C	NC	COREVDD	AB3	AB6	AB9	AB16	CNF2	CNF5	CNF6	FPDAT17	NC
B	NC	VSS	AB5	NC	AB10	AB14	CNF1	CNF4	CLKI2	VSS	NC
A	NC	COREVDD	AB4	AB7	AB11	AB15	CNF0	NC	PWMOUT	IOVDD	NC
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**

4.2 Pinout Diagram - TQFP15 - 128-pin

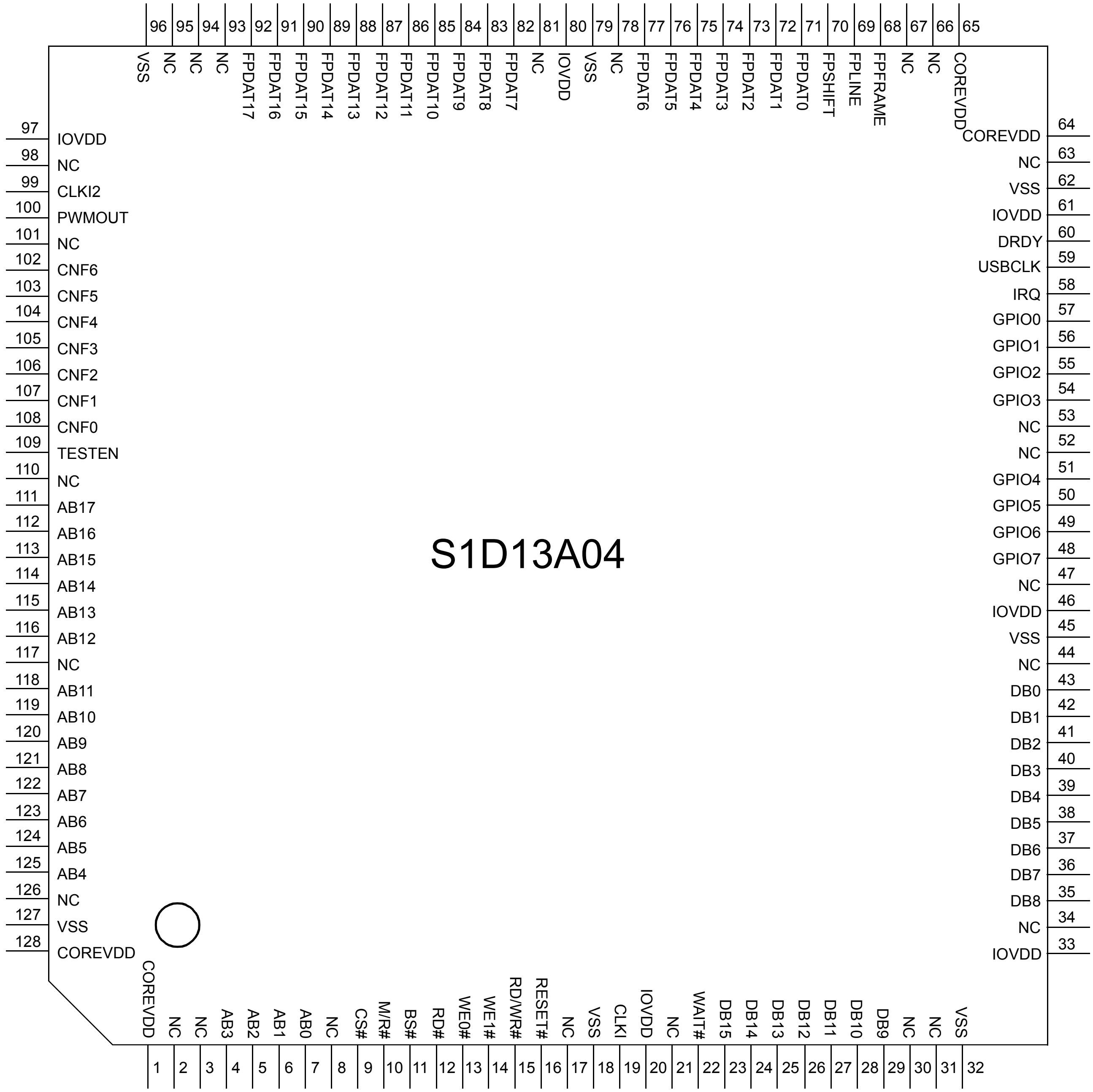


Figure 4-2: Pinout Diagram - TQFP15 128-pin

4.3 Pin Descriptions

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
CI	=	CMOS input
LI	=	LVTTL input
LB2A	=	LVTTL IO buffer (6mA/-6mA@3.3V)
LB3P	=	Low noise LVTTL IO buffer (6mA/-6mA@3.3V)
LO3	=	Low noise LVTTL Output buffer (3mA/-3mA@3.3V)
LB3M	=	Low noise LVTTL IO buffer with input mask (3mA/-3mA@3.3V)
T1	=	Test mode control input with pull-down resistor (typical value of 50KΩ at 3.3V)
Hi-Z	=	High Impedance
CUS	=	Custom Cell Type

[a] LVTTL is Low Voltage TTL (see Section 5, "D.C. Characteristics" on page 29).

4.3.1 Host Interface

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	TQFP15 Pin#	Cell	RESET# State	Description
AB0	I	D1	7	LI	—	This input pin has multiple functions. • For Generic #1, this pin is not used and should be connected to VSS. • For Generic #2, this pin inputs system address bit 0 (A0). • For SH-3/SH-4, this pin is not used and should be connected to VSS. • For MC68K #1, this pin inputs the lower data strobe (LDS#). • For MC68K #2, this pin inputs system address bit 0 (A0). • For REDCAP2, this pin is not used and should be connected to VSS. • For DragonBall, this pin is not used and should be connected to VSS. See Table 4-8: "Host Bus Interface Pin Mapping," on page 27 for summary.
AB[17:1]	I	D6, C6, A6, B6, E6, D5, A5, B5, C5, D4, A4, C4, B3, A3, C3, D3, D2	111-116, 118-125, 4-6	CI	—	System address bus bits 17-1.

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	TQFP15 Pin#	Cell	RESET# State	Description
DB[15:0]	IO	G2, G3, H4, H1, H2, H3, J2, K3, L3, J3, J4, K4, L4, J5, K5, L5	23-29, 35-43	LB2A	Hi-Z	Input data from the system data bus. • For Generic #1, these pins are connected to D[15:0]. • For Generic #2, these pins are connected to D[15:0]. • For SH-3/SH-4, these pins are connected to D[15:0]. • For MC68K #1, these pins are connected to D[15:0]. • For MC68K #2, these pins are connected to D[31:16] for a 32-bit device (e.g. MC68030) or D[15:0] for a 16-bit device (e.g. MC68340). • For REDCAP2, these pins are connected to D[15:0]. • For DragonBall, these pins are connected to D[15:0]. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.
WE0#	I	E5	13	LI	—	This input pin has multiple functions. • For Generic #1, this pin inputs the write enable signal for the lower data byte (WE0#). • For Generic #2, this pin inputs the write enable signal (WE#) • For SH-3/SH-4, this pin inputs the write enable signal for data byte 0 (WE0#). • For MC68K #1, this pin must be tied to IO V_{DD} • For MC68K #2, this pin inputs the bus size bit 0 (SIZ0). • For REDCAP2, this pin inputs the byte enable signal for the D[7:0] data byte (EB1). • For DragonBall, this pin inputs the byte enable signal for the D[7:0] data byte (LWE). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.
WE1#	I	F4	14	LI	—	This input pin has multiple functions. • For Generic #1, this pin inputs the write enable signal for the upper data byte (WE1#). • For Generic #2, this pin inputs the byte enable signal for the high data byte (BHE#). • For SH-3/SH-4, this pin inputs the write enable signal for data byte 1 (WE1#). • For MC68K #1, this pin inputs the upper data strobe (UDS#). • For MC68K #2, this pin inputs the data strobe (DS#). • For REDCAP2, this pin inputs the byte enable signal for the D[15:8] data byte (EB0). • For DragonBall, this pin inputs the byte enable signal for the D[15:8] data byte (UWE). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.
CS#	I	E4	9	CI	—	Chip select input. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	TQFP15 Pin#	Cell	RESET# State	Description
M/R#	I	E3	10	LI	—	This input pin is used to select between the display buffer and register address spaces of the S1D13A04. M/R# is set high to access the display buffer and low to access the registers. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.
BS#	I	E2	11	LI	—	This input pin has multiple functions. • For Generic #1, this pin must be tied to IO V_{DD}. • For Generic #2, this pin must be tied to IO V_{DD}. • For SH-3/SH-4, this pin inputs the bus start signal (BS#). • For MC68K #1, this pin inputs the address strobe (AS#). • For MC68K #2, this pin inputs the address strobe (AS#). • For REDCAP2, this pin must be tied to IO V_{DD}. • For DragonBall, this pin must be tied to IO V_{DD}. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.
RD/WR#	I	F3	15	LI	—	This input pin has multiple functions. • For Generic #1, this pin inputs the read command for the upper data byte (RD1#). • For Generic #2, this pin must be tied to IO V_{DD}. • For SH-3/SH-4, this pin inputs the RD/WR# signal. The S1D13A04 needs this signal for early decode of the bus cycle. • For MC68K #1, this pin inputs the R/W# signal. • For MC68K #2, this pin inputs the R/W# signal. • For REDCAP2, this pin inputs the $R/\overline{W}$ signal. • For DragonBall, this pin must be tied to IO V_{DD}. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.
RD#	I	E1	12	LI	—	This input pin has multiple functions. • For Generic #1, this pin inputs the read command for the lower data byte (RD0#). • For Generic #2, this pin inputs the read command (RD#). • For SH-3/SH-4, this pin inputs the read signal (RD#). • For MC68K #1, this pin must be tied to IO V_{DD}. • For MC68K #2, this pin inputs the bus size bit 1 (SIZ1). • For REDCAP2, this pin inputs the output enable ($\overline{OE}$). • For DragonBall, this pin inputs the output enable ($\overline{OE}$). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary.

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	TQFP15 Pin#	Cell	RESET# State	Description
WAIT#	IO	G1	22	LB2A	Hi-Z	During a data transfer, this output pin is driven active to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to the high impedance state after the data transfer is complete. Its active polarity is configurable. See Table 4-7: “Summary of Power-On/Reset Options,” on page 26. • For Generic #1, this pin outputs the wait signal (WAIT#). • For Generic #2, this pin outputs the wait signal (WAIT#). • For SH-3 mode, this pin outputs the wait request signal (WAIT#). • For SH-4 mode, this pin outputs the device ready signal (RDY#). • For MC68K #1, this pin outputs the data transfer acknowledge signal (DTACK#). • For MC68K #2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#). • For REDCAP2, this pin is unused (Hi-Z). • For DragonBall, this pin outputs the data transfer acknowledge signal (DTACK). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 27 for summary. **Note:** This pin should be tied to the inactive voltage level as selected by CNF5, using a pull-up or pull-down resistor. If CNF5 = 1, the WAIT# pin should be tied low using a pull-down resistor. If CNF5 = 0, the WAIT# pin should be tied high using a pull-up resistor. If WAIT# is not used, this pin should be tied either high or low using a pull-up or pull-down resistor.
RESET#	I	F1	16	LI	—	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

4.3.2 LCD Interface

Table 4-3: LCD Interface Pin Descriptions

Pin Name	Type	PFBGA Pin#	TQFP15 Pin#	Cell	RESET# State	Description
FPDAT[17:0]	O	C10, D9, D10, D11, D8, E9, E10, E11, E8, F7, F10, F8, G7, G11, G10, G9, G8, H11	92, 91, 90, 89, 88, 87, 86, 85, 84, 83, 82, 77, 76, 75, 74, 73, 72, 71	LB3P	0	Panel Data bits 17-0.
FPFRAME	O	J9	68	LB3P	0	This output pin has multiple functions. • Frame Pulse • SPS for ‘Direct’ HR-TFT See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
FPLINE	O	H9	69	LB3P	0	This output pin has multiple functions. • Line Pulse • LP for ‘Direct’ HR-TFT See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
FPSHIFT	O	H10	70	LB3P	0	This output pin has multiple functions. • Shift Clock • CLK for ‘Direct’ HR-TFT See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
DRDY	O	K9	60	LO3	0	This output pin has multiple functions. • Display enable (DRDY) for TFT panels • 2nd shift clock (FPSHIFT2) for passive LCD with Format 1 interface • LCD backplane bias signal (MOD) for all other LCD panels • General Purpose Output See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
GPIO0	IO	L8	57	LB3M	—	This pin has multiple functions. • PS for ‘Direct’ HR-TFT • General purpose IO pin 0 (GPIO0) GPIO0 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is used for HR-TFT, it must be configured as an output using REG[64h]. Otherwise, it must either be configured as an output or be pulled high or low externally to avoid unnecessary current drain. See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.

Table 4-3: LCD Interface Pin Descriptions

Pin Name	Type	PFBGA Pin#	TQFP15 Pin#	Cell	RESET# State	Description
GPIO1	IO	J7	56	LB3M	—	This pin has multiple functions. • CLS for ‘Direct’ HR-TFT • General purpose IO pin 1 (GPIO1) GPIO1 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is used for HR-TFT, it must be configured as an output using REG[64h]. Otherwise, it must either be configured as an output or be pulled high or low externally to avoid unnecessary current drain. See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
GPIO2	IO	K7	55	LB3M	—	This pin has multiple functions. • REV for ‘Direct’ HR-TFT • General purpose IO pin 2 (GPIO2) GPIO2 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is used for HR-TFT, it must be configured as an output using REG[64h]. Otherwise, it must either be configured as an output or be pulled high or low externally to avoid unnecessary current drain. See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
GPIO3	IO	L7	54	LB3M	—	This pin has multiple functions. • SPL for ‘Direct’ HR-TFT • General purpose IO pin 3 (GPIO3) GPIO3 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is used for HR-TFT, it must be configured as an output using REG[64h]. Otherwise, it must either be configured as an output or be pulled high or low externally to avoid unnecessary current drain. See Table 4.6 “LCD Interface Pin Mapping,” on page 28 for summary.
GPIO4	IO	H7	51	LB3M	—	This pin has multiple functions. • USBPUP • General purpose IO pin 4 (GPIO4) GPIO4 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is not used for USB, it must either be configured as an output using REG[64h] or be pulled high or low externally to avoid unnecessary current drain.

Table 4-3: LCD Interface Pin Descriptions

Pin Name	Type	PFBGA Pin#	TQFP15 Pin#	Cell	RESET# State	Description
GPIO5	IO	G6	50	LB3M	—	This pin has multiple functions. • USBDETECT • General purpose IO pin 5 (GPIO5) GPIO5 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is not used for USB, it must either be configured as an output using REG[64h] or be pulled high or low externally to avoid unnecessary current drain.
GPIO6	IO	K6	49	CUS	—	This pin has multiple functions. • USBDM • General purpose IO pin 6 (GPIO6) GPIO6 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is not used for USB, it must either be configured as an output using REG[64h] or be pulled high or low externally to avoid unnecessary current drain.
GPIO7	IO	L6	48	CUS	—	This pin has multiple functions. • USBDP • General purpose IO pin 7 GPIO7 defaults to a Hi-Z state during every RESET and defaults to an input after every RESET. When this pin is not used for USB, it must either be configured as an output using REG[64h] or be pulled high or low externally to avoid unnecessary current drain.
IRQ	O	K8	58	LO3	0	This output pin is the IRQ pin for USB. When IRQ is activated, an active high pulse is generated and stays high until the IRQ is serviced by software at REG[404Ah] or REG[404Ch].
PWMOUT	O	A9	100	LO3	0	This pin has multiple functions. • PWM Clock output • General purpose output

4.3.3 Clock Input

Table 4-4: Clock Input Pin Descriptions

Pin Name	Type	PFBGA Pin#	TQFP15 Pin#	Cell	RESET# State	Description
CLKI	I	F5	19	CI	—	Typically used as input clock source for bus clock and memory clock
CLKI2	I	B9	99	CI	—	Typically used as input clock source for pixel clock
USBCLK	I	J8	59	LI	—	Typically used as input clock source for USB

4.3.4 Miscellaneous

Table 4-5: Miscellaneous Pin Descriptions

Pin Name	Type	PFBGA Pin#	TQFP15 Pin#	Cell	RESET# State	Description
CNF[6:0]	I	C9, C8, B8, D7, C7, B7, A7	102-108	CI	—	These inputs are used to configure the S1D13A04 - see Table 4-7: “Summary of Power-On/Reset Options,” on page 26. **Note: These pins are used for configuration of the S1D13A04 and must be connected directly to IO V_{DD} or V_{SS}.**
TESTEN	I	E7	109	T1	—	Test Enable input used for production test only (has type 1 pull-down resistor with a typical value of 50KΩ at 3.3V). **Note: This pin must not be connected.**

4.3.5 Power And Ground

Table 4-6: Power And Ground Pin Descriptions

Pin Name	Type	PFBGA Pin#	TQFP15 Pin#	Cell	RESET# State	Description
IOVDD	P	L2, G4, H6, L9, A10, F11	20, 33, 46, 61, 80, 97	P	—	6 IO V_{DD} pins.
COREVDD	P	A2, C2, L10, J10	1, 64-65, 128	P	—	2 double-bonded Core $V_{DD.}$ pins on TQFP package. 4 Core $V_{DD.}$ pins on PFBGA package.
VSS	P	B2, F2, K2, G5, F9, B10, K10	18, 32, 45, 62, 79, 96, 127	P	—	7 V_{SS} pins.

4.4 Summary of Configuration Options

These pins are used for configuration of the S1D13A04 and must be connected directly to IOV_{DD} or V_{SS}. The state of CNF[6:0] are latched on the rising edge of RESET#. Changing state at any other time has no effect.

Table 4-7: Summary of Power-On/Reset Options

<table>
<tr><th rowspan="2">S1D13A04 Configuration Input</th><th colspan="2">Power-On/Reset State</th></tr>
<tr><th>1 (connected to IO V_{DD})</th><th>0 (connected to V_{SS})</th></tr>
<tr><td>CNF4,CNF[2:0]</td><td colspan="2">Select host bus interface as follows:
<table>
<tr><th>CNF4</th><th>CNF2</th><th>CNF1</th><th>CNF0</th><th>Host Bus</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>SH-4/SH-3 interface, Big Endian</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>SH-4/SH-3 interface, Little Endian</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>MC68K #1, Big Endian</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>MC68K #2, Big Endian</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Generic #1, Big Endian</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Generic #1, Little Endian</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Generic #2, Little Endian</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>REDCAP2, Big Endian</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>DragonBall (MC68EZ328/MC68VZ328), Big Endian</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>CNF3</td><td colspan="2">Reserved. Must be set to 1.</td></tr>
<tr><td>CNF5
(see note)</td><td>WAIT# is active high</td><td>WAIT# is active low</td></tr>
<tr><td>CNF6</td><td>CLKI to BCLK divide ratio 2:1</td><td>CLKI to BCLK divide ratio 1:1</td></tr>
</table>

Note

If CNF5 = 1, the WAIT# pin should be tied low using a pull-down resistor. If CNF5 = 0, the WAIT# pin should be tied high using a pull-up resistor. If WAIT# is not used, this pin should be tied either high or low using a pull-up or pull-down resistor.

4.5 Host Bus Interface Pin Mapping

Table 4-8: Host Bus Interface Pin Mapping

S1D13A04 Pin Name	Generic #1	Generic #2	Hitachi SH-3 /SH-4	Motorola MC68K #1	Motorola MC68K #2	Motorola REDCAP2	Motorola MC68EZ328/ MC68VZ328 DragonBall
AB[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]
AB0	A0[1]	A0	A0[1]	LDS#	A0	A0[1]	A0[1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0][2]	D[15:0]	D[15:0]
CS#	External Decode		CSn#	External Decode		$\overline{\text{CSn}}$	$\overline{\text{CSX}}$
M/R#	External Decode						
CLKI	BUSCLK	BUSCLK	CKIO	CLK	CLK	CLK	CLKO
BS#	Connected to IO V_{DD}		BS#	AS#	AS#	Connected to IO V_{DD}	
RD/WR#	RD1#	Connected to IO V_{DD}	RD/WR#	R/W#	R/W#	R/$\overline{\text{W}}$	Connected to IO V_{DD}
RD#	RD0#	RD#	RD#	Connected to IO V_{DD}	SIZ1	$\overline{\text{OE}}$	$\overline{\text{OE}}$
WE0#	WE0#	WE#	WE0#	Connected to IO V_{DD}	SIZ0	$\overline{\text{EB1}}$	$\overline{\text{LWE}}$
WE1#	WE1#	BHE#	WE1#	UDS#	DS#	$\overline{\text{EB0}}$	$\overline{\text{UWE}}$
WAIT#	WAIT#	WAIT#	WAIT#/ RDY#	DTACK#	DSACK1#	N/A	$\overline{\text{DTACK}}$
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	$\overline{\text{RESET\_OUT}}$	$\overline{\text{RESET}}$

Note

[1] A0 for these busses is not used internally by the S1D13A04 and should be connected to V_{SS}.

[2] If the target MC68K bus is 32-bit, then these signals should be connected to D[31:16].

4.6 LCD Interface Pin Mapping

Table 4-9: LCD Interface Pin Mapping

Pin Name	Monochrome Passive Panel		Color Passive Panel				Color TFT Panel			
	Single		Single				Others			'Direct' HR-TFT[1]
				Format 1	Format 2					
	4-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit
FPFRAME	FPFRAME									SPS
FPLINE	FPLINE									LP
FPSHIFT	FPSHIFT									DCLK
DRDY	MOD			FPSHIFT2	MOD		DRDY			GPO[2]
FPDAT0	driven 0	D0	driven 0	D0 (B5)[3]	D0 (G3)[3]	D0 (R6)[3]	R2	R3	R5	R5
FPDAT1	driven 0	D1	driven 0	D1 (R5)[3]	D1 (R3)[3]	D1 (G5)[3]	R1	R2	R4	R4
FPDAT2	driven 0	D2	driven 0	D2 (G4)[3]	D2 (B2)[3]	D2 (B4)[3]	R0	R1	R3	R3
FPDAT3	driven 0	D3	driven 0	D3 (B3)[3]	D3 (G2)[3]	D3 (R4)[3]	G2	G3	G5	G5
FPDAT4	D0	D4	D0 (R2)[3]	D4 (R3)[3]	D4 (R2)[3]	D8 (B5)[3]	G1	G2	G4	G4
FPDAT5	D1	D5	D1 (B1)[3]	D5 (G2)[3]	D5 (B1)[3]	D9 (R5)[3]	G0	G1	G3	G3
FPDAT6	D2	D6	D2 (G1)[3]	D6 (B1)[3]	D6 (G1)[3]	D10 (G4)[3]	B2	B3	B5	B5
FPDAT7	D3	D7	D3 (R1)[3]	D7 (R1)[3]	D7 (R1)[3]	D11 (B3)[3]	B1	B2	B4	B4
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	D4 (G3)[3]	B0	B1	B3	B3
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	D5 (B2)[3]	driven 0	R0	R2	R2
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	D6 (R2)[3]	driven 0	driven 0	R1	R1
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	D7 (G1)[3]	driven 0	driven 0	R0	R0
FPDAT12	driven 0	driven 0	driven 0	driven 0	driven 0	D12 (R3)[3]	driven 0	G0	G2	G2
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	D13 (G2)[3]	driven 0	driven 0	G1	G1
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	D14 (B1)[3]	driven 0	driven 0	G0	G0
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	D15 (R1)[3]	driven 0	B0	B2	B2
FPDAT16	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B1	B1
FPDAT17	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B0	B0
GPIO0	GPIO0									PS
GPIO1	GPIO1									CLS
GPIO2	GPIO2									REV
GPIO3	GPIO3									SPL

Note

1 GPIO pins default to inputs at reset and require special configuration using REG[64h] when the 'Direct' HR-TFT interface is desired.

2 When the 'Direct' HR-TFT interface is selected (REG[0Ch] bits 1-0 = 10), DRDY becomes a general purpose output (GPO) controllable using the 'Direct' HR-TFT LCD Interface GPO Control bit (REG[14h] bit 0). This GPO can be used to control the HR-TFT MOD signal if required. For further information, see the bit description for REG[14h] bit 0.

3 These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see Section 6.5, "Display Interface" on page 54.

5 D.C. Characteristics

Note

When applying Supply Voltages to the S1D13A04, Core V_{DD} must be applied to the chip before, or simultaneously with IO V_{DD}, or damage to the chip may result.

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Supply Voltage	V_{SS} - 0.3 to 3.0	V
IO V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	1.8 (note 1)	2.0 (note 1)	2.2 (note 1)	V
		V_{SS} = 0 V	2.25	2.5	2.75	V
IO V_{DD}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
V_{IN}	Input Voltage		V_{SS}		IO V_{DD}	V
			V_{SS}		CORE V_{DD}	
T_{OPR}	Operating Temperature		-40	25	85	° C

1. When Core V_{DD} is 2.0V ± 10%, the MCLK must be less than or equal to 30MHz (MCLK ≤ 30MHz)

Table 5-3: Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			170	µA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	VDD = min. I_{OH} = -3mA (Type 1) -6mA (Type 2)	V_{DD} - 0.4			V
V_{OL}	Low Level Output Voltage	VDD = min. I_{OL} = 3mA (Type 1) 6mA (Type 2)			0.4	V
V_{IH}	High Level Input Voltage	LVTTL Level, V_{DD} = max	2.0			V
V_{IL}	Low Level Input Voltage	LVTTL Level, V_{DD} = min			0.8	V
R_{PD}	Pull Down Resistance	V_{IN} = V_{DD}	20	50	120	kΩ
C_I	Input Pin Capacitance				10	pF
C_O	Output Pin Capacitance				10	pF
C_{IO}	Bi-Directional Pin Capacitance				10	pF

6 A.C. Characteristics

Conditions: IO V_{DD} = 3.3V ± 10%
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 50pF (Bus/MPU Interface)
C_L = 0pF (LCD Panel Interface)

6.1 Clock Timing

6.1.1 Input Clocks

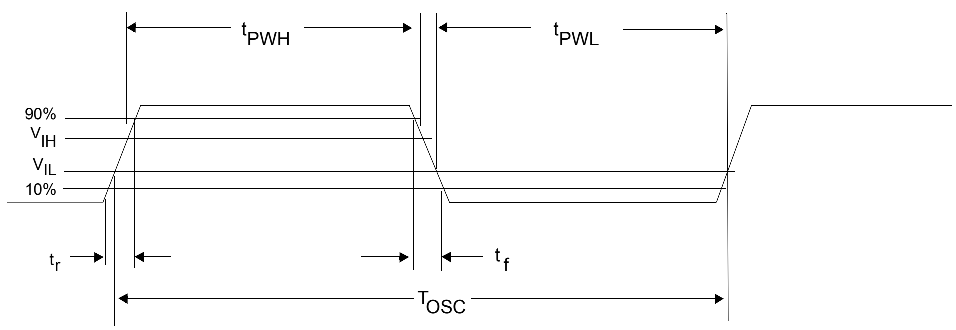


Figure 6-1: Clock Input Requirements

Table 6-1: Clock Input Requirements for CLKI when CLKI to BCLK divide > 1

Symbol	Parameter	Min	Max	Units
f_{OSC}	Input Clock Frequency (CLKI)		100	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	4.5		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	4.5		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Note
Maximum internal requirements for clocks derived from CLKI must be considered when determining the frequency of CLKI. See Section 6.1.2, “Internal Clocks” on page 31 for internal clock requirements.

Table 6-2: Clock Input Requirements for CLKI when CLKI to BCLK divide = 1

Symbol	Parameter	Min	Max	Units
f_{OSC}	Input Clock Frequency (CLKI)		66	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	3		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	3		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Note
Maximum internal requirements for clocks derived from CLKI must be considered when determining the frequency of CLKI. See Section 6.1.2, “Internal Clocks” on page 31 for internal clock requirements.

Table 6-3: Clock Input Requirements for CLKI2

Symbol	Parameter	Min	Max	Units
f_{OSC}	Input Clock Frequency (CLKI2)		66	MHz
T_{OSC}	Input Clock period (CLKI2)	$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI2)	3		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI2)	3		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Note
Maximum internal requirements for clocks derived from CLKI2 must be considered when determining the frequency of CLKI2. See Section 6.1.2, “Internal Clocks” on page 31 for internal clock requirements.

6.1.2 Internal Clocks

Table 6-4: Internal Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{BCLK}	Bus Clock frequency		66	MHz
f_{MCLK}	Memory Clock frequency		50 (note 1,note 2)	MHz
f_{PCLK}	Pixel Clock frequency		50	MHz
f_{PWMCLK}	PWM Clock frequency		66	MHz

1. When COREVDD = 2.0V ±10% f_{MCLK} max = 30MHz.
2. MCLK is derived from BCLK, therefore when BCLK is greater than 50MHz, MCLK must be divided using REG[04h] bits 5-4.

Note
For further information on internal clocks, refer to Section 7, “Clocks” on page 83.

6.2 RESET# Timing

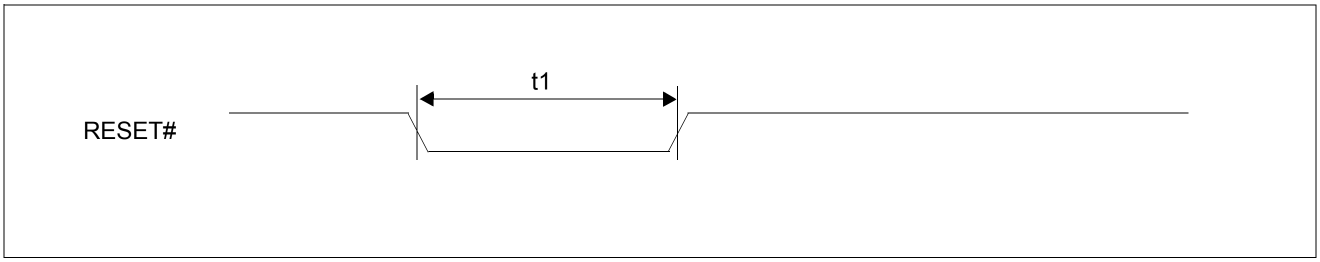


Figure 6-2 S1D13A04 RESET# Timing

Table 6-5 S1D13A04 RESET# Timing

Symbol	Parameter	Min	Max	Units
t1	Active Reset Pulse Width	1	—	CLKI

6.3 CPU Interface Timing

6.3.1 Generic #1 Interface Timing (e.g. Epson EOC33)

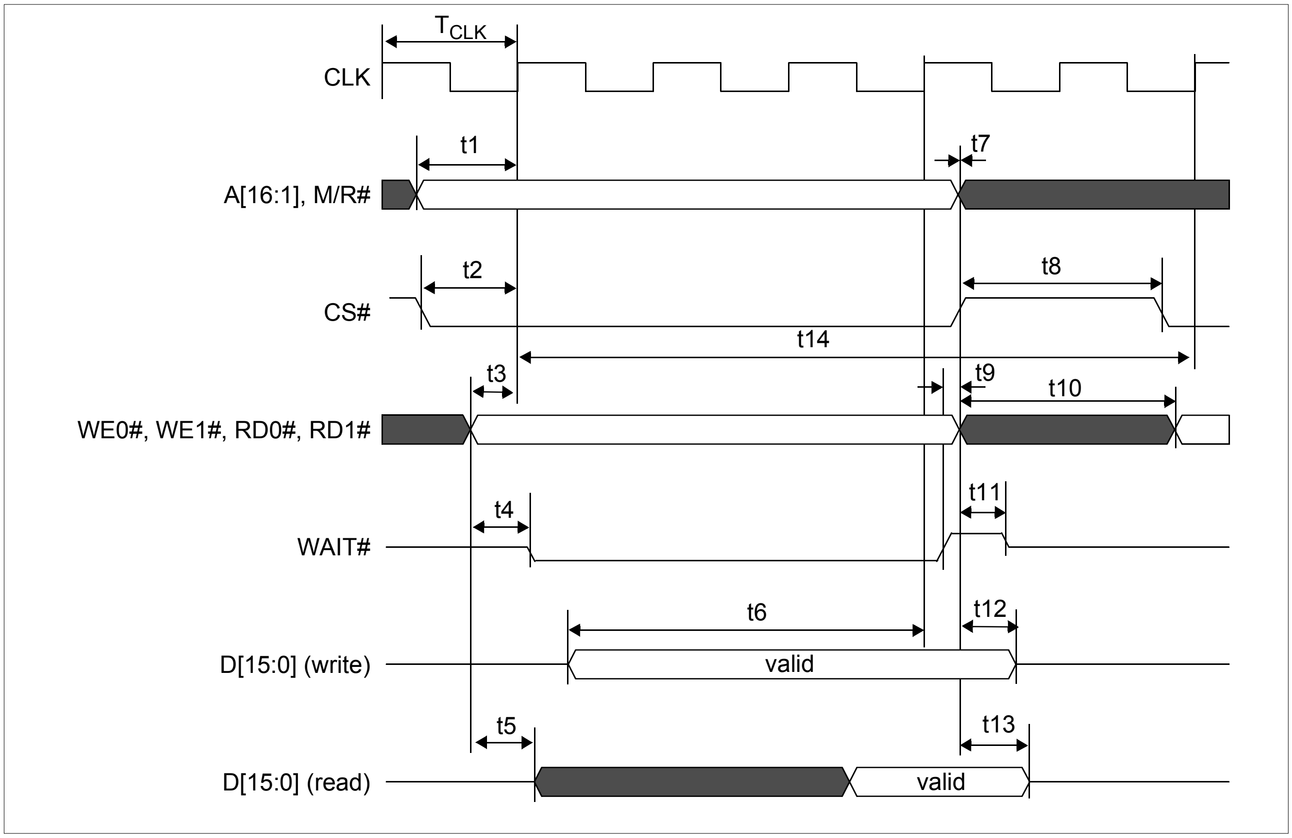


Figure 6-3: Generic #1 Interface Timing

Table 6-6: Generic #1 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{CLK}	Bus clock frequency		50	MHz
T_{CLK}	Bus clock period	$1/f_{CLK}$		ns
t1	A[16:1], M/R# setup to first CLK rising edge where CS# = 0 and either RD0#, RD1# = 0 or WE0#, WE1# = 0	9		ns
t2	CS# setup to CLK rising edge	9		ns
t3	RD0#, RD1#, WE0#, WE1# setup to CLK rising edge	1		ns
t4	RD0#, RD1# or WE0#, WE1# state change to WAIT# driven low	1	10	ns
t5	RD0#, RD1# falling edge to D[15:0] driven (read cycle)	2	10	ns
t6	D[15:0] setup to 4th rising CLK edge after CS#=0 and WE0#, WE1#=0	1		T_{CLK}
t7	A[16:1], M/R# and CS# hold from RD0#, RD1#, WE0#, WE1# rising edge	0		ns
t8	CS# deasserted to reasserted	0		ns
t9	WAIT# rising edge to RD0#, RD1#, WE0#, WE1# rising edge	0		ns
t10	WE0#, WE1#, RD0#, RD1# deasserted to reasserted	1		T_{CLK}
t11	Rising edge of either RD0#, RD1# or WE0#, WE1# to WAIT# high impedance		0.5	T_{CLK}
t12	D[15:0] hold from WE0#, WE1# rising edge (write cycle)	2		ns
t13	D[15:0] hold from RD0#, RD1# rising edge (read cycle)	1		ns
t14	Cycle Length	5		T_{CLK}

Table 6-7: Generic #1 Interface Truth Table for Little Endian

WE0#	WE1#	RD0#	RD1#	D[15:8]	D[7:0]	Comments
0	0	1	1	valid	valid	16-bit write
0	1	1	1	-	valid	8-bit write; data on low byte (even byte address[1])
1	0	1	1	valid	-	8-bit write; data on high byte (odd byte address[1])
1	1	0	0	valid	valid	16-bit read
1	1	0	1	-	valid	8-bit read; data on low byte (even byte address[1])
1	1	1	0	valid	-	8-bit read; data on high byte (odd byte address[1])

Table 6-8: Generic #1 Interface Truth Table for Big Endian

WE0#	WE1#	RD0#	RD1#	D[15:8]	D[7:0]	Comments
0	0	1	1	valid	valid	16-bit write
0	1	1	1	-	valid	8-bit write; data on low byte (odd byte address[1])
1	0	1	1	valid	-	8-bit write; data on high byte (even byte address[1])
1	1	0	0	valid	valid	16-bit read
1	1	0	1	-	valid	8-bit read; data on low byte (odd byte address[1])
1	1	1	0	valid	-	8-bit read; data on high byte (even byte address[1])

1. Because A0 is not used internally, all addresses are seen by the S1D13A04 as even addresses (16-bit word address aligned on even byte addresses).

6.3.2 Generic #2 Interface Timing (e.g. ISA)

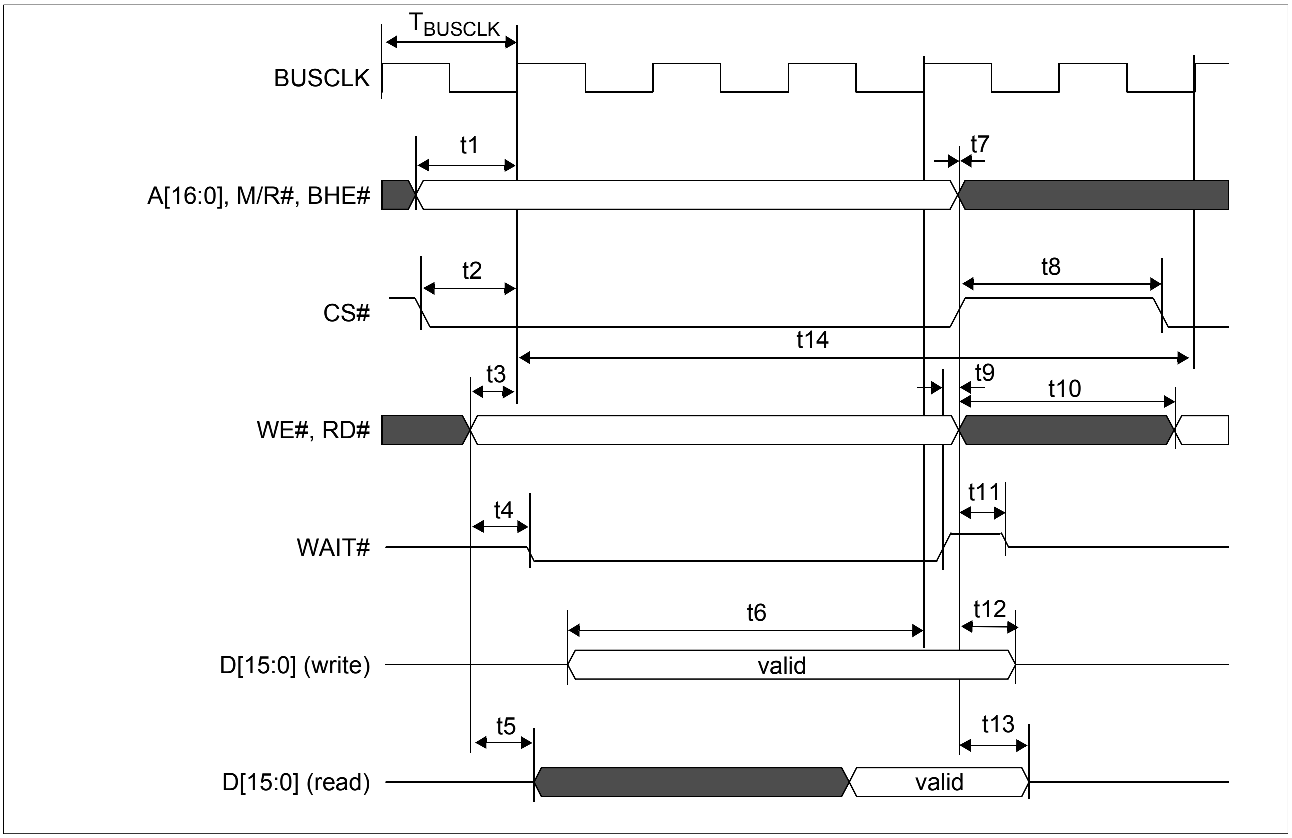


Figure 6-4: Generic #2 Interface Timing

Table 6-9: Generic #2 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{BUSCLK}	Bus clock frequency		50	MHz
T_{BUSCLK}	Bus clock period	$1/f_{BUSCLK}$		ns
t1	A[16:0], M/R#, BHE# setup to first BUSCLK rising edge where CS# = 0 and either RD# = 0 or WE# = 0	9		ns
t2	CS# setup to BUSCLK rising edge	9		ns
t3	RD#, WE# setup to BUSCLK rising edge	1		ns
t4	RD# or WE# state change to WAIT# driven low	1	10	ns
t5	RD# falling edge to D[15:0] driven (read cycle)	2	10	ns
t6	D[15:0] setup to 4th rising BUSCLK edge after CS#=0 and WE#=0	1		T_{BUSCLK}
t7	A[16:0], M/R#, BHE# and CS# hold from RD#, WE# rising edge	0		ns
t8	CS# deasserted to reasserted	0		ns
t9	WAIT# rising edge to RD#, WE# rising edge	0		ns
t10	WE#, RD# deasserted to reasserted	1		T_{BUSCLK}
t11	Rising edge of either RD# or WE# to WAIT# high impedance		0.5	T_{BUSCLK}
t12	D[15:0] hold from WE# rising edge (write cycle)	2		ns
t13	D[15:0] hold from RD# rising edge (read cycle)	1		ns
t14	Cycle Length	6		T_{BUSCLK}

Table 6-10: Generic #2 Interface Truth Table for Little Endian

WE#	RD#	BHE#	A0	D[15:8]	D[7:0]	Comments
0	1	0	0	valid	valid	16-bit write
0	1	1	0	-	valid	8-bit write at even address
0	1	0	1	valid	-	8-bit write at odd address
1	0	0	0	valid	valid	16-bit read
1	0	1	0	-	valid	8-bit read at even address
1	0	0	1	valid	-	8-bit read at odd address

Note

Generic #2 interface only supports Little Endian mode.

6.3.3 Hitachi SH-3 Interface Timing

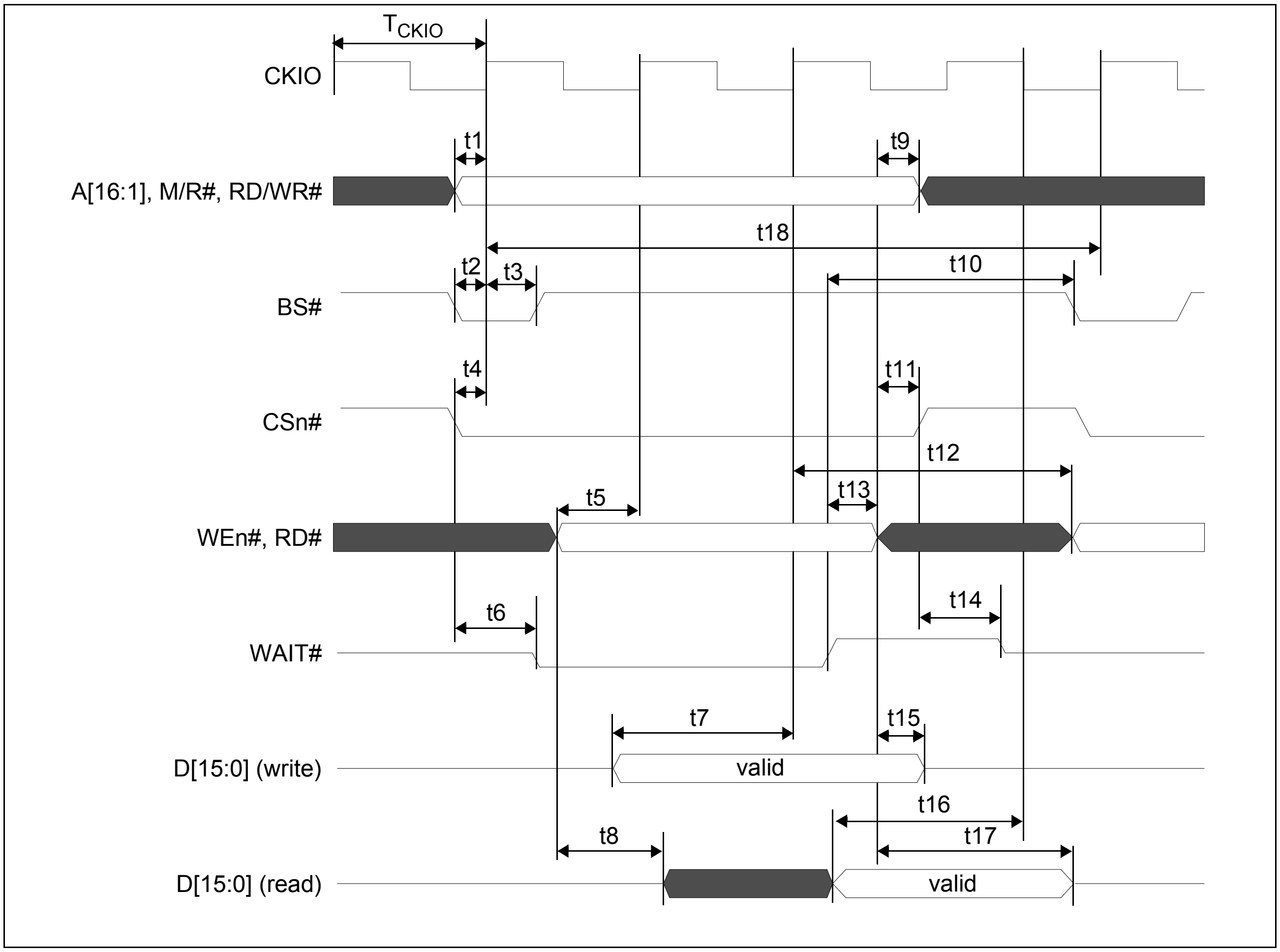


Figure 6-5: Hitachi SH-3 Interface Timing

Note

For this interface, the following formula must apply:

MCLK = BCLK ≤ 33MHz

If a BCLK greater than 33MHz is desired, MCLK must be divided such that MCLK is not greater than 33MHz (see REG[04h] bits 5-4).

Table 6-11: Hitachi SH-3 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{CKIO}	Bus clock frequency		66	MHz
T_{CKIO}	Bus clock period	$1/f_{CKIO}$		ns
t1	A[16:1], RD/WR# setup to CKIO	1		ns
t2	BS# setup	1		ns
t3	BS# hold	5		ns
t4	CSn# setup	1		ns
t5	WEn#, RD# setup to next CKIO after BS# low	0		ns
t6	Falling edge CSn# to WAIT# driven low	3	10	ns
t7	D[15:0] setup to 3rd CKIO rising edge after BS# deasserted (write cycle)	1		T_{CKIO}
t8	Falling edge of RD# to D[15:0] driven (read cycle)	2	12	ns
t9	WE#, RD# deasserted to A[16:1], M/R#, RD/WR# deasserted	0		ns
t10	Rising edge of WAIT# to BS# falling	T_{CKIO} + 16		ns
t11	WE#, RD# deasserted to CS# high	0		ns
t12	CKIO rising edge before WAIT# deasserted to WEn#, RD# asserted for next cycle	2		T_{CKIO}
t13	Rising edge of WAIT# to WE#, RD# deasserted	0		ns
t14	Rising edge of CSn# to WAIT# high impedance		0.5	T_{CKIO}
t15	D[15:0] hold from WEn# deasserted (write cycle)	2 (note 1)		ns
t16	D[15:0] setup to CKIO falling edge (read cycle)	12		ns
t17	Rising edge of RD# to D[15:0] high impedance (read cycle)	1	5	ns
t18	Cycle Length	4		T_{CKIO}

1. The S1D13A04 requires 2ns of write data hold time.

6.3.4 Hitachi SH-4 Interface Timing

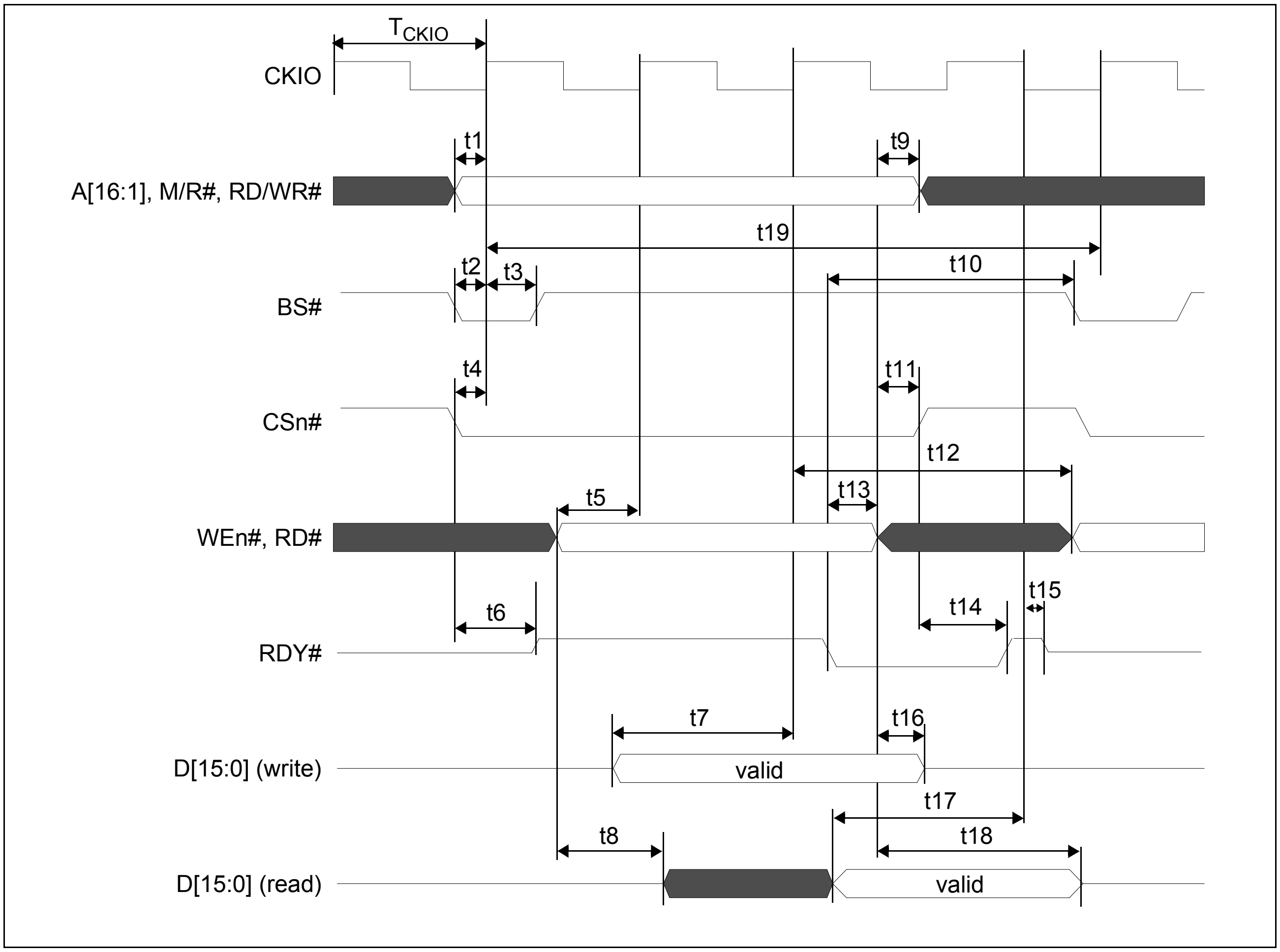


Figure 6-6: Hitachi SH-4 Interface Timing

Table 6-12: Hitachi SH-4 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{CKIO}	Bus clock frequency		66	MHz
T_{CKIO}	Bus clock period	$1/f_{CKIO}$		ns
t1	A[16:1], M/R#, RD/WR# setup to CKIO	1		ns
t2	BS# setup	1		ns
t3	BS# hold	5		ns
t4	CSn# setup	1		ns
t5	WEn#, RD# setup to 2nd CKIO rising edge after BS# low	0		ns
t6	Falling edge CSn# to RDY driven high	3	10	ns
t7	D[15:0] setup to 3rd CKIO rising edge after BS# deasserted (write cycle)	1		T_{CKIO}
t8	Falling edge RD# to D[15:0] driven (read cycle)	2	12	ns
t9	WE#,RD# deasserted to A[16:1],M/R#,RD/WR# deasserted	0		ns
t10	RDY falling edge to BS# falling	T_{CKIO} + 11		ns
t11	WE#,RD# deasserted to CS# high	0		ns
t12	CKIO rising edge before RDY deasserted to WEn#, RD# asserted for next cycle	2		T_{CKIO}
t13	RDY falling edge to WE#,RD# deasserted	0		ns
t14	Rising edge CSn# to RDY rising edge	3	10	ns
t15	CKIO falling edge to RDY tristate	3	9	ns
t16	D[15:0] hold from WEn# deasserted (write cycle)	3		ns
t17	D[15:0] setup to CKIO falling edge (read cycle)	12		ns
t18	Rising edge of RD# to D[15:0] high impedance (read cycle)	1	4	ns
t19	Cycle Length	4		T_{CKIO}

6.3.5 Motorola MC68K #1 Interface Timing (e.g. MC68000)

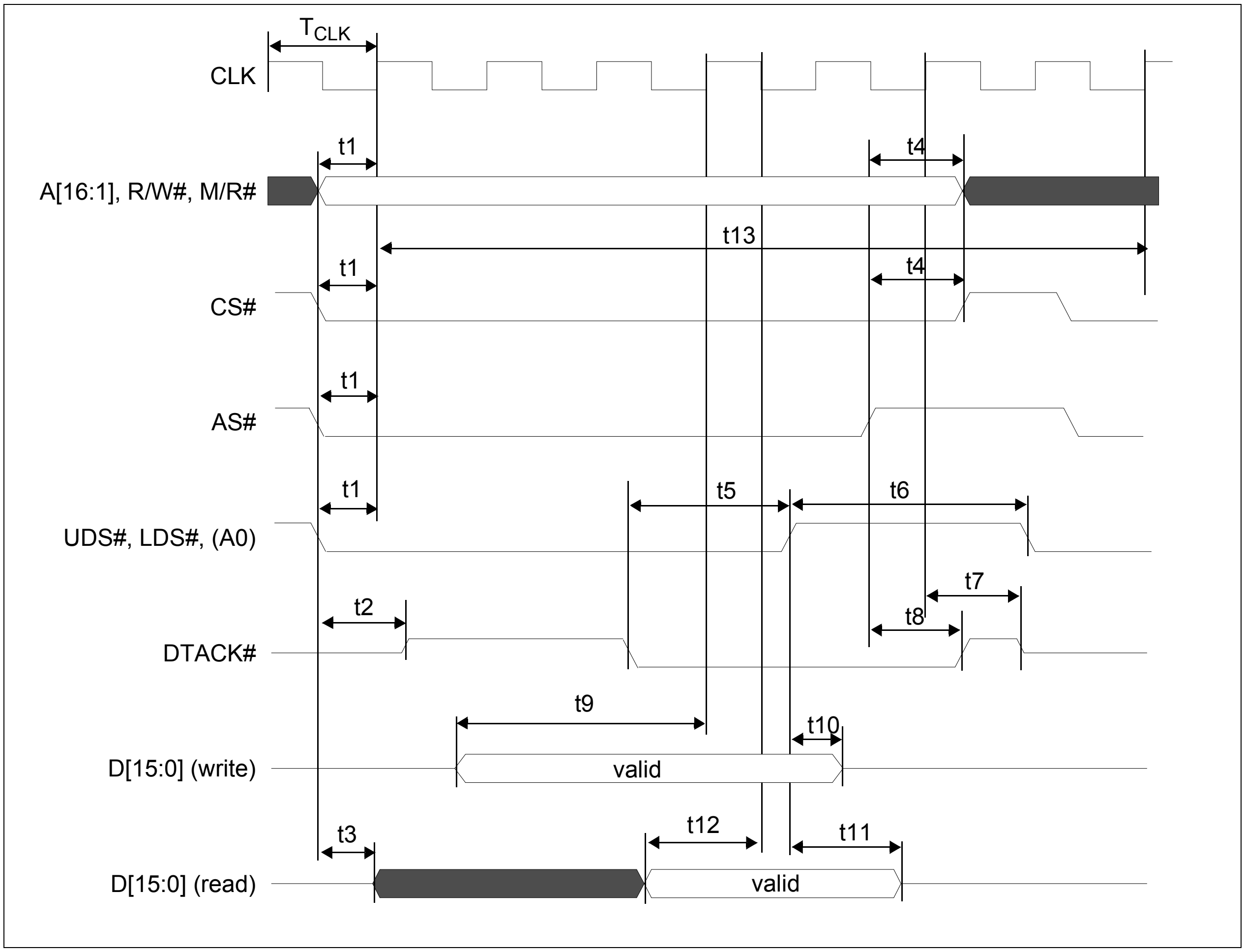


Figure 6-7: Motorola MC68K #1 Interface Timing

Table 6-13: Motorola MC68K#1 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{CLK}	Bus clock frequency		66	MHz
T_{CLK}	Bus clock period	$1/f_{CLK}$		ns
t1	A[16:1], M/R#, R/W# and CS# and AS# and UDS#, LDS# setup to first CLK rising edge	1		ns
t2	CS# and AS# asserted to DTACK# driven	3	10	ns
t3	UDS# = 0 or LDS# = 0 to D[15:0] driven (read cycle)		10	ns
t4	A[16:1], M/R#, R/W# and CS# hold from AS# rising edge	0		ns
t5	DTACK# falling edge to UDS#, LDS# rising edge	0		ns
t6	UDS#, LDS# deasserted high to reasserted low	1		T_{CLK}
t7	CLK rising edge to DTACK# high impedance		T_{CLK} - 2	ns
t8	AS# rising edge to DTACK# rising edge	3	11	ns
t9	D[15:0] valid to 4th CLK rising edge where CS# = 0, AS# = 0 and either UDS# = 0 or LDS# = 0 (write cycle)	1		T_{CLK}
t10	D[15:0] hold from UDS#, LDS# falling edge (write cycle)	4		ns
t11	UDS#, LDS# rising edge to D[15:0] high impedance (read cycle)	2		ns
t12	D[15:0] valid setup time to 2nd CLK falling edge after DTACK# goes low (read cycle)	10		ns
t13	Cycle Length	7		T_{CLK}

6.3.6 Motorola MC68K #2 Interface Timing (e.g. MC68030)

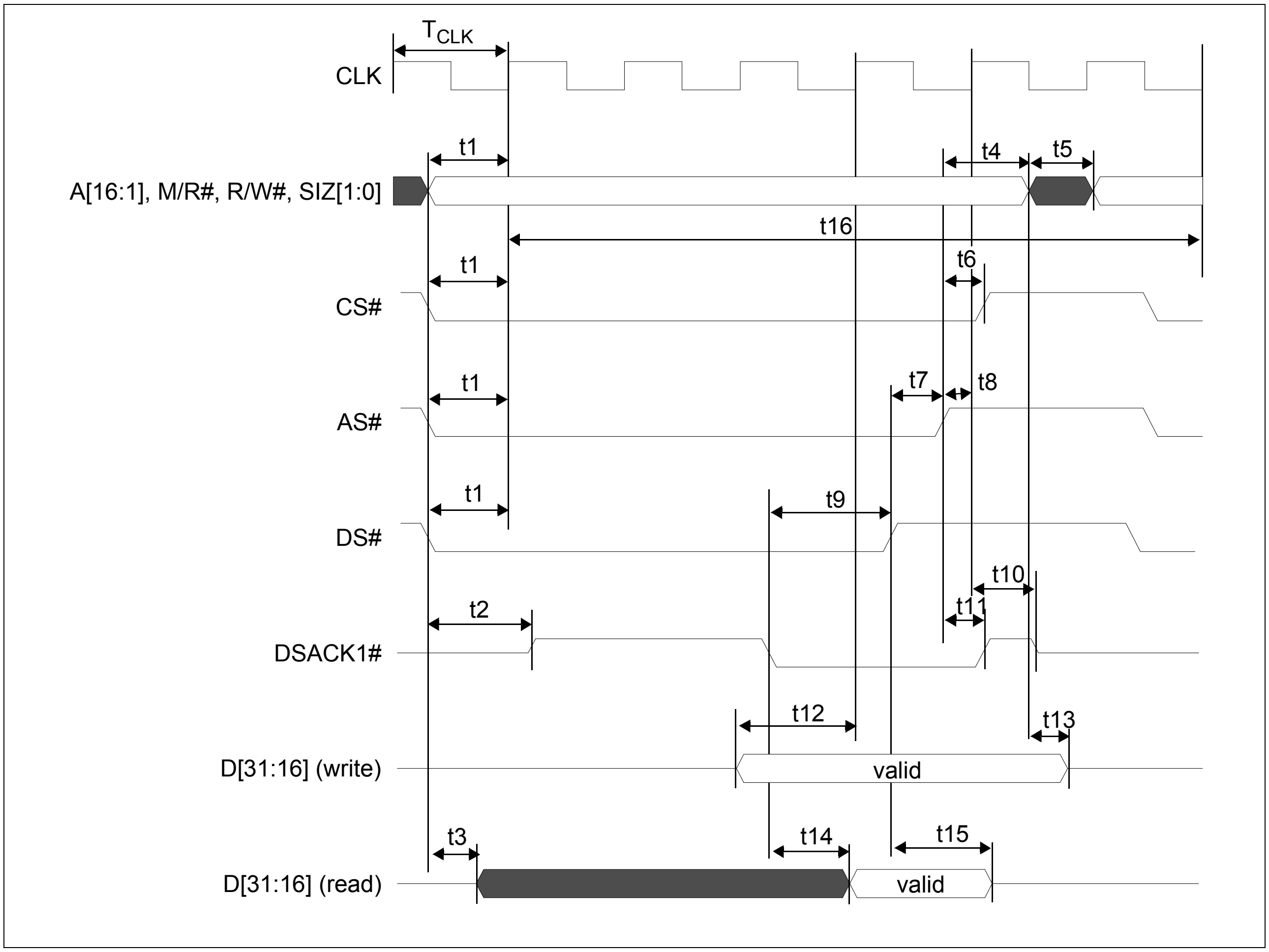


Figure 6-8: Motorola MC68K #2 Interface Timing

Table 6-14: Motorola MC68K#2 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{CLK}	Bus clock frequency		50	MHz
T_{CLK}	Bus clock period	$1/f_{CLK}$		ns
t1	A[16:0], M/R#, R/W#, SIZ[1:0] and CS# and AS# and DS# setup to first CLK rising edge	1		ns
t2	CS# and AS# asserted low to DSACK1# driven	3	10	ns
t3	A[1:0], R/W#, SIZ[1:0], DS# asserted to D[15:0] driven		8	ns
t4	A[16:1], M/R#, R/W#, SIZ[1:0] hold from AS# rising edge	0		ns
t5	R/W#, A[1:0], SIZ[1:0] deasserted to R/W#, A[1:0], SIZ[1:0] asserted for next cycle	1		T_{CLK}
t6	CS# hold from AS# rising edge	0		ns
t7	DS# rising edge to AS# rising edge	0		ns
t8	AS# setup to CLK rising edge	1		ns
t9	DSACK1# falling edge to DS# rising edge	0		ns
t10	CLK rising edge to DSACK1# high impedance		T_{CLK} - 2	ns
t11	AS# rising edge to DSACK1# rising edge	3	9	ns
t12	D[15:0] setup to 4th CLK rising edge after CS#=0, AS#=0, and UDS#=0 or LDS#=0	1		T_{CLK}
t13	D[15:0] hold from A[1:0], R/W#, SIZ[1:0] (write cycle)	1		ns
t14	DSACK1# falling edge to D[15:0] valid (read cycle)		3	ns
t15	DS# rising edge to D[15:0] high impedance (read cycle)	2	7	ns
t16	Cycle Length	6		T_{CLK}

6.3.7 Motorola REDCAP2 Interface Timing

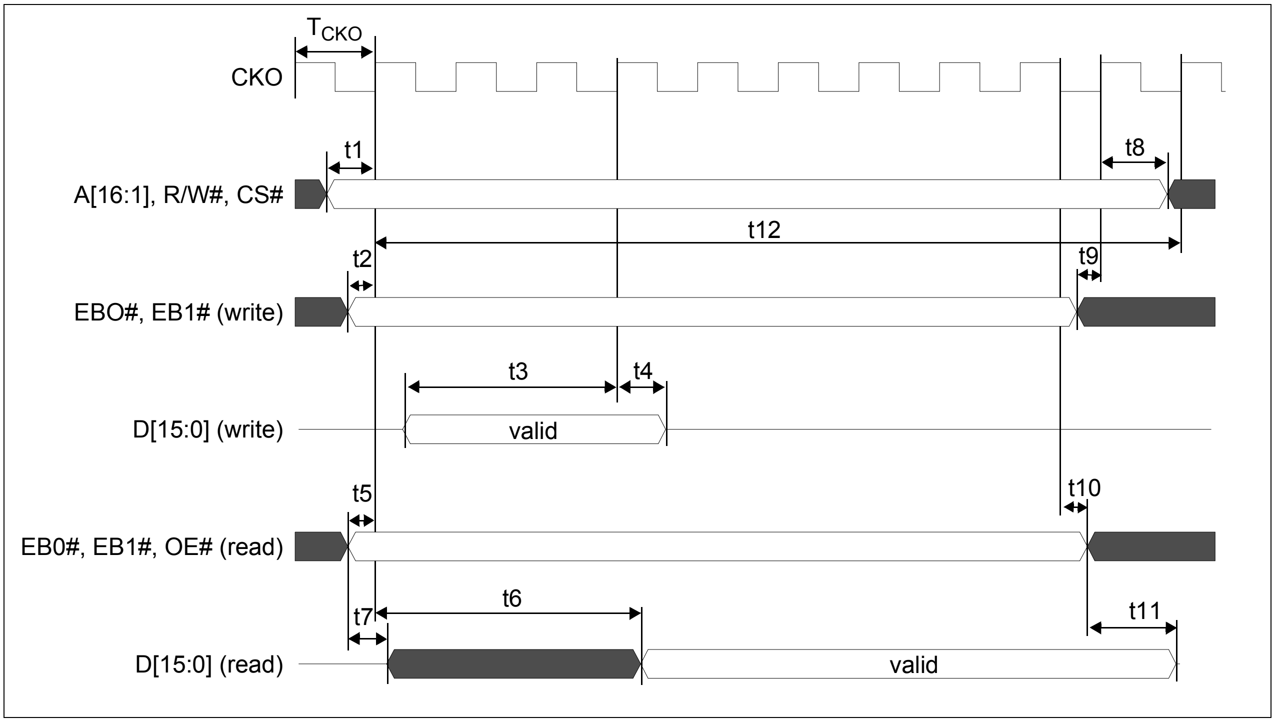


Figure 6-9: Motorola Redcap2 Interface Timing

Table 6-15: Motorola Redcap2 Interface Timing

Symbol	Parameter	Min	Max	Unit
f_{CKO}	Bus clock frequency		17	MHz
T_{CKO}	Bus clock period	$1/f_{CKO}$		ns
t1	A[16:1], R/W, CSn# setup to CKO rising edge	1		ns
t2	$\overline{EB0}$,$\overline{EB1}$ setup to CKO rising edge (write)	1		ns
t3	D[15:0] input setup to 4th CKO rising edge after CSn# and $\overline{EB0}$ or $\overline{EB1}$ asserted low (write cycle)	1		T_{CKO}
t4	D[15:0] input hold from 4th CKO rising edge after CSn# and $\overline{EB0}$ or $\overline{EB1}$ asserted low (write cycle)	11		ns
t5	$\overline{EB0}$,$\overline{EB1}$,$\overline{OE}$ setup to CKO rising edge (read cycle)	1		ns
t6a	1st CKO rising edge after CSn#, EB0 or EB1,OE asserted low to D[15:0] valid for MCLK = BCLK (read cycle)		5	T_{CKO}
t6b	1st CKO rising edge after CSn#, EB0 or EB1,OE asserted low to D[15:0] valid for MCLK = BCLK ÷ 2 (read cycle)		8	T_{CKO}
t6c	1st CKO rising edge after CSn#, EB0 or EB1,OE asserted low to D[15:0] valid for MCLK = BCLK ÷ 3 (read cycle)		10	T_{CKO}
t6d	1st CKO rising edge after CSn#, EB0 or EB1,OE asserted low to D[15:0] valid for MCLK = BCLK ÷ 4 (read cycle)		13	T_{CKO}
t7	$\overline{EB0}$,$\overline{EB1}$,$\overline{OE}$ falling edge to D[15:0] driven (read cycle)	4	11	ns
t8	A[16:1], R/W, CSn hold from CKO rising edge	0		ns
t9	EB0, EB1 setup to CKO rising edge (write cycle)	1		ns
t10	CKO falling edge to EB0, EB1, OE deasserted (read)	0		ns
t11	OE, EB0, EB1 deasserted to D[15:0] output high impedance (read)	1	7	ns
t12	Cycle Length (note 1)	10	10	T_{CKO}

1. The cycle length for the REDCAP interface is fixed.
2. The Read and Write 2D BitBLT functions are not available when using the REDCAP interface.

6.3.8 Motorola Dragonball Interface Timing with $\overline{\text{DTACK}}$ (e.g. MC68EZ328/MC68VZ328)

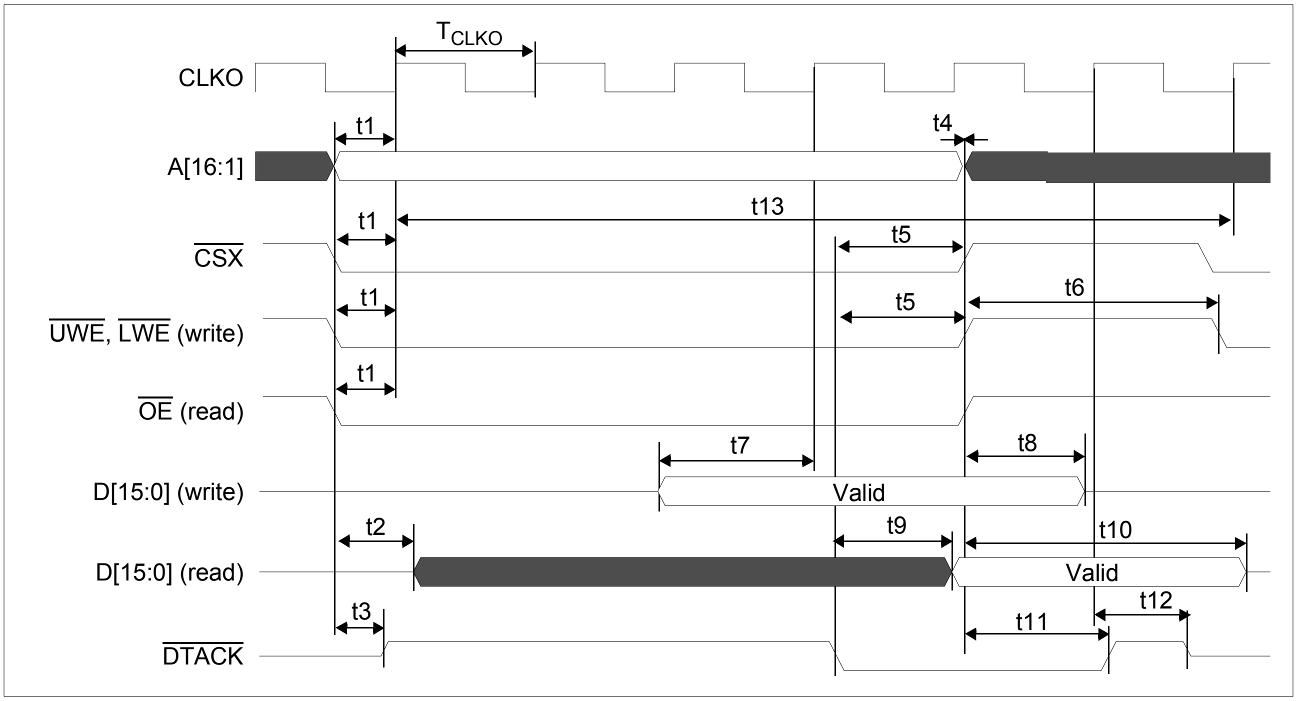


Figure 6-10: Motorola Dragonball Interface Timing with $\overline{\text{DTACK}}$

Table 6-16: Motorola Dragonball Interface Timing with $\overline{DTACK}$

Symbol	Parameter	Min	Max	Unit
f_{CLKO}	Clock frequency		33 (note 1)	MHz
T_{CLKO}	Clock period	$1/f_{CLKO}$		ns
t1	A[16:1], $\overline{CSX}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ setup to CLKO rising edge	1		ns
t2	$\overline{CSX}$ and $\overline{OE}$ asserted low to D[15:0] driven (read cycle)		11	ns
t3	$\overline{CSX}$ asserted low to $\overline{DTACK}$ driven		11	ns
t4	A[16:1] hold from $\overline{CSX}$ rising edge	0		ns
t5	$\overline{DTACK}$ falling edge to $\overline{UWE}$, $\overline{LWE}$ and $\overline{CSX}$ rising edge	0		ns
t6	$\overline{UWE}$, $\overline{LWE}$ deasserted to reasserted	2		T_{CLKO}
t7	D[15:0] valid to fourth CLKO rising edge where $\overline{CSX}$ = 0 and $\overline{UWE}$ = 0 or $\overline{LWE}$ = 0 (write cycle)	1		T_{CLKO}
t8	D[15:0] hold from UWE, LWE rising edge (write cycle)	2		ns
t9	$\overline{DTACK}$ falling edge to D[15:0] valid (read cycle)		T_{CLKO} + 4	ns
t10	$\overline{CSX}$ rising edge to D[15:0] high impedance (read cycle)	2	6	ns
t11	$\overline{CSX}$ rising edge to $\overline{DTACK}$ rising edge	3	9	ns
t12	CLKO rising edge to $\overline{DTACK}$ high impedance		9	ns
t13	Cycle Length	5		T_{CLKO}

1. The MC68VZ328 has a maximum clock frequency of 33MHz.
   The MC68EZ328 has a maximum clock frequency of 16MHz.

6.3.9 Motorola Dragonball Interface Timing w/o $\overline{\text{DTACK}}$ (e.g. MC68EZ328/MC68VZ328)

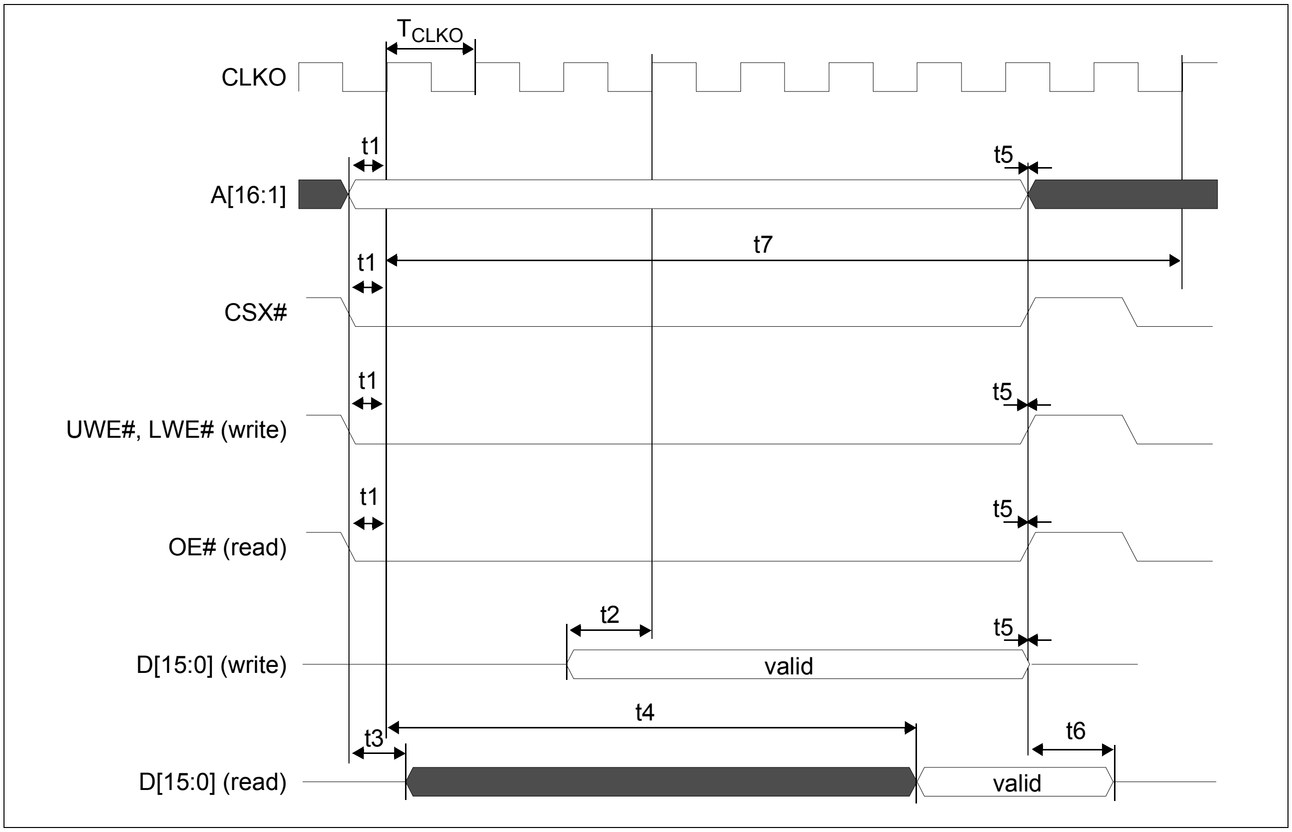


Figure 6-11: Motorola Dragonball Interface Timing w/o $\overline{\text{DTACK}}$

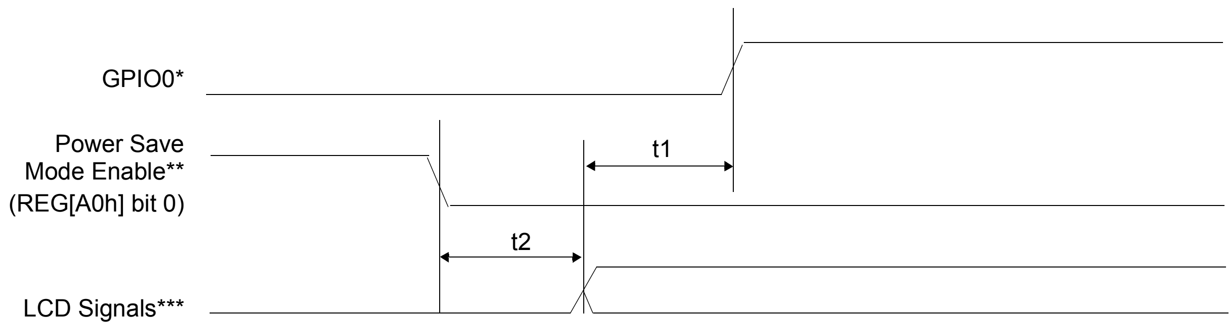
Table 6-17: Motorola Dragonball Interface Timing w/o $\overline{DTACK}$

Symbol	Parameter	Min	Max	Unit
f_{CLKO}	Bus clock frequency		33 (note 1)	MHz
T_{CLKO}	Bus clock period	$1/f_{CLKO}$		ns
t1	A[16:1] and CSX# and UWE#, LWE# and OE# setup to CLKO rising edge	1		ns
t2	D[15:0] valid to 4th CLK rising edge where CSX# = 0 and UWE# = 0 or LWE# = 0 (write cycle)	1		T_{CLKO}
t3	CSX# and OE# asserted low to D[15:0] driven (read cycle)		11	ns
t4a	1st CLKO rising edge after CSX# and OE# asserted to D[15:0] valid for MCLK=BCLK (read cycle)		5	T_{CLKO}
t4b	1st CLKO rising edge after CSX# and OE# asserted to D[15:0] valid for MCLK=BCLK ÷ 2 (read cycle)		8	T_{CLKO}
t4c	1st CLKO rising edge after CSX# and OE# asserted to D[15:0] valid for MCLK=BCLK ÷ 3 (read cycle) (see note 2)		10	T_{CLKO}
t4d	1st CLKO rising edge after CSX# and OE# asserted to D[15:0] valid for MCLK=BCLK ÷ 4 (read cycle) (see note 2)		13	T_{CLKO}
t5	A[16:1] and UWE#, LWE# and OE# and D[15:0] (write) hold from CSX# rising edge	0		ns
t6	CSX# rising edge to D[15:0] high impedance	2	6	ns
t7	Cycle Length	9	9	T_{CLKO}

1. The MC68VZ328 has a maximum clock frequency of 33MHz.
   The MC68EZ328 has a maximum clock frequency of 16MHz.
2. The MC68EZ328 does not support the MCLK = BCLK ÷ 3 and MCLK = BCLK ÷ 4 options.
3. The cycle length for the Dragonball w/o $\overline{DTACK}$ interface is fixed.
4. The Read and Write 2D BitBLT functions are not available when using the Dragonball w/o $\overline{DTACK}$ interface.

6.4 LCD Power Sequencing

6.4.1 Passive/TFT Power-On Sequence



*It is recommended to use the general purpose IO pin GPIO0 to control the LCD bias power.
**The LCD power-on sequence is activated by programming the Power Save Mode Enable bit (REG[14h] bit 4) to 0.
***LCD Signals include: FPDAT[17:0], FPSHIFT, FPLINE, FPFRAME, and DRDY.

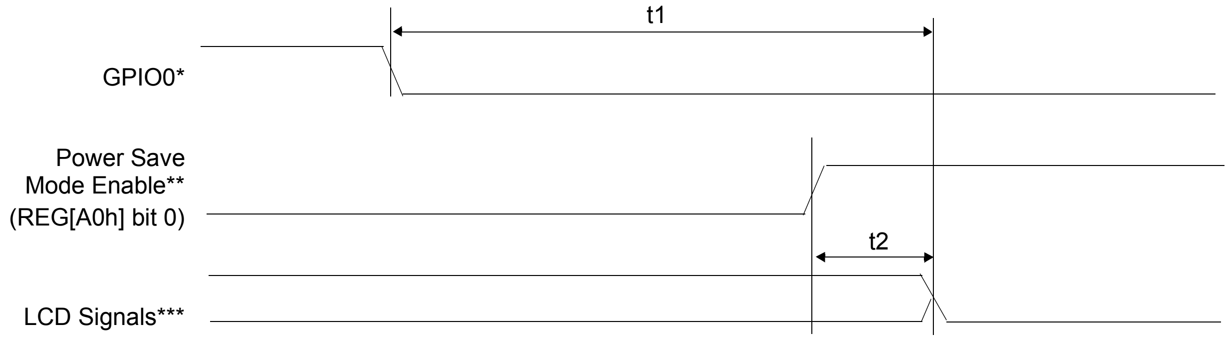
Figure 6-12: Passive/TFT Power-On Sequence Timing

Table 6-18: Passive/TFT Power-On Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	LCD signals active to LCD bias active	Note 1	Note 1	
t2	Power Save Mode disabled to LCD signals active	0	1	BCLK

1. t1 is controlled by software and must be determined from the bias power supply delay requirements of the panel connected.

6.4.2 Passive/TFT Power-Off Sequence



*It is recommended to use the general purpose IO pin GPIO0 to control the LCD bias power.
**The LCD power-off sequence is activated by programming the Power Save Mode Enable bit (REG[14h] bit 4) to 1.
***LCD Signals include: FPDAT[17:0], FPSHIFT, FPLINE, FPFRAME, and DRDY.

Figure 6-13: Passive/TFT Power-Off Sequence Timing

Table 6-19: Passive/TFT Power-Off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	LCD bias deactivated to LCD signals inactive	Note 1	Note 1	
t2	Power Save Mode enabled to LCD signals low	0	1	BCLK

1. t1 is controlled by software and must be determined from the bias power supply delay requirements of the panel connected.

6.4.3 ‘Direct’ HR-TFT Interface Power-On/Off Sequence

For ‘Direct’ HR-TFT Interface Power-On/Off sequence information, see *Connecting to the Sharp HR-TFT Panels*, document number X37A-G-011-xx.

6.5 Display Interface

The timing parameters required to drive a flat panel display are shown below. Timing details for each supported panel type are provided in the remainder of this section.

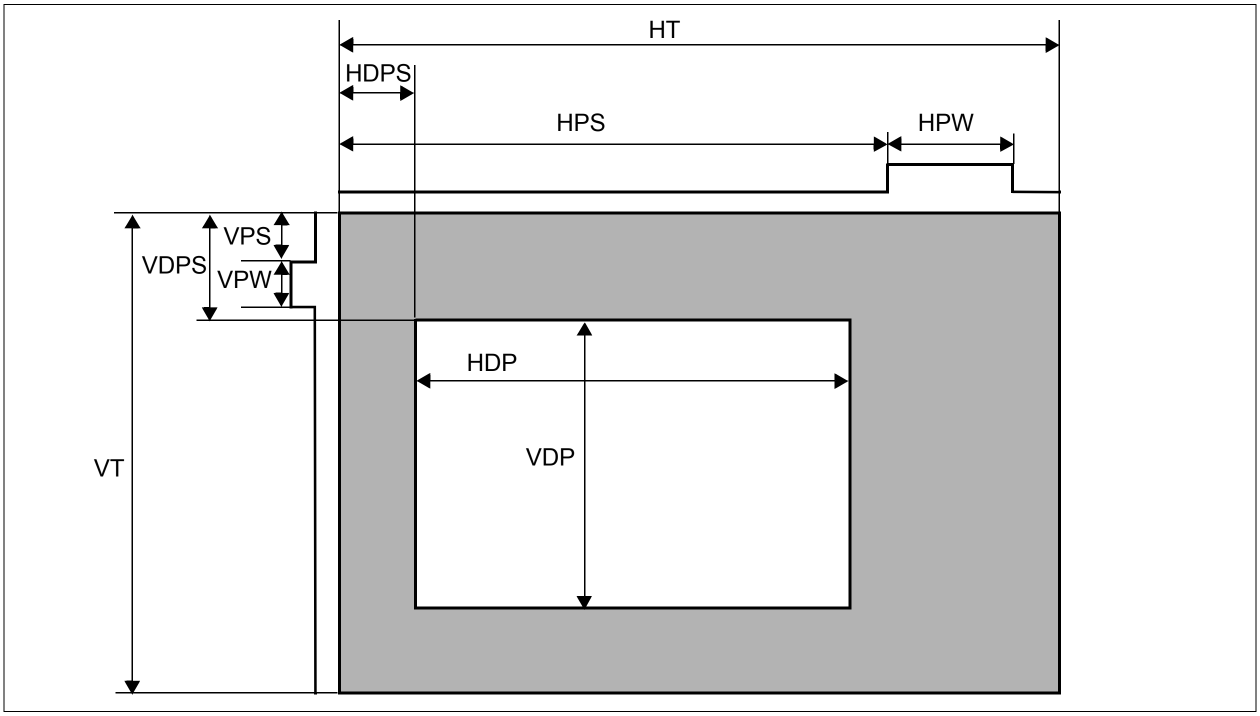


Figure 6-14: Panel Timing Parameters

Table 6-20: Panel Timing Parameter Definition and Register Summary

Symbol	Description	Derived From	Units
HT	Horizontal Total	((REG[20h] bits 6-0) + 1) x 8	
HDP[1]	Horizontal Display Period[1]	((REG[24h] bits 6-0) + 1) x 8	
HDPS	Horizontal Display Period Start Position	For STN panels: ((REG[28h] bits 9-0) + *22*)	Ts
		For TFT panels: ((REG[28h] bits 9-0) + *5*)	
HPS	FPLINE Pulse Start Position	(REG[2Ch] bits 9-0) + 1	
HPW	FPLINE Pulse Width	(REG[2Ch] bits 22-16) + 1	
VT	Vertical Total	(REG[30h] bits 9-0) + 1	
VDP	Vertical Display Period	(REG[34h] bits 9-0) + 1	
VDPS	Vertical Display Period Start Position	REG[38h] bits 9-0	Lines (HT)
VPS	FPFRAME Pulse Start Position	REG[2Ch] bits 9-0	
VPW	FPFRAME Pulse Width	(REG[3Ch] bits 18-16) + 1	

1. For passive panels, the HDP must be a minimum of 32 pixels and must be increased by multiples of 16.
   For TFT panels, the HDP must be a minimum of 8 pixels and must be increased by multiples of 8.
2. The following formulas must be valid for all panel timings:
   HDPS + HDP < HT
   VDPS + VDP < VT

6.5.1 Generic STN Panel Timing

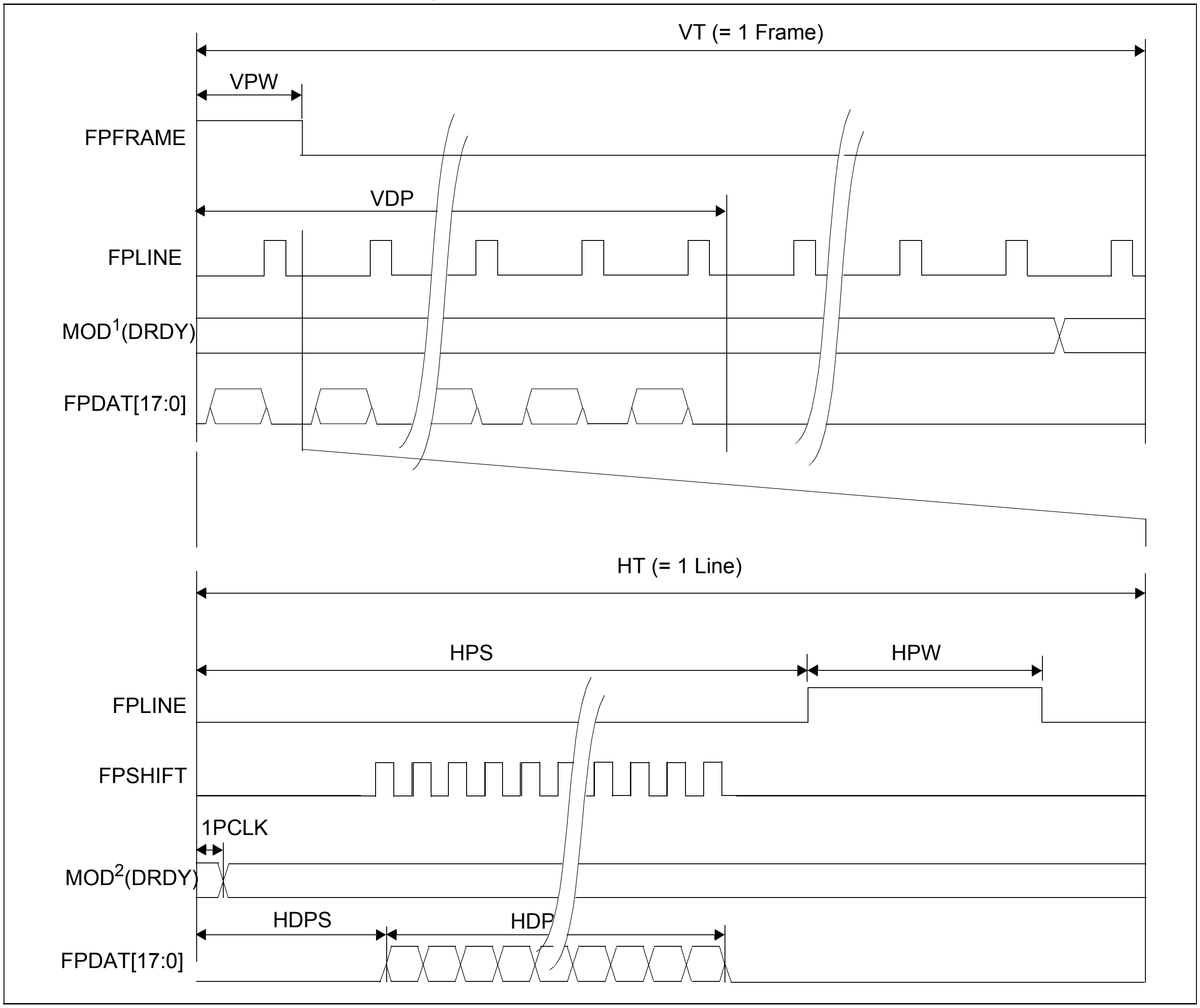


Figure 6-15: Generic STN Panel Timing

VT	= Vertical Total	= [(REG[30h] bits 9-0) + 1] lines
VPS	= FPFRAME Pulse Start Position	= 0 lines, because REG[2Ch] bits 9-0 = 0
VPW	= FPFRAME Pulse Width	= [(REG[3Ch] bits 18-16) + 1] lines
VDPS	= Vertical Display Period Start Position	= 0 lines, because REG[38h] bits 9-0 = 0
VDP	= Vertical Display Period	= [(REG[34h] bits 9-0) + 1] lines
HT	= Horizontal Total	= [((REG[20h] bits 6-0) + 1) x 8] pixels
HPS	= FPLINE Pulse Start Position	= [(REG[2Ch] bits 9-0) + 1] pixels
HPW	= FPLINE Pulse Width	= [(REG[2Ch] bits 22-16) + 1] pixels
HDPS	= Horizontal Display Period Start Position	= 22 pixels, because REG[28h] bits 9-0 = 0
HDP	= Horizontal Display Period	= [((REG[24h] bits 6-0) + 1) x 8] pixels

*For passive panels, the HDP must be a minimum of 32 pixels and must be increased by multiples of 16.

*HPS must comply with the following formula:

HPS > HDP + 22

HPS + HPW < HT

*Panel Type Bits (REG[0Ch] bits 1-0) = 00b (STN)

*FPFRAME Pulse Polarity Bit (REG[3Ch] bit 23) = 1 (active high)

*FPLINE Polarity Bit (REG[2Ch] bit 23) = 1 (active high)

*MOD^{1} is the MOD signal when REG[0Ch] bits 21-16 = 0 (MOD toggles every FPFRAME)

*MOD^{2} is the MOD signal when REG[0Ch] bits 21-16 = n (MOD toggles every n FPLINE)

6.5.2 Single Monochrome 4-Bit Panel Timing

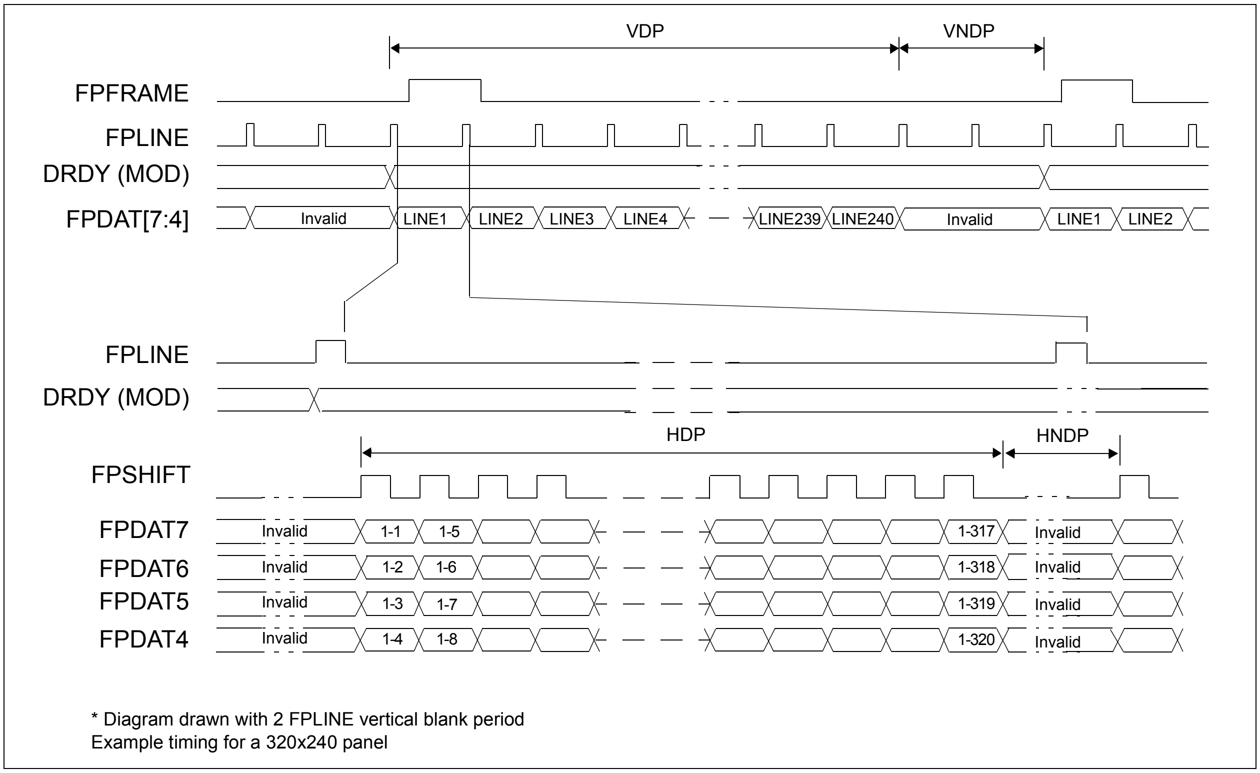


Figure 6-16: Single Monochrome 4-Bit Panel Timing

VDP = Vertical Display Period
= (REG[34h] bits 9:0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[30h] bits 9:0) - (REG[34h] bits 9:0) Lines

HDP = Horizontal Display Period
= ((REG[24h] bits 6:0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[20h] bits 6:0) + 1) x 8Ts) - (((REG[24h] bits 6:0) + 1) x 8Ts)

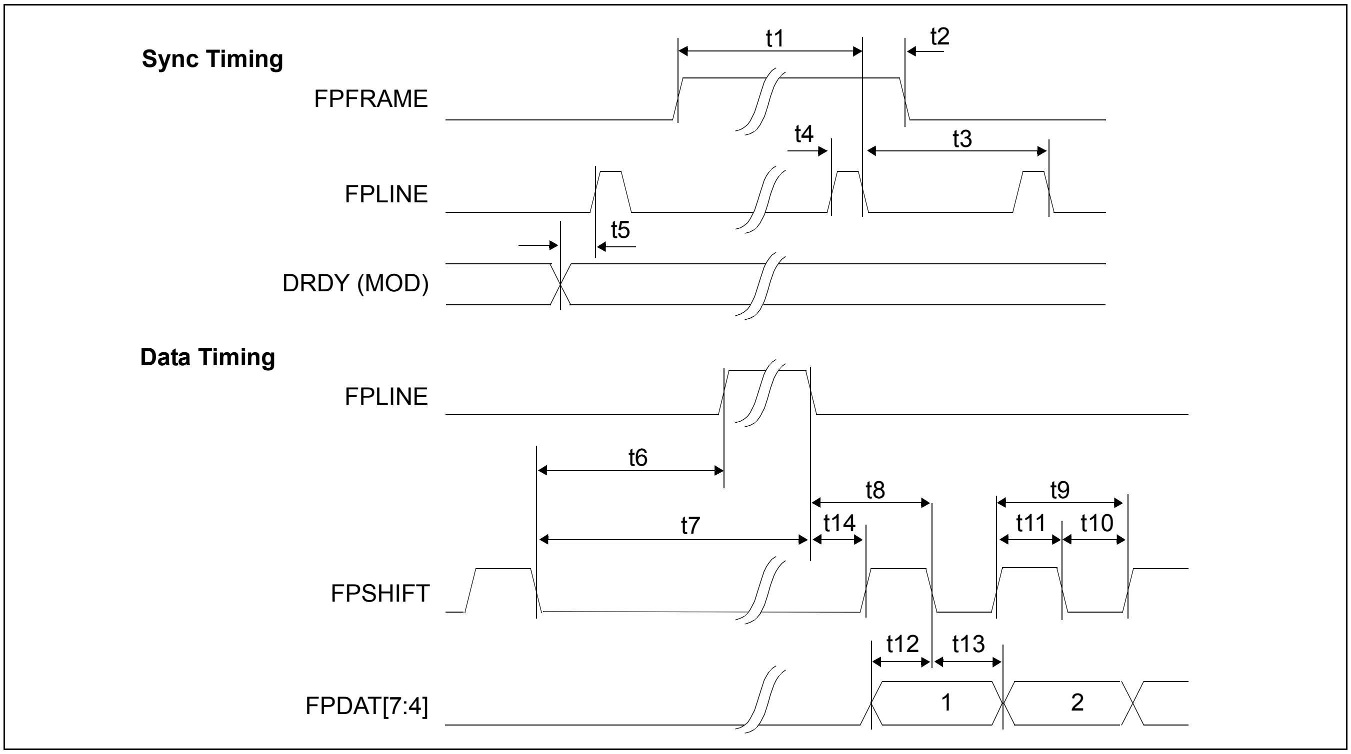


Figure 6-17: Single Monochrome 4-Bit Panel A.C. Timing

Table 6-21: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			Ts
t9	FPSHIFT period	4			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	FPDAT[7:4] setup to FPSHIFT falling edge	1			Ts
t13	FPDAT[7:4] hold to FPSHIFT falling edge	2			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 2, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.5.3 Single Monochrome 8-Bit Panel Timing

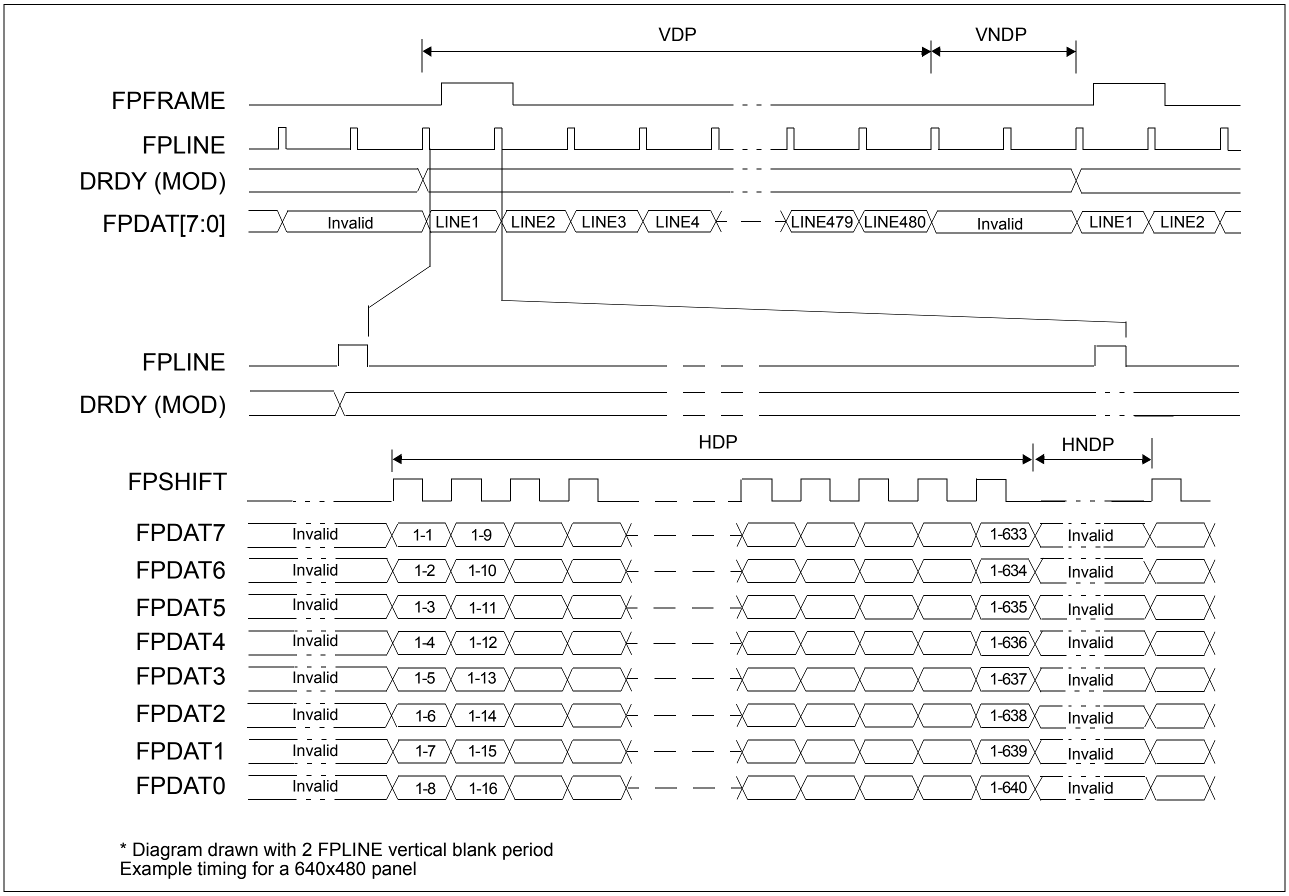


Figure 6-18: Single Monochrome 8-Bit Panel Timing

VDP = Vertical Display Period
= (REG[34h] bits 9:0) + 1 Lines
VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[30h] bits 9:0) - (REG[34h] bits 9:0) Lines
HDP = Horizontal Display Period
= ((REG[24h] bits 6:0) + 1) x 8Ts
HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[20h] bits 6:0) + 1) x 8Ts) - (((REG[24h] bits 6:0) + 1) x 8Ts)

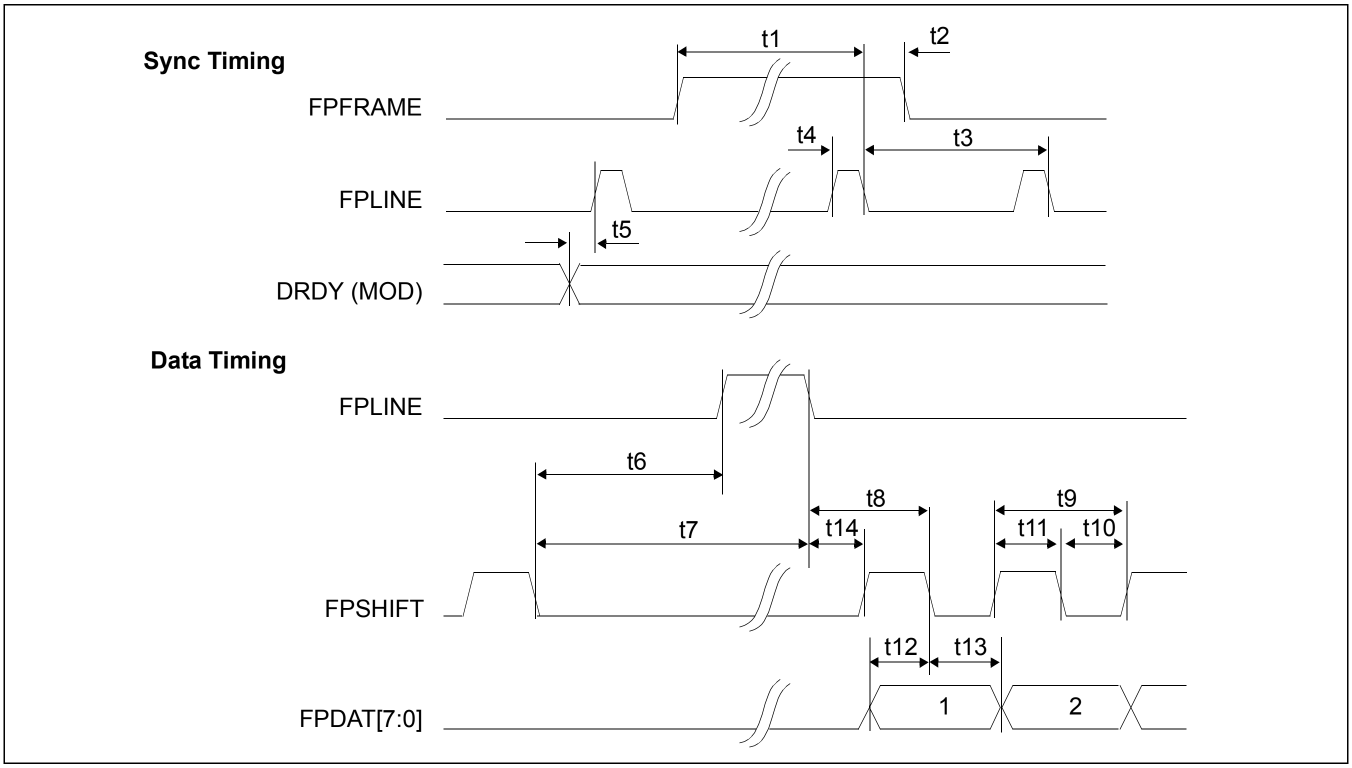


Figure 6-19: Single Monochrome 8-Bit Panel A.C. Timing

Table 6-22: Single Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 4			Ts
t9	FPSHIFT period	8			Ts
t10	FPSHIFT pulse width low	4			Ts
t11	FPSHIFT pulse width high	4			Ts
t12	FPDAT[7:0] setup to FPSHIFT falling edge	4			Ts
t13	FPDAT[7:0] hold to FPSHIFT falling edge	4			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 4, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.5.4 Single Color 4-Bit Panel Timing

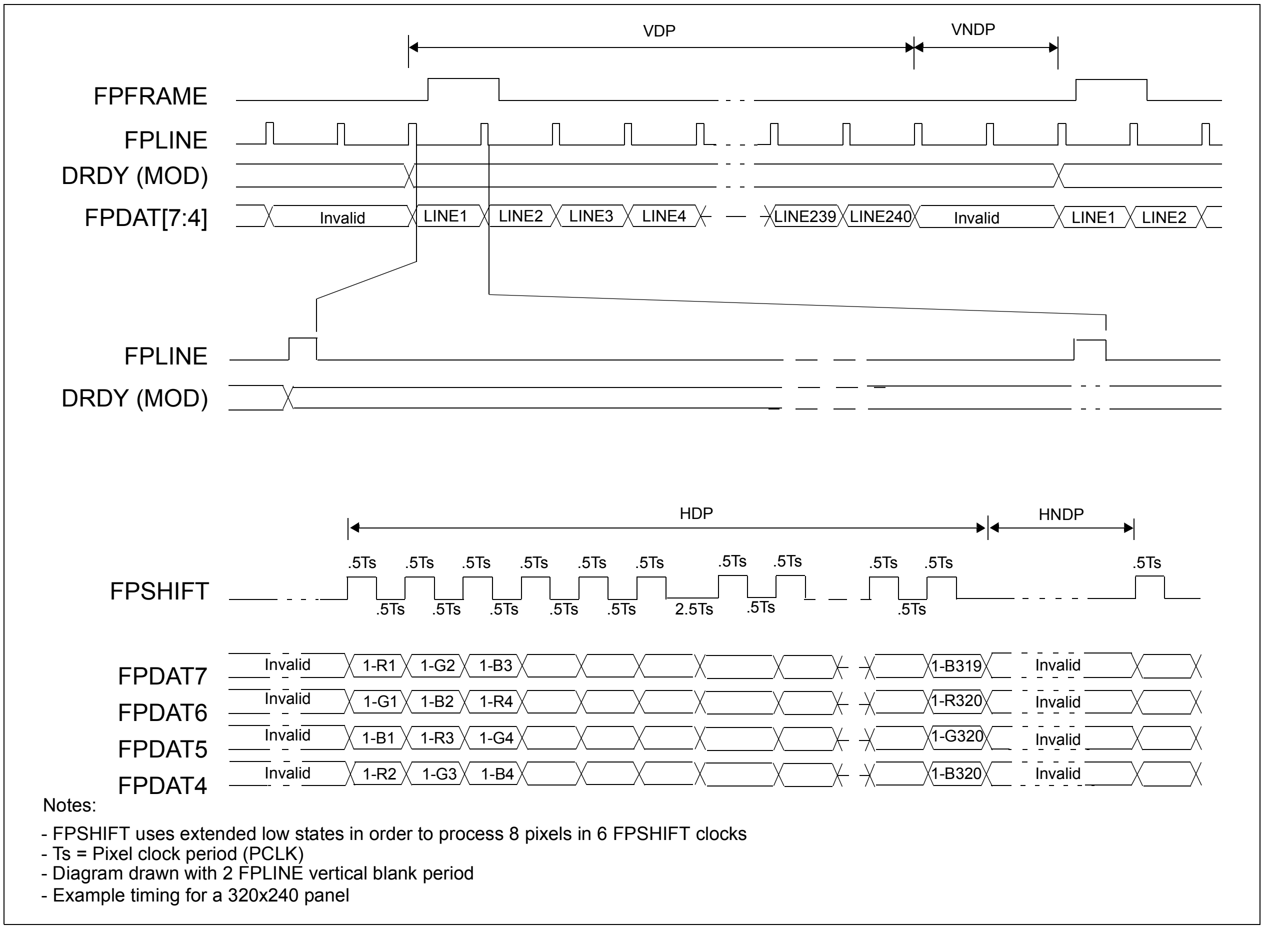


Figure 6-20: Single Color 4-Bit Panel Timing

VDP = Vertical Display Period
= (REG[34h] bits 9:0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[30h] bits 9:0) - (REG[34h] bits 9:0) Lines

HDP = Horizontal Display Period
= ((REG[24h] bits 6:0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[20h] bits 6:0) + 1) x 8Ts) - (((REG[24h] bits 6:0) + 1) x 8Ts)

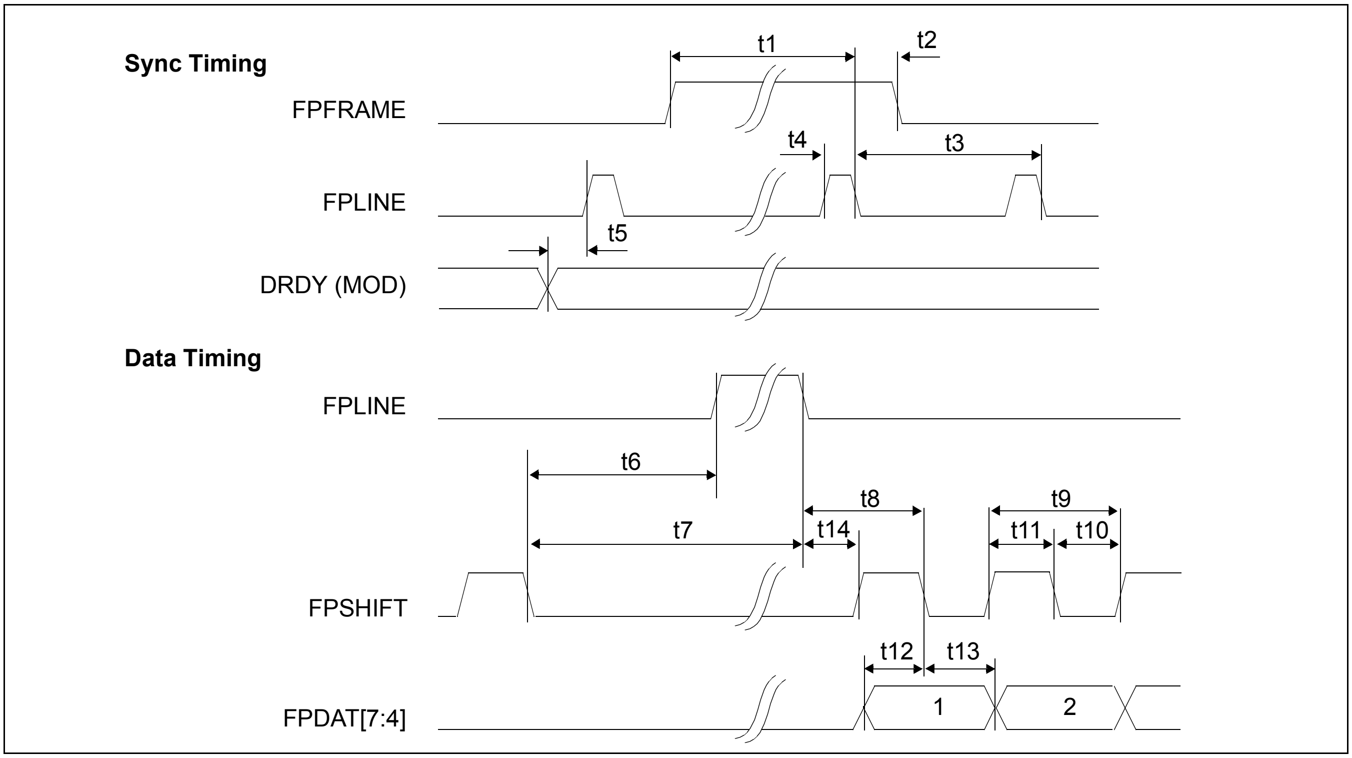


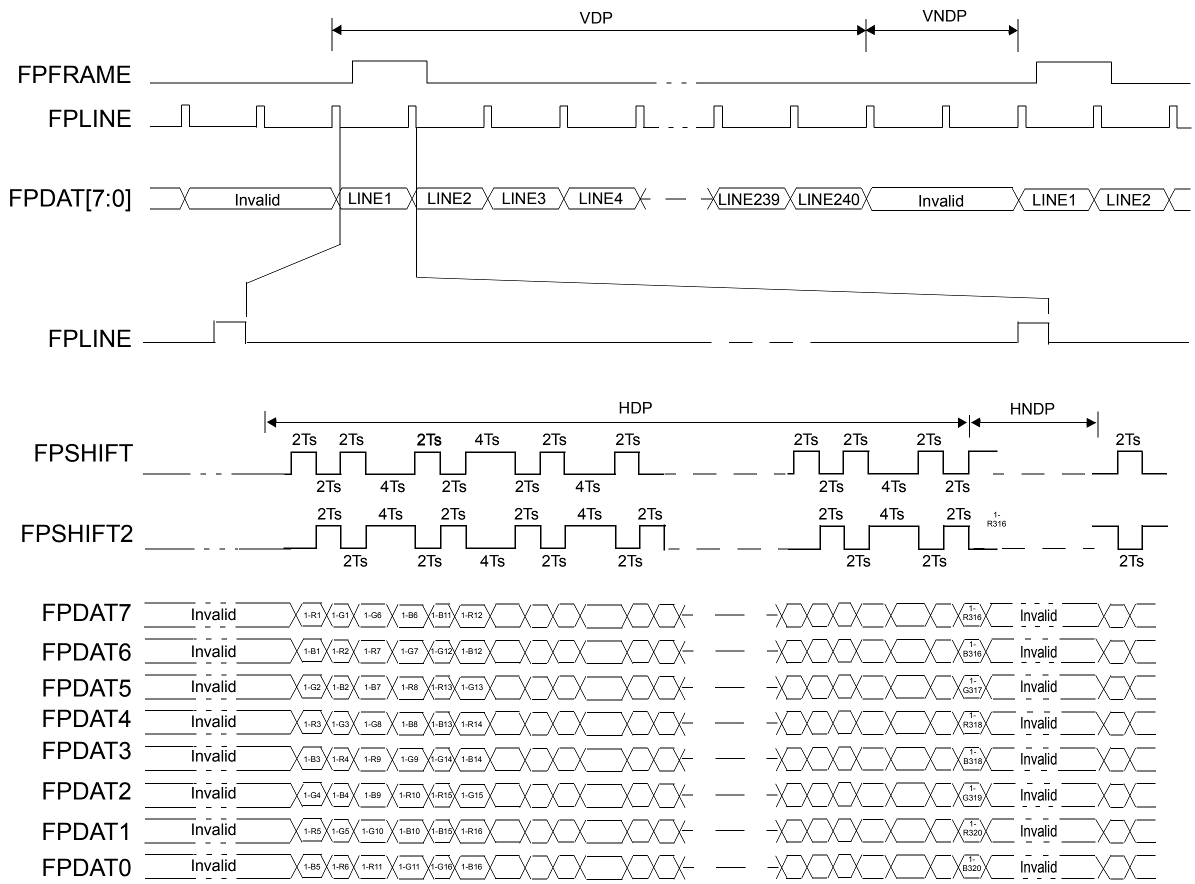
Figure 6-21: Single Color 4-Bit Panel A.C. Timing

Table 6-23: Single Color 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 0.5			Ts
t9	FPSHIFT period	1			Ts
t10	FPSHIFT pulse width low	0.5			Ts
t11	FPSHIFT pulse width high	0.5			Ts
t12	FPDAT[7:4] setup to FPSHIFT falling edge	0.5			Ts
t13	FPDAT[7:4] hold to FPSHIFT falling edge	0.5			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 1.5), if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$) + 1, if negative add $t3_{min}$

6.5.5 Single Color 8-Bit Panel Timing (Format 1)



Notes:

- The duty cycle of FPSHIFT changes in order to process 16 pixels in 6 FPSHIFT/FPSHIFT2 rising edges
- Ts = Pixel clock period (PCLK)
- Diagram drawn with 2 FPLINE vertical blank period
- Example timing for a 320x240 panel

Figure 6-22: Single Color 8-Bit Panel Timing (Format 1)

VDP = Vertical Display Period
= (REG[34h] bits 9:0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[30h] bits 9:0) - (REG[34h] bits 9:0) Lines

HDP = Horizontal Display Period
= ((REG[24h] bits 6:0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[20h] bits 6:0) + 1) x 8Ts) - (((REG[24h] bits 6:0) + 1) x 8Ts)

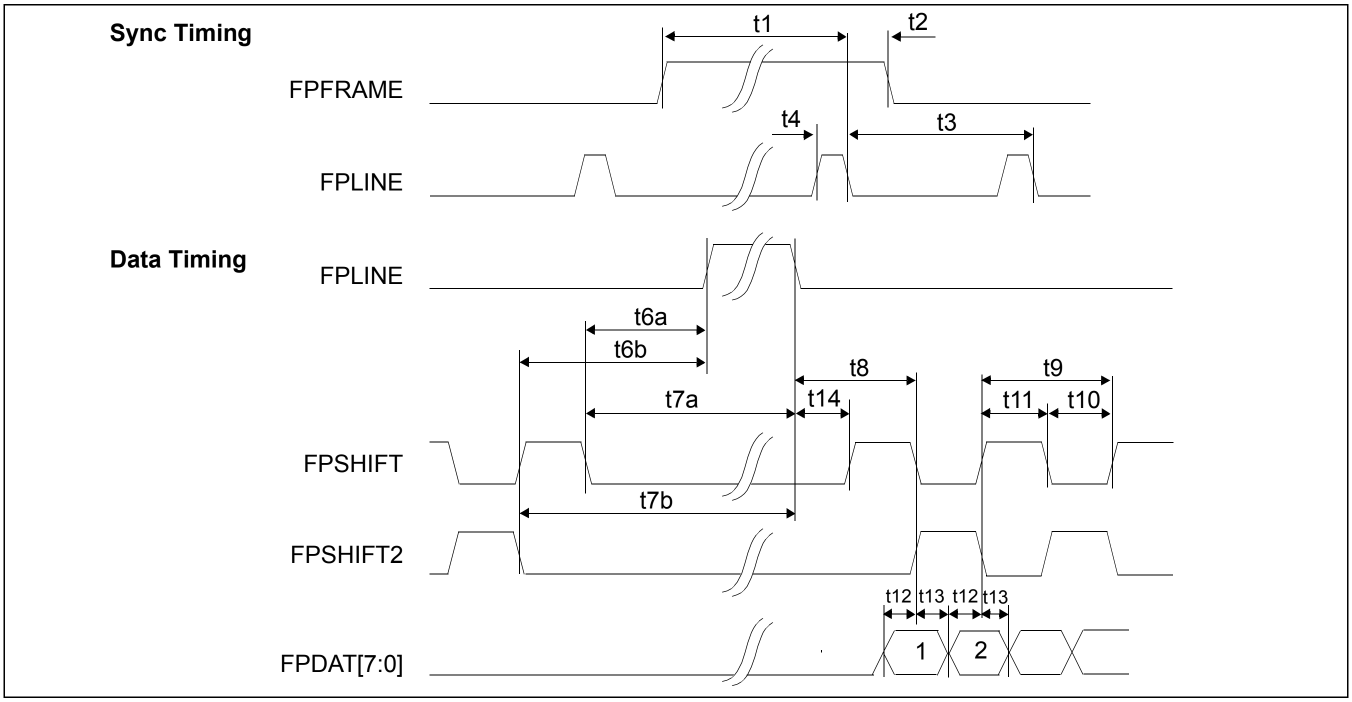


Figure 6-23: Single Color 8-Bit Panel A.C. Timing (Format 1)

Table 6-24: Single Color 8-Bit Panel A.C. Timing (Format 1)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t6a	FPSHIFT falling edge to FPLINE rising edge	note 6			Ts
t6b	FPSHIFT2 falling edge to FPLINE rising edge	note 7			Ts
t7a	FPSHIFT falling edge to FPLINE falling edge	t6a + t4			Ts
t7b	FPSHIFT2 falling edge to FPLINE falling edge	t6b + t4			Ts
t8	FPLINE falling edge to FPSHIFT rising, FPSHIFT2 falling edge	t14 + 2			Ts
t9	FPSHIFT2, FPSHIFT period	4		6	Ts
t10	FPSHIFT2, FPSHIFT pulse width low	2			Ts
t11	FPSHIFT2, FPSHIFT pulse width high	2			Ts
t12	FPDAT[7:0] setup to FPSHIFT2, FPSHIFT falling edge	1			Ts
t13	FPDAT[7:0] hold from FPSHIFT2, FPSHIFT falling edge	1			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t6a_{min}$ = HPS - (HDP + HDPS), if negative add $t3_{min}$
7. $t6b_{min}$ = HPS - (HDP + HDPS) + 2, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.5.6 Single Color 8-Bit Panel Timing (Format 2)

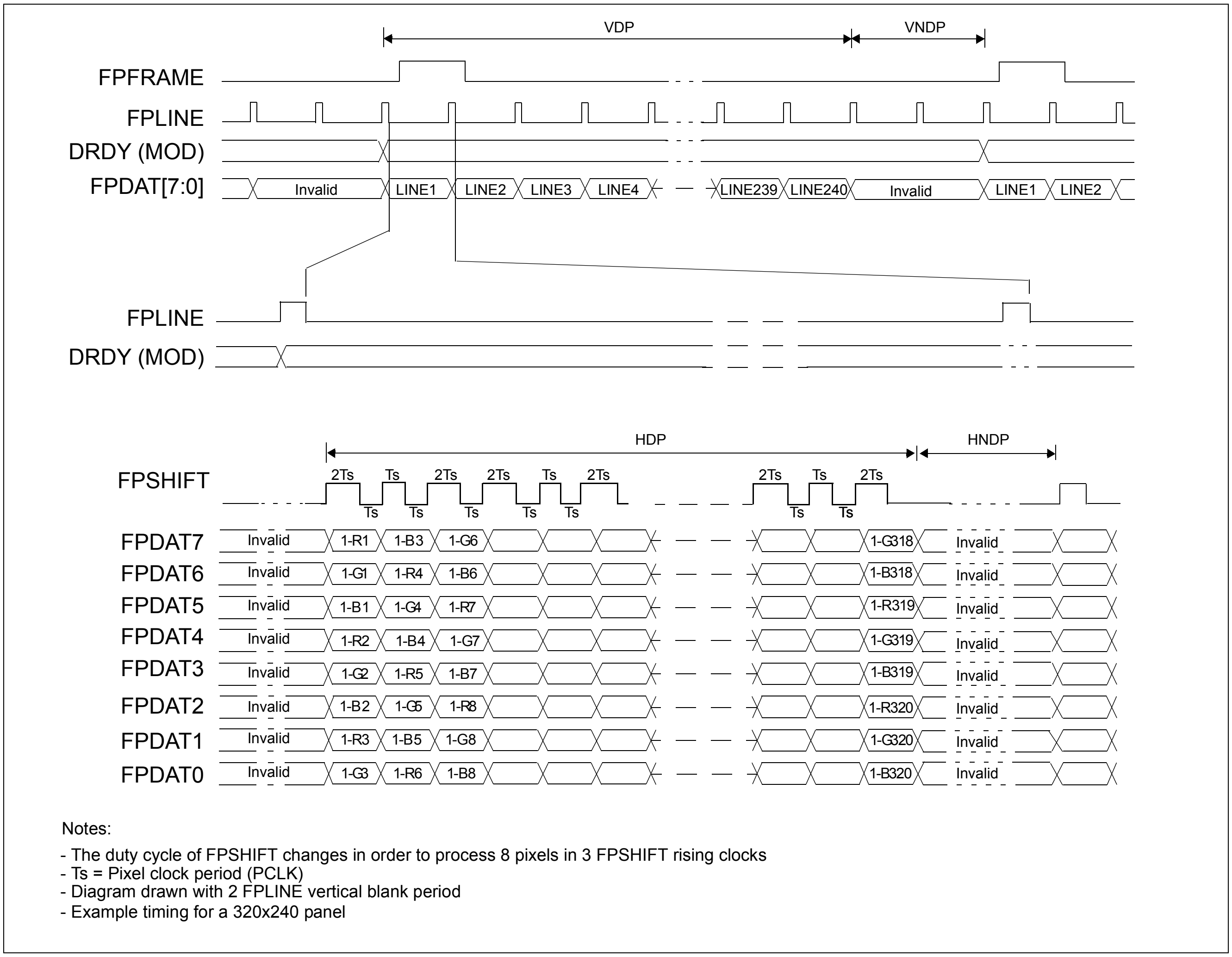


Figure 6-24: Single Color 8-Bit Panel Timing (Format 2)

VDP = Vertical Display Period
= (REG[34h] bits 9:0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[30h] bits 9:0) - (REG[34h] bits 9:0) Lines

HDP = Horizontal Display Period
= ((REG[24h] bits 6:0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[20h] bits 6:0) + 1) x 8Ts) - (((REG[24h] bits 6:0) + 1) x 8Ts)

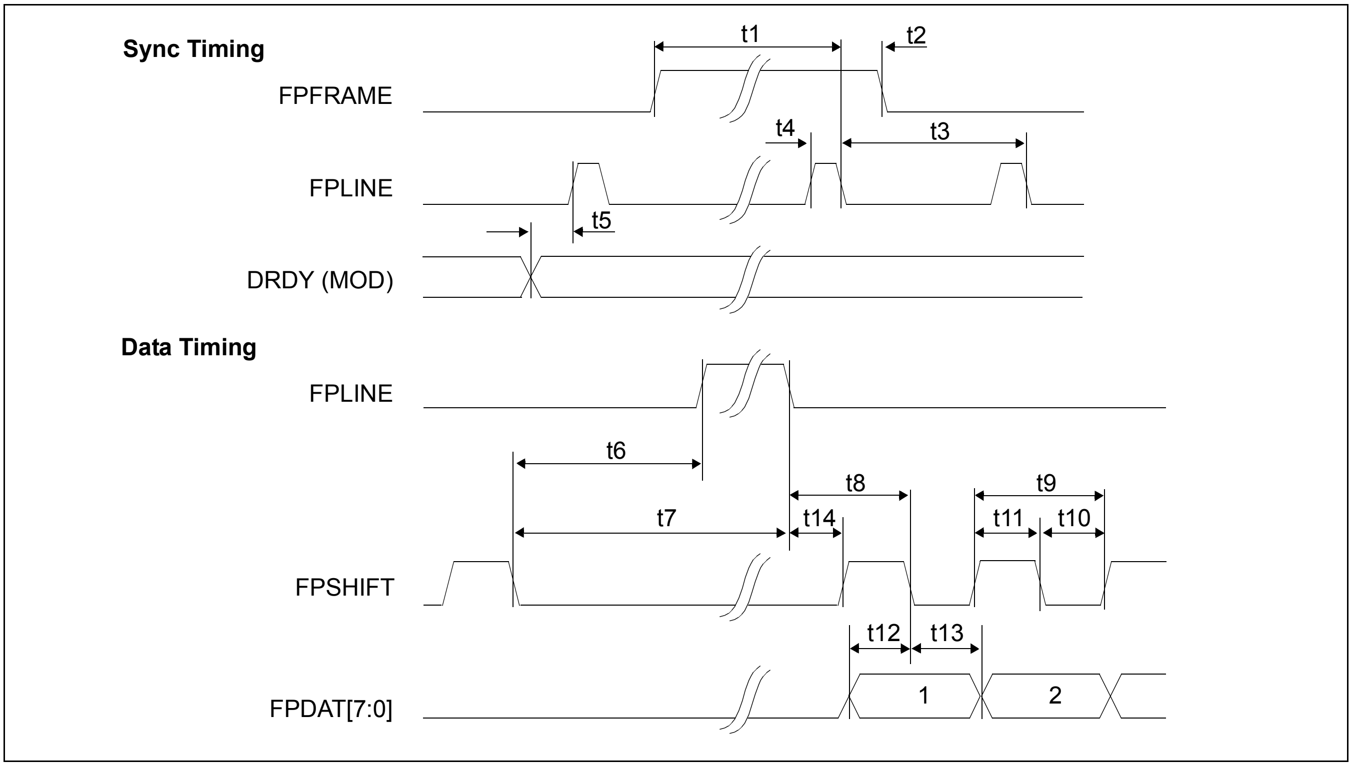


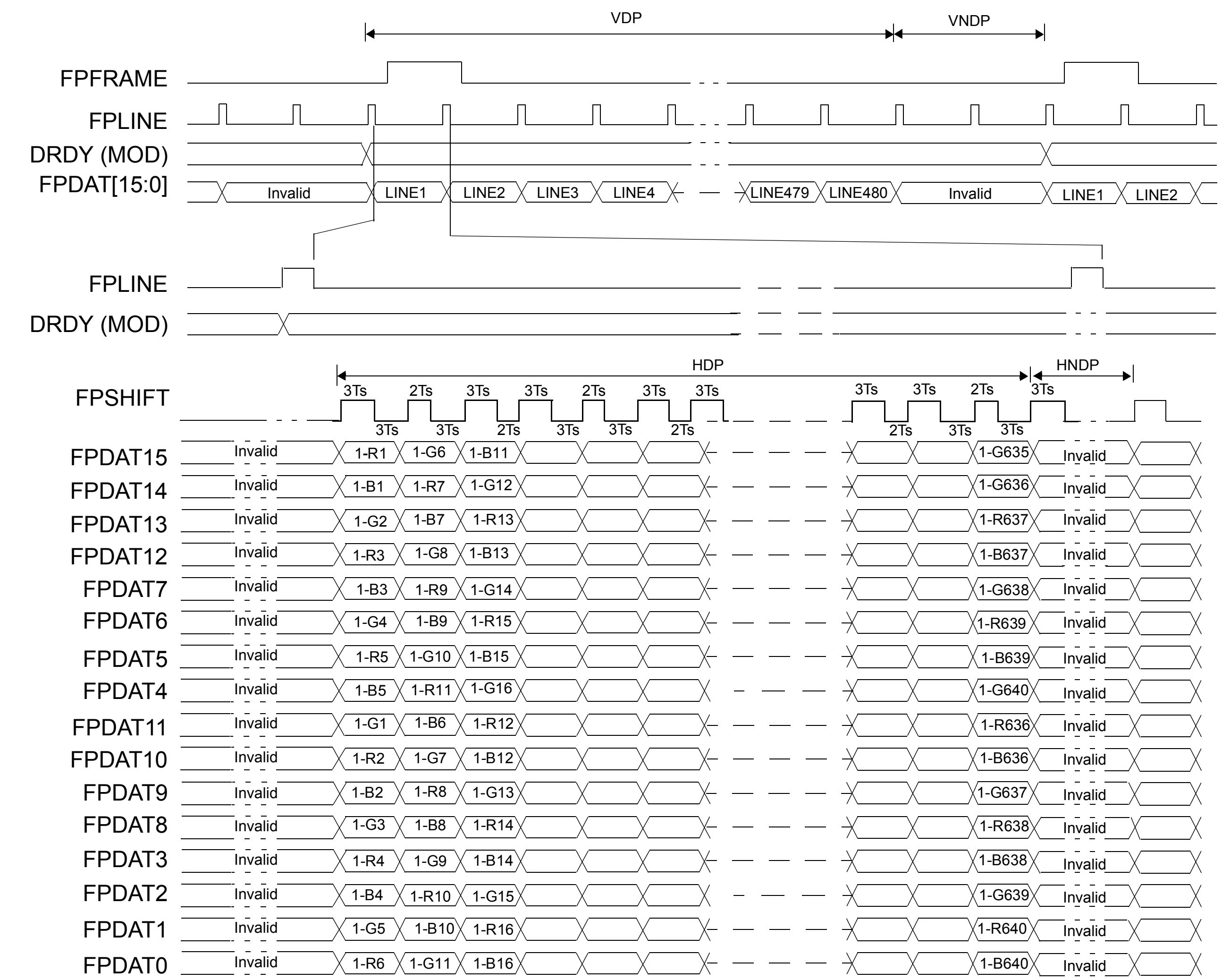
Figure 6-25: Single Color 8-Bit Panel A.C. Timing (Format 2)

Table 6-25: Single Color 8-Bit Panel A.C. Timing (Format 2)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			Ts
t9	FPSHIFT period	2			Ts
t10	FPSHIFT pulse width low	1			Ts
t11	FPSHIFT pulse width high	1			Ts
t12	FPDAT[7:0] setup to FPSHIFT falling edge	1			Ts
t13	FPDAT[7:0] hold to FPSHIFT falling edge	1			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 1, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.5.7 Single Color 16-Bit Panel Timing



Notes:

- The duty cycle of FPSHIFT changes in order to process 16 pixels in 3 FPSHIFT rising clocks
- Ts = Pixel clock period (PCLK)
- Diagram drawn with 2 FPLINE vertical blank period
- Example timing for a 640x480 panel

Figure 6-26: Single Color 16-Bit Panel Timing

VDP = Vertical Display Period
= (REG[34h] bits 9:0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[30h] bits 9:0) - (REG[34h] bits 9:0) Lines

HDP = Horizontal Display Period
= ((REG[24h] bits 6:0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[20h] bits 6:0) + 1) x 8Ts) - (((REG[24h] bits 6:0) + 1) x 8Ts)

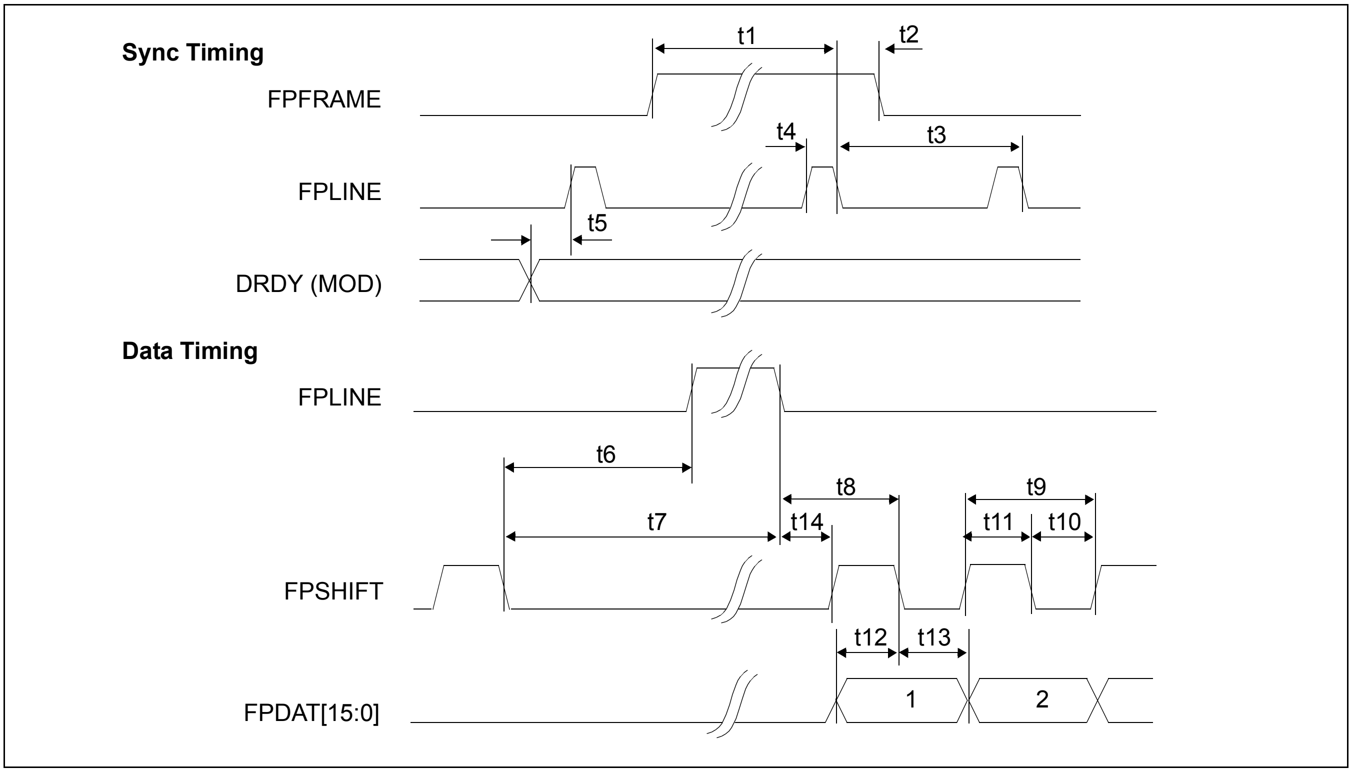


Figure 6-27: Single Color 16-Bit Panel A.C. Timing

Table 6-26: Single Color 16-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 3			Ts
t9	FPSHIFT period	5			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	FPDAT[15:0] setup to FPSHIFT rising edge	2			Ts
t13	FPDAT[15:0] hold to FPSHIFT rising edge	2			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 2, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.5.8 Generic TFT Panel Timing

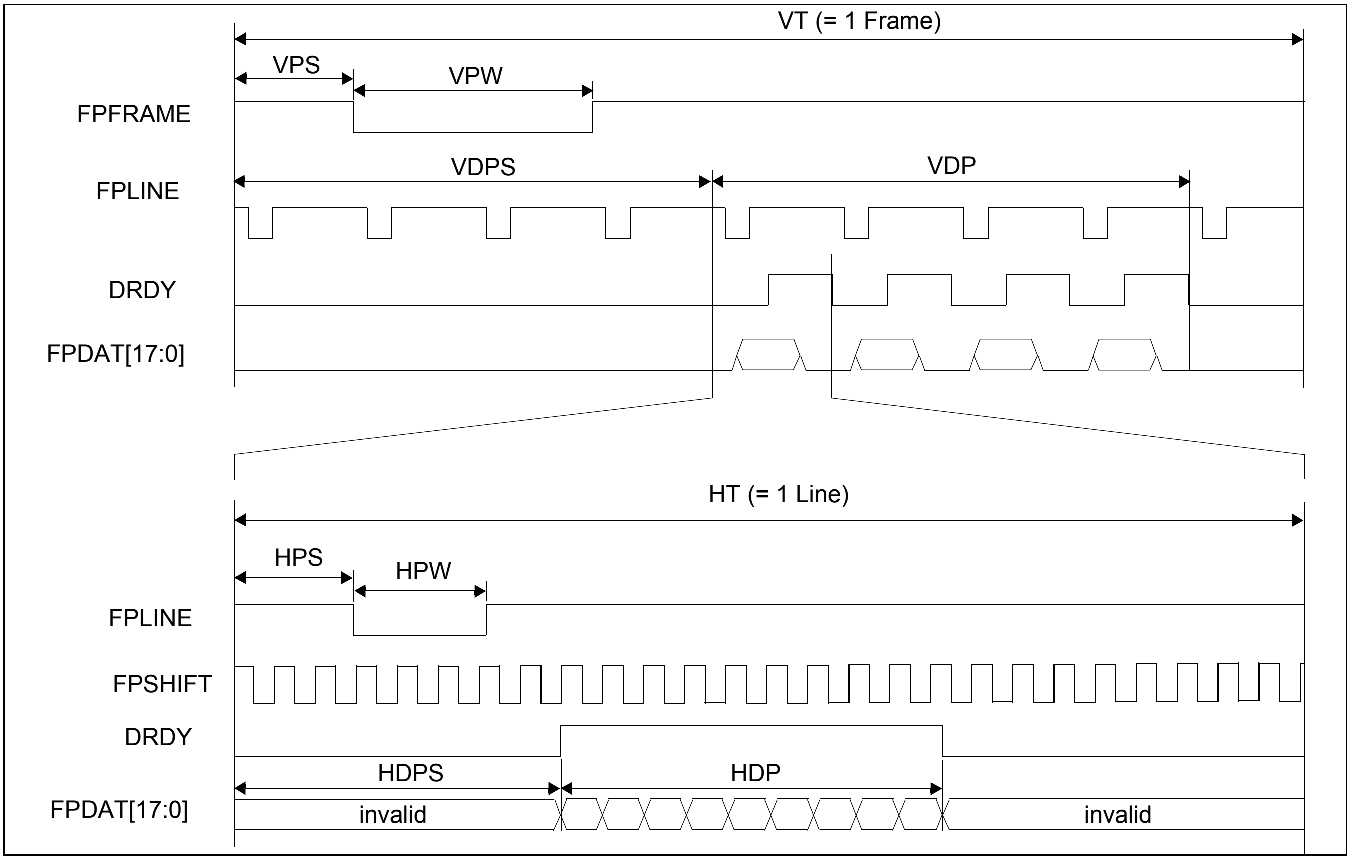


Figure 6-28: Generic TFT Panel Timing

VT	= Vertical Total	= [(REG[30h] bits 9-0) + 1] lines
VPS	= FPFRAME Pulse Start Position	= (REG[3Ch] bits 9-0) lines
VPW	= FPFRAME Pulse Width	= [(REG[3Ch] bits 18-16) + 1] lines
VDPS	= Vertical Display Period Start Position	= (REG[38h] bits 9-0) lines
VDP	= Vertical Display Period	= [(REG[34h] bits 9-0) + 1] lines
HT	= Horizontal Total	= [((REG[20h] bits 6-0) + 1) x 8] pixels
HPS	= FPLINE Pulse Start Position	= [(REG[2Ch] bits 9-0) + 1] pixels
HPW	= FPLINE Pulse Width	= [(REG[2Ch] bits 22-16) + 1] pixels
HDPS	= Horizontal Display Period Start Position	= [(REG[28h] bits 9-0) + 5] pixels
HDP	= Horizontal Display Period	= [((REG[24h] bits 6-0) + 1) x 8] pixels

*For TFT panels, the HDP must be a minimum of 8 pixels and must be increased by multiples of 8.
*Panel Type Bits (REG[0Ch] bits 1-0) = 01 (TFT)
*FPLINE Pulse Polarity Bit (REG[2Ch] bit 23) = 0 (active low)
*FPFRAME Polarity Bit (REG[3Ch] bit 23) = 0 (active low)

6.5.9 9/12/18-Bit TFT Panel Timing

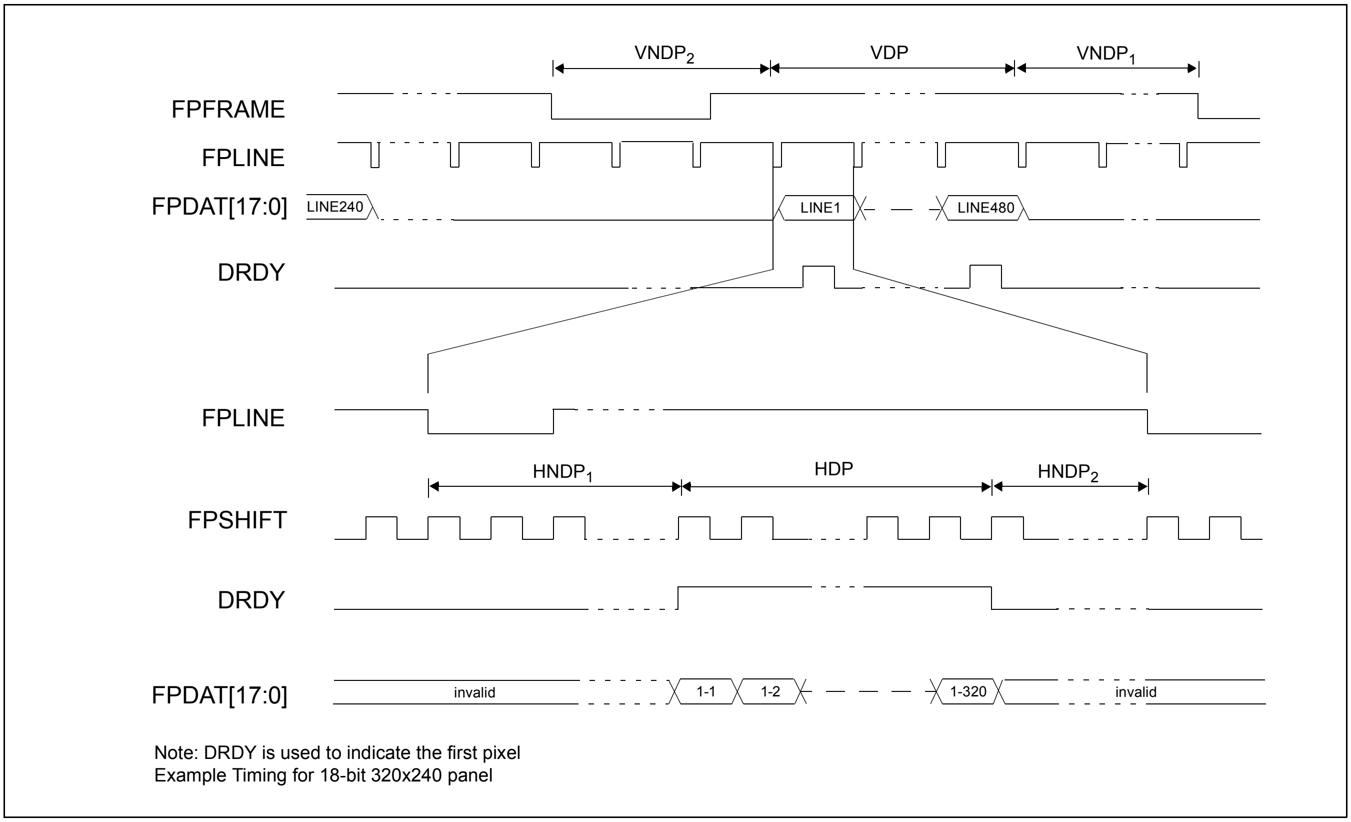


Figure 6-29: 18-Bit TFT Panel Timing

VDP	= Vertical Display Period	
	= VDP Lines	
VNDP	= Vertical Non-Display Period	
	= VNDP1 + VNDP2	
	= VT - VDP Lines	
VNDP1	= Vertical Non-Display Period 1	
	= VNDP - VNDP2 Lines	
VNDP2	= Vertical Non-Display Period 2	
	= VDPS - VPS Lines	if negative add VT
HDP	= Horizontal Display Period	
	= HDP Ts	
HNDP	= Horizontal Non-Display Period	
	= HNDP1 + HNDP2	
	= HT - HDP Ts	
HNDP1	= Horizontal Non-Display Period 1	
	= HDPS - HPS Ts	if negative add HT
HNDP2	= Horizontal Non-Display Period 2	
	= HPS - (HDP + HDPS) Ts	if negative add HT

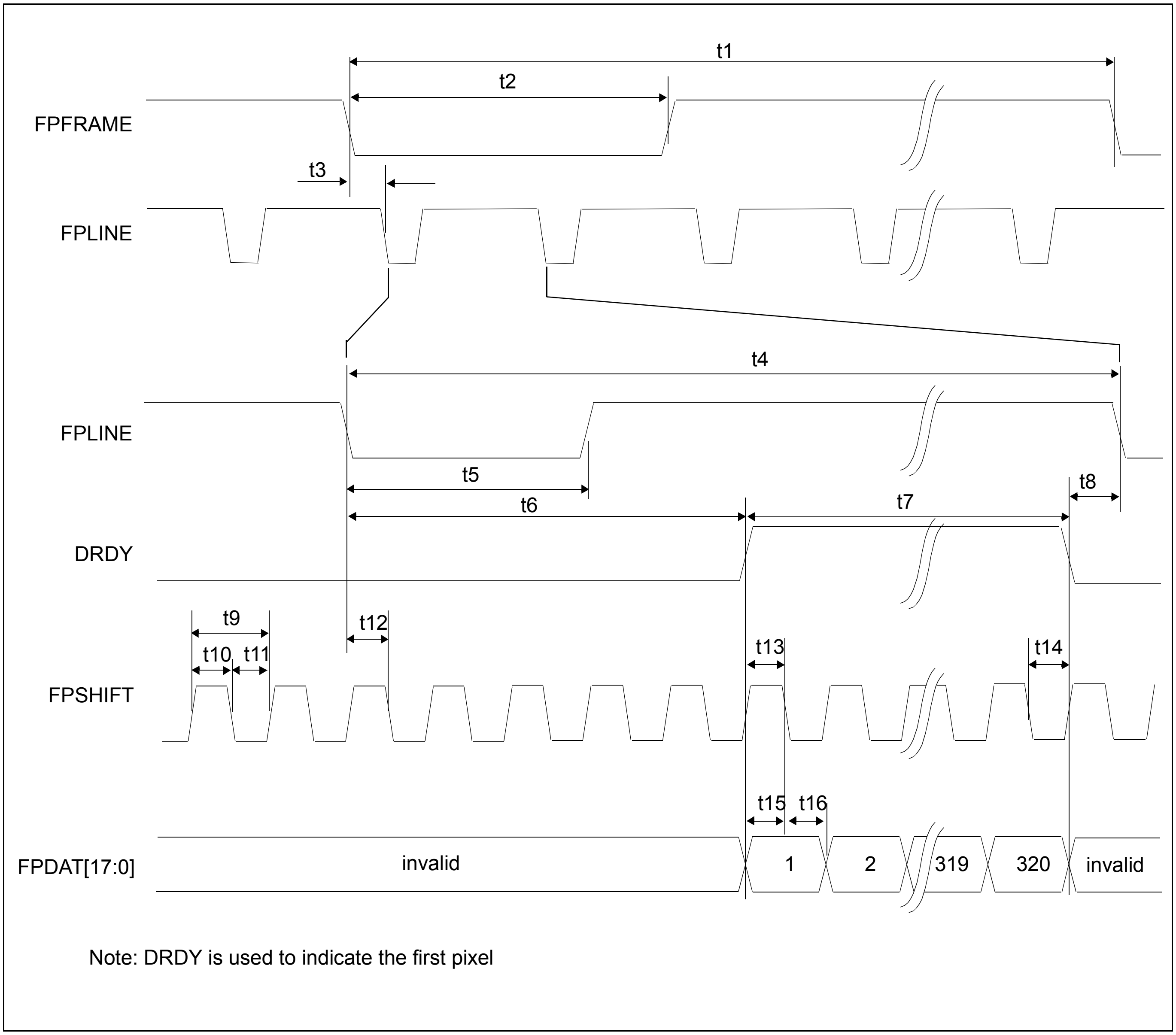


Figure 6-30: TFT A.C. Timing

Table 6-27: TFT A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME cycle time	VT			Lines
t2	FPFRAME pulse width low	VPW			Lines
t3	FPFRAME falling edge to FPLINE falling edge phase difference	HPS			Ts (note 1)
t4	FPLINE cycle time	HT			Ts
t5	FPLINE pulse width low	HPW			Ts
t6	FPLINE Falling edge to DRDY active	note 2		250	Ts
t7	DRDY pulse width	HDP			Ts
t8	DRDY falling edge to FPLINE falling edge	note 3			Ts
t9	FPSHIFT period	1			Ts
t10	FPSHIFT pulse width high	0.5			Ts
t11	FPSHIFT pulse width low	0.5			Ts
t12	FPLINE setup to FPSHIFT falling edge	0.5			Ts
t13	DRDY to FPSHIFT falling edge setup time	0.5			Ts
t14	DRDY hold from FPSHIFT falling edge	0.5			Ts
t15	Data setup to FPSHIFT falling edge	0.5			Ts
t16	Data hold from FPSHIFT falling edge	0.5			Ts

1. Ts = pixel clock period
2. t6min = HDPS - HPS if negative add HT
3. t8min = HPS - (HDP + HDPS) if negative add HT

6.5.10 160x160 Sharp 'Direct' HR-TFT Panel Timing (e.g. LQ031B1DDxx)

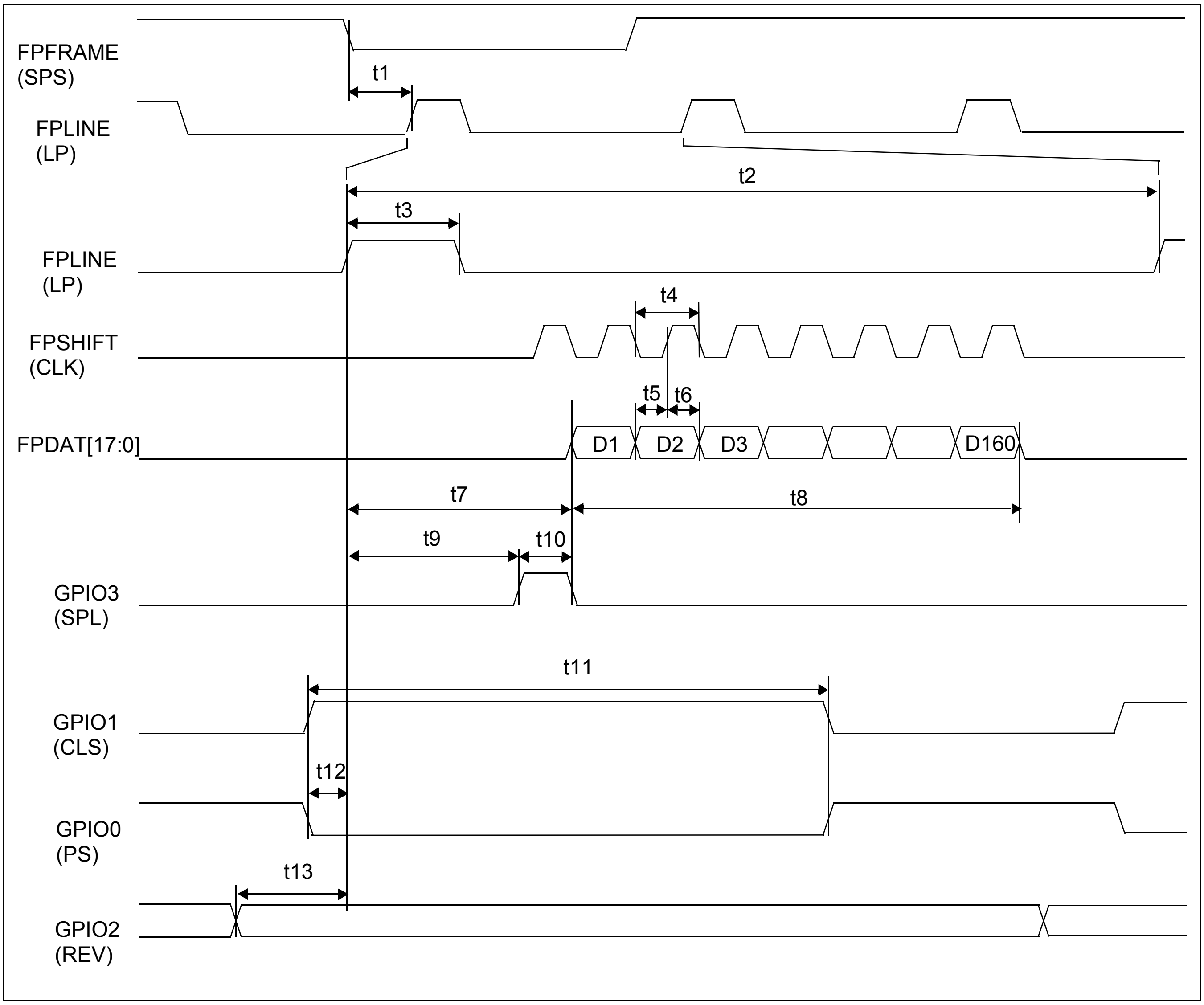


Figure 6-31: 160x160 Sharp 'Direct' HR-TFT Panel Horizontal Timing

Table 6-28: 160x160 Sharp 'Direct' HR-TFT Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPLINE start position		13		Ts (note 1)
t2	Horizontal total period	180		220	Ts
t3	FPLINE width		2		Ts
t4	FPSHIFT period		1		Ts
t5	Data setup to FPSHIFT rising edge	0.5			Ts
t6	Data hold from FPSHIFT rising edge	0.5			Ts
t7	Horizontal display start position		5		Ts
t8	Horizontal display period		160		Ts
t9	FPLINE rising edge to GPIO3 rising edge		4		Ts
t10	GPIO3 pulse width		1		Ts
t11	GPIO1(GPIO0) pulse width		136		Ts
t12	GPIO1 rising edge (GPIO0 falling edge) to FPLINE rise edge		4		Ts
t13	GPIO2 toggle edge to FPLINE rise edge		10		Ts

1. Ts = pixel clock period
2. t1typ = (REG[2Ch] bits 9-0) + 1
3. t2typ = ((REG[20h] bits 6-0) + 1) x 8
4. t3typ = (REG[2Ch] bits 22-16) + 1
5. t7typ = ((REG[28h] bits 9-0) + 5) - ((REG[2Ch] bits 9-0) + 1)
6. t8typ = ((REG[24h] bits 6-0) + 1) x 8

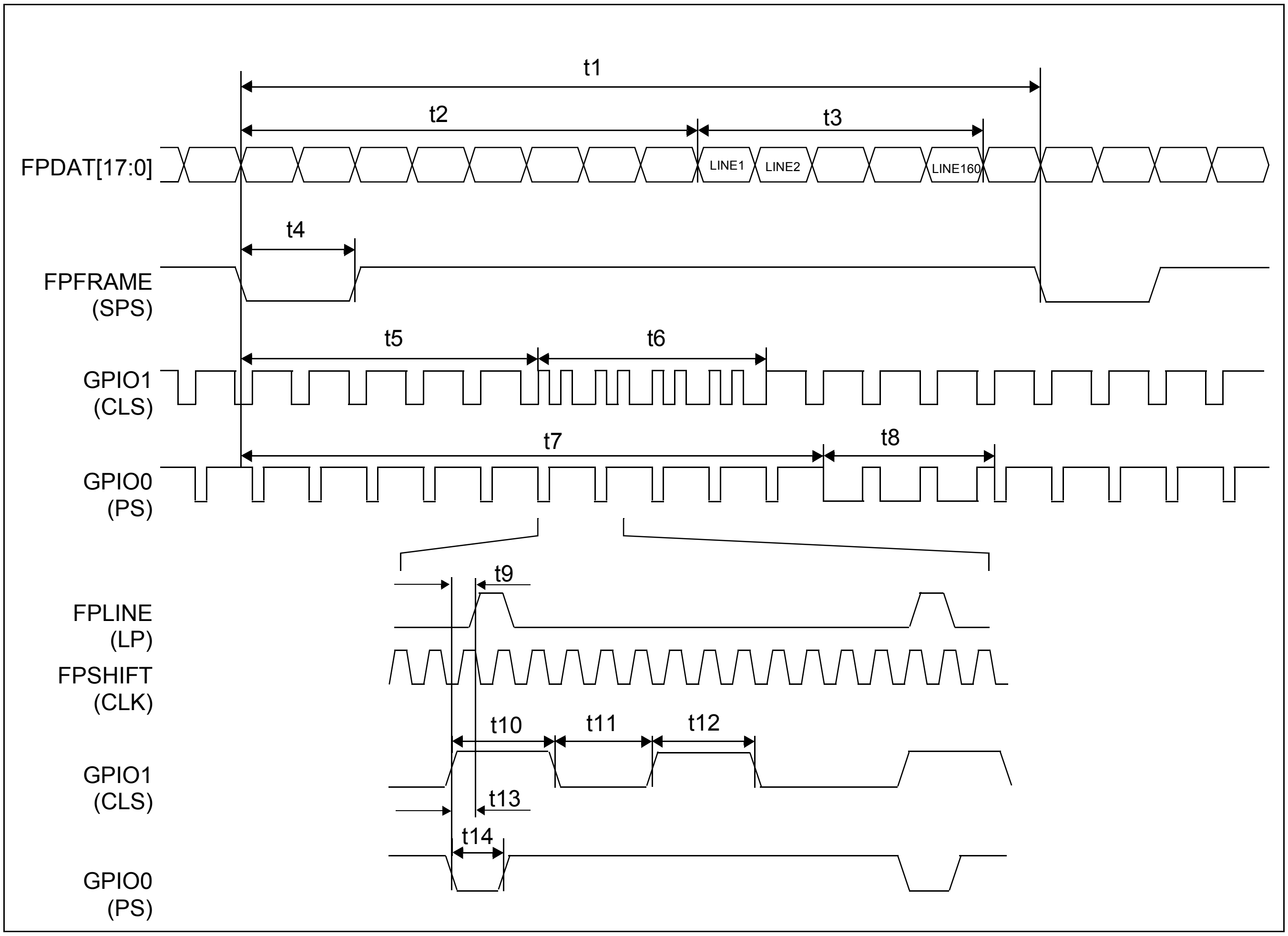


Figure 6-32: 160x160 Sharp 'Direct' HR-TFT Panel Vertical Timing

Table 6-29: 160x160 Sharp 'Direct' HR-TFT Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	203		264	Lines
t2	Vertical display start position		40		Lines
t3	Vertical display period		160		Lines
t4	Vertical sync pulse width		2		Lines
t5	FPFRAME falling edge to GPIO1 alternate timing start		5		Lines
t6	GPIO1 alternate timing period		4		Lines
t7	FPFRAME falling edge to GPIO0 alternate timing start		40		Lines
t8	GPIO0 alternate timing period		162		Lines
t9	GPIO1 first pulse rising edge to FPLINE rising edge		4		Ts (note 1)
t10	GPIO1 first pulse width		48		Ts
t11	GPIO1 first pulse falling edge to second pulse rising edge		40		Ts
t12	GPIO1 second pulse width		48		Ts
t13	GPIO0 falling edge to FPLINE rising edge		4		Ts
t14	GPIO0 low pulse width		24		Ts

1. Ts = pixel clock period

6.5.11 320x240 Sharp ‘Direct’ HR-TFT Panel Timing (e.g. LQ039Q2DS01)

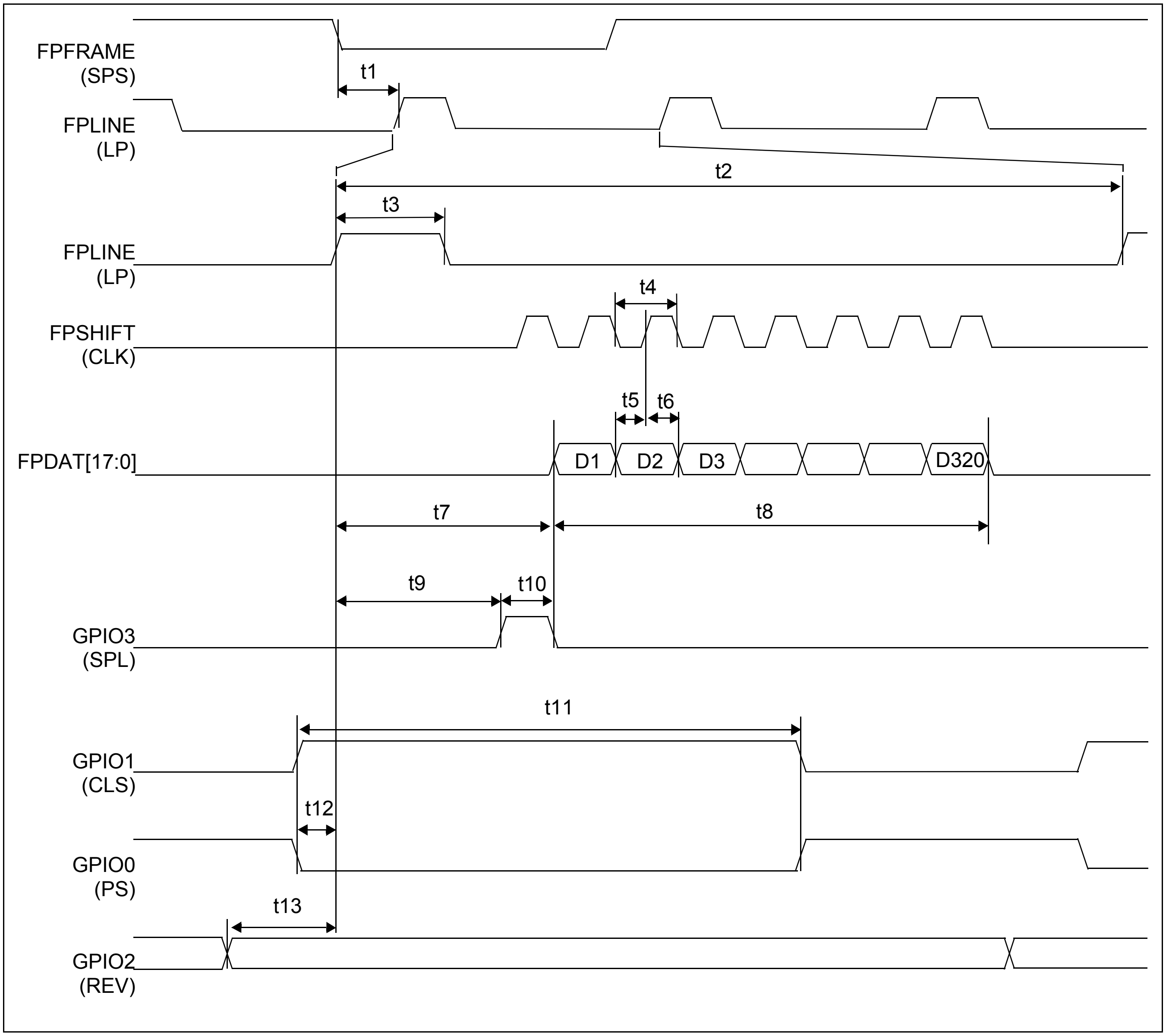


Figure 6-33: 320x240 Sharp ‘Direct’ HR-TFT Panel Horizontal Timing

Table 6-30: 320x240 Sharp ‘Direct’ HR-TFT Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPLINE start position		14		Ts (note 1)
t2	Horizontal total period	400		440	Ts
t3	FPLINE width		1		Ts
t4	FPSHIFT period		1		Ts
t5	Data setup to FPSHIFT rising edge	0.5			Ts
t6	Data hold from FPSHIFT rising edge	0.5			Ts
t7	Horizontal display start position		60		Ts
t8	Horizontal display period		320		Ts
t9	FPLINE rising edge to GPIO3 rising edge		59		Ts
t10	GPIO3 pulse width		1		Ts
t11	GPIO1(GPIO0) pulse width		353		Ts
t12	GPIO1 rising edge (GPIO0 falling edge) to FPLINE rise edge		5		Ts
t13	GPIO2 toggle edge to FPLINE rise edge		11		Ts

1. Ts = pixel clock period
2. t1typ = (REG[2Ch] bits 9-0) + 1
3. t2typ = ((REG[20h] bits 6-0) + 1) x 8
4. t3typ = (REG[2Ch] bits 22-16) + 1
5. t7typ = ((REG[28h] bits 9-0) + 5) - ((REG[2Ch] bits 9-0) + 1)
6. t8typ = ((REG[24h] bits 6-0) + 1) x 8

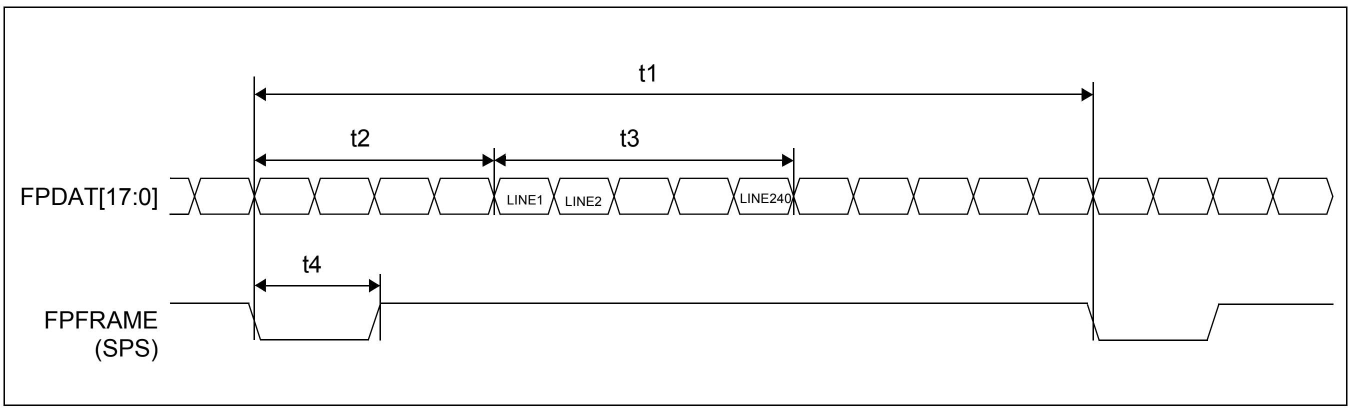


Figure 6-34: 320x240 Sharp ‘Direct’ HR-TFT Panel Vertical Timing

Table 6-31: 320x240 Sharp ‘Direct’ HR-TFT Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	245		330	Lines
t2	Vertical display start position		4		Lines
t3	Vertical display period		240		Lines
t4	Vertical sync pulse width		2		Lines

6.6 USB Timing

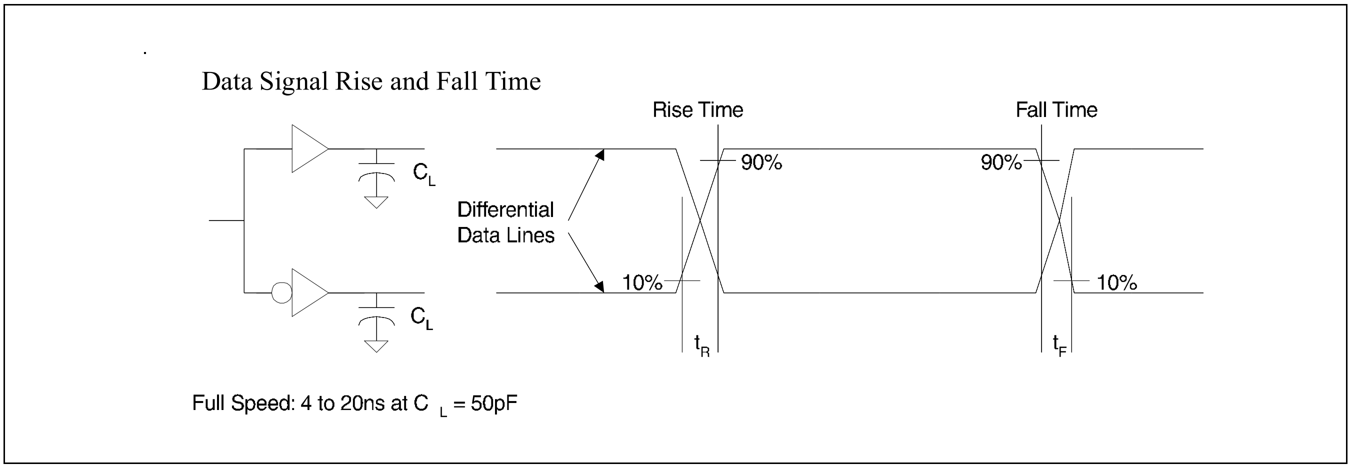


Figure 6-35 Data Signal Rise and Fall Time

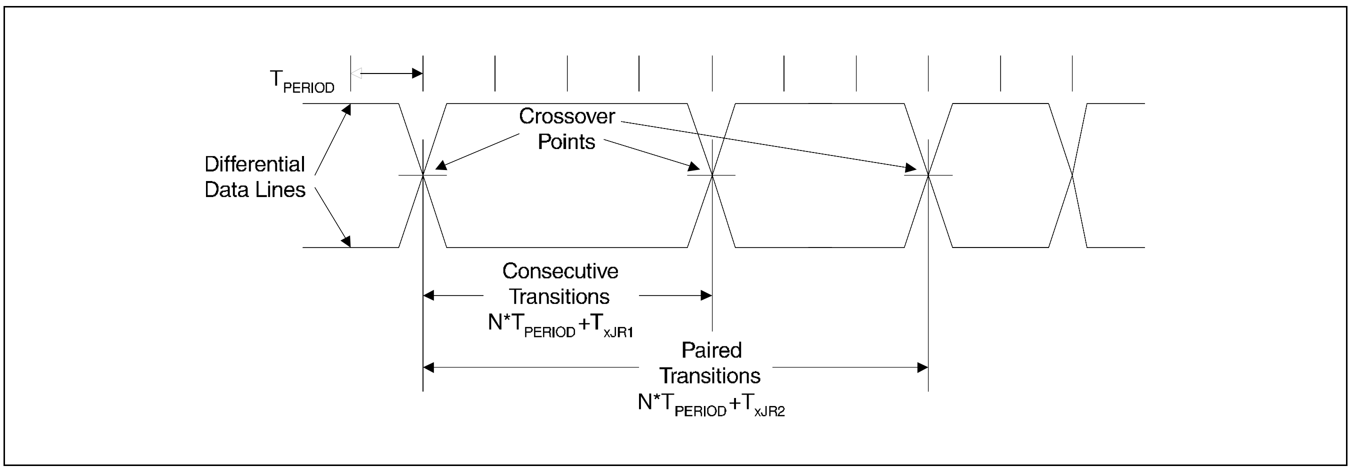


Figure 6-36 Differential Data Jitter

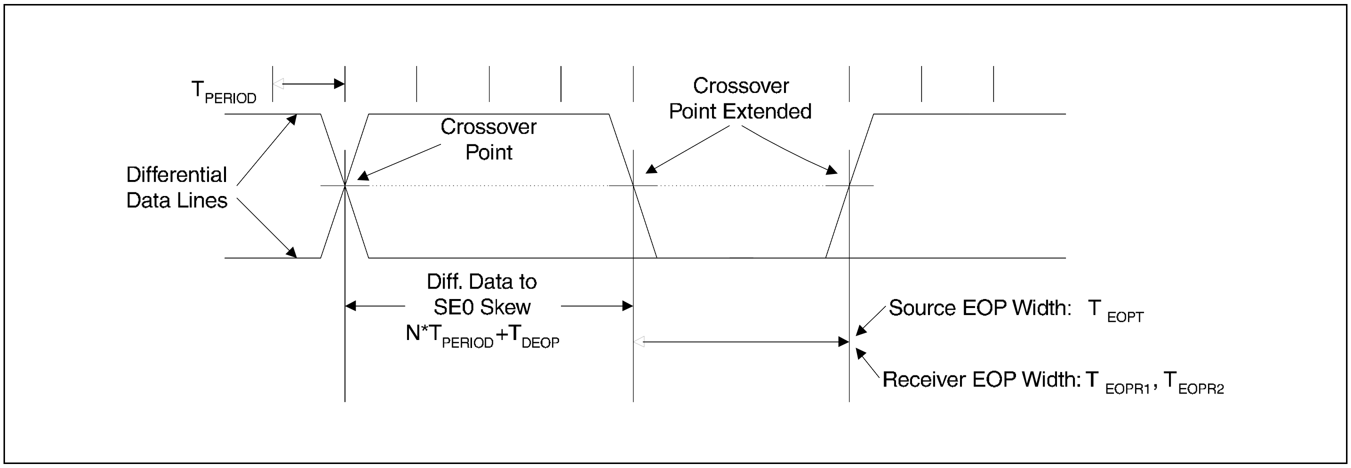


Figure 6-37 Differential to EOP Transition Skew and EOP Width

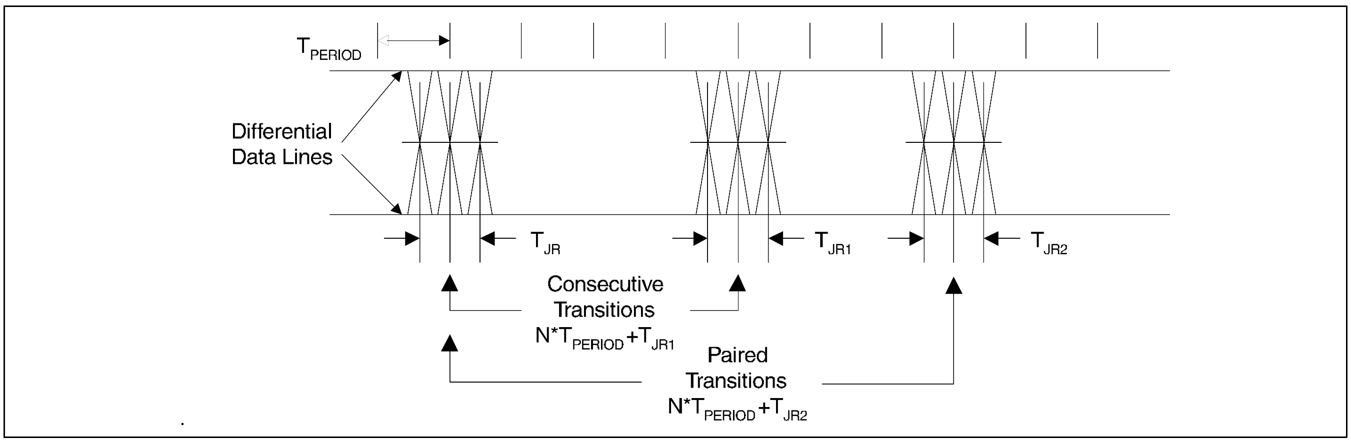


Figure 6-38 Receiver Jitter Tolerance

Table 6-32 USB Interface Timing

Symbol	Parameter	Conditions	Waveform	Min	Typ	Max	Unit
USB_{FREQ}	USB Clock Frequency				48		MHz
T_{PERIOD}	USB Clock Period		Figure 6-35		$\frac{1}{USB_{FREQ}}$		
T_R	Rise & Fall Times	C_L = 50 pF Notes 1,2	Figure 6-35	4		20	ns
T_F				4		20	
T_{RFM}	Rise/Fall time matching	(T_R / T_F)	Figure 6-35	90		110	%
V_{CRS}	Output Signal Crossover Voltage			1.3		2.0	V
Z_{DRV}	Driver Output Resistance	Steady State Drive		28 Note 5		44	Ω
T_{DRATE}	Data Rate			11.97	12	12.03	Mbs
T_{DDJ1}	Source Differential Driver Jitter to Next Transition	Notes 3,4.	Figure 6-36	-3.5	0	3.5	ns

Table 6-32 USB Interface Timing

Symbol	Parameter	Conditions	Waveform	Min	Typ	Max	Unit
T_{DDJ2}	Source Differential Driver Jitter for Paired Transitions	Notes 3,4	Figure 6-36	-4.0	0	4.0	ns
T_{DEOP}	Differential to EOP Transition Skew	Note 4	Figure 6-37	-2	0	5	ns
T_{EOPT}	Source EOP Width	Note 4	Figure 6-37	160	167	175	ns
T_{JR1}	Receiver Data Jitter Tolerance to Next Transition	Note 4	Figure 6-38	-18.5	0	18.5	ns
T_{JR2}	Receiver Data Jitter Tolerance for Paired Transitions	Note 4	Figure 6-38	-9	0	9	ns
T_{EOPR1}	EOP Width at Receiver; Must reject as EOP	Note 4	Figure 6-37	40			ns
T_{EOPR2}	EOP Width at Receiver; Must accept as EOP	Note 4	Figure 6-37	80			ns

1 Measured from 10% to 90% of the data signal.
2 The rising and falling edges should be smoothly transitioning (monotonic).
3 Timing difference between the differential data signals.
4 Measured at crossover point of differential data signals.
5 20 Ω is placed in series to meet this USB specification. The actual driver output impedance is 15 Ω.

7 Clocks

7.1 Clock Descriptions

7.1.1 BCLK

BCLK is an internal clock derived from CLKI. BCLK can be a divided version (÷1, ÷2) of CLKI. CLKI is typically derived from the host CPU bus clock.

The source clock options for BCLK may be selected as in the following table.

Table 7-1: BCLK Clock Selection

Source Clock Options	BCLK Selection
CLKI	CNF6 = 0
CLKI ÷ 2	CNF6 = 1

Note
For synchronous bus interfaces, it is recommended that BCLK be set the same as the CPU bus clock (not a divided version of CLKI) e.g. SH-3, SH-4.

7.1.2 MCLK

MCLK provides the internal clock required to access the embedded SRAM. The S1D13A04 is designed with efficient power saving control for clocks (clocks are turned off when not used); reducing the frequency of MCLK does not necessarily save more power. Furthermore, reducing the MCLK frequency relative to the BCLK frequency increases the CPU cycle latency and so reduces screen update performance. For a balance of power saving and performance, the MCLK should be configured to have a high enough frequency setting to provide sufficient screen refresh as well as acceptable CPU cycle latency.

Note
The maximum frequency of MCLK is 50MHz (30MHz if running CORE V_{DD} at 2.0V ± 10%). As MCLK is derived from BCLK, when BCLK is greater than 50MHz, MCLK must be divided using REG[04h] bits 5-4.

The Memory Controller Power Save Status bit (REG[14h] bit 6) must return a 1 before disabling the MCLK source.

The source clock options for MCLK may be selected as in the following table.

Table 7-2: MCLK Clock Selection

Source Clock Options	MCLK Selection
BCLK	REG[04h] bits 5-4 = 00
BCLK ÷ 2	REG[04h] bits 5-4 = 01
BCLK ÷ 3	REG[04h] bits 5-4 = 10
BCLK ÷ 4	REG[04h] bits 5-4 = 11

7.1.3 PCLK

PCLK is the internal clock used to control the panel. It should be chosen to match the optimum frame rate of the panel. See Section 10, “Frame Rate Calculation” on page 147 for details on the relationship between PCLK and frame rate.

Some flexibility is possible in the selection of PCLK. Firstly, panels typically have a range of permissible frame rates. Secondly, it may be possible to choose a higher PCLK frequency and tailor the horizontal non-display period to bring down the frame-rate to its optimal value.

The source clock options for PCLK may be selected as in the following table.

Table 7-3: PCLK Clock Selection

Source Clock Options	PCLK Selection
MCLK	REG[08h] bits 7-0 = 00h
MCLK ÷2	REG[08h] bits 7-0 = 10h
MCLK ÷3	REG[08h] bits 7-0 = 20h
MCLK ÷4	REG[08h] bits 7-0 = 30h
MCLK ÷8	REG[08h] bits 7-0 = 40h
BCLK	REG[08h] bits 7-0 = 01h
BCLK ÷2	REG[08h] bits 7-0 = 11h
BCLK ÷3	REG[08h] bits 7-0 = 21h
BCLK ÷4	REG[08h] bits 7-0 = 31h
BCLK ÷8	REG[08h] bits 7-0 = 41h
CLKI	REG[08h] bits 7-0 = 02h
CLKI ÷2	REG[08h] bits 7-0 = 12h
CLKI ÷3	REG[08h] bits 7-0 = 22h
CLKI ÷4	REG[08h] bits 7-0 = 32h
CLKI ÷8	REG[08h] bits 7-0 = 42h
CLKI2	REG[08h] bits 7-0 = 03h
CLKI2 ÷2	REG[08h] bits 7-0 = 13h
CLKI2 ÷3	REG[08h] bits 7-0 = 23h
CLKI2 ÷4	RREG[08h] bits 7-0 = 33h
CLKI2 ÷8	REG[08h] bits 7-0 = 43h

There is a relationship between the frequency of MCLK and PCLK that must be maintained.

Table 7-4: Relationship between MCLK and PCLK

SwivelView Orientation	Color Depth (bpp)	MCLK to PCLK Relationship
SwivelView 0° and 180°	16	$f_{MCLK} \geq f_{PCLK}$
	8	$f_{MCLK} \geq f_{PCLK} \div 2$
	4	$f_{MCLK} \geq f_{PCLK} \div 4$
	2	$f_{MCLK} \geq f_{PCLK} \div 8$
	1	$f_{MCLK} \geq f_{PCLK} \div 16$
SwivelView 90° and 270°	16/8/4/2/1	$f_{MCLK} \geq 1.25 f_{PCLK}$

7.1.4 PWMCLK

PWMCLK is the internal clock used by the Pulse Width Modulator for output to the panel.

The source clock options for PWMCLK may be selected as in the following table.

Table 7-5: PWMCLK Clock Selection

Source Clock Options	PWMCLK Selection
CLKI	REG[70h] bits 2-1 = 00
CLKI2	REG[70h] bits 2-1 = 01
MCLK	REG[70h] bits 2-1 = 10
PCLK	REG[70h] bits 2-1 = 11

For further information on controlling PWMCLK, see “PWM Clock Configuration Register” on page 114..

7.1.5 USBCLK

CLKUSB is an internal clock derived from USBCLK and should be fixed at 48MHz. USBCLK must be active to access the USB Registers.

7.2 Clock Selection

The following diagram provides a logical representation of the S1D13A04 internal clocks.

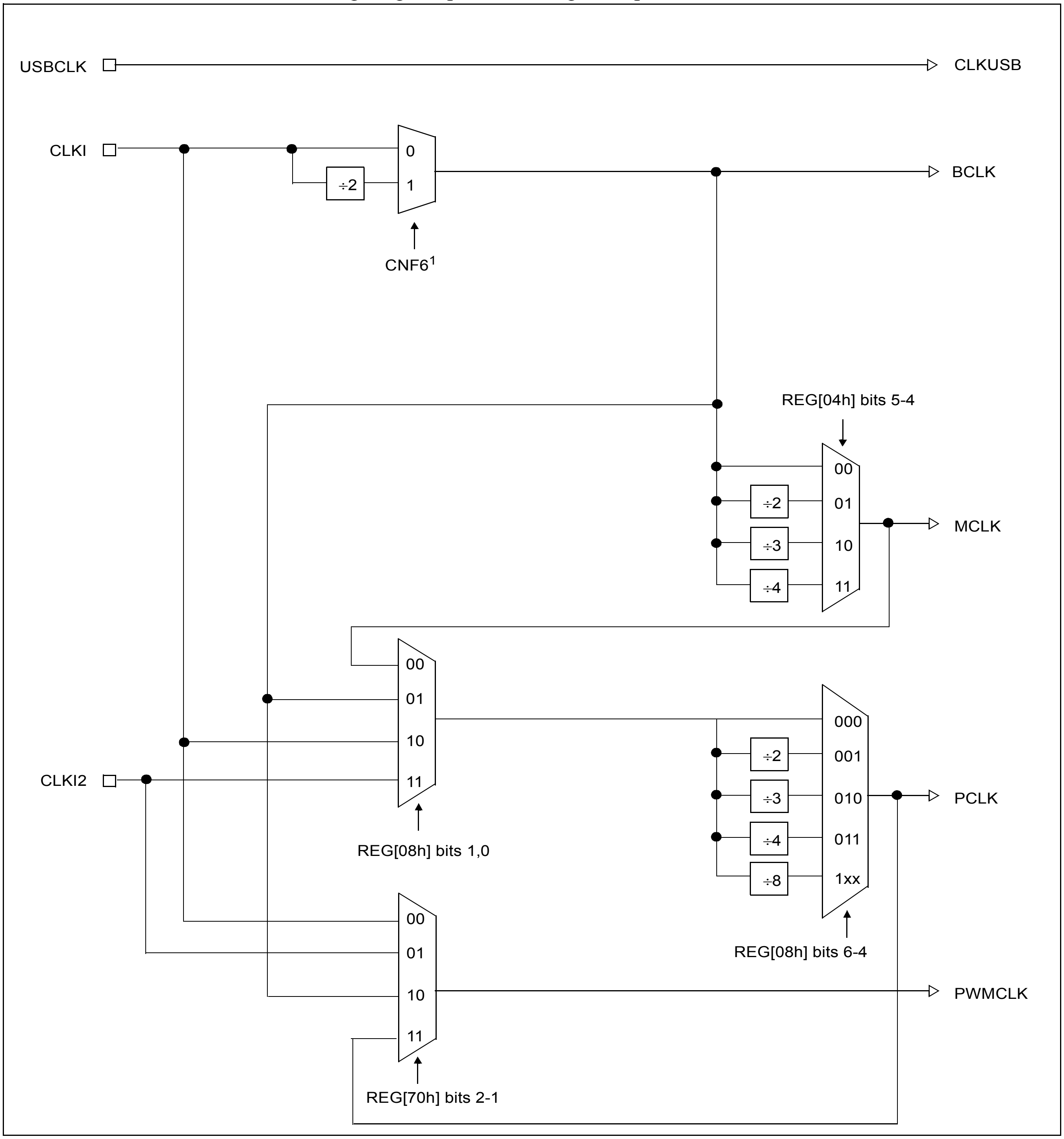


Figure 7-1: Clock Selection

Note
[1] CNF6 must be set at RESET#.

7.3 Clocks versus Functions

Table 7-6: “S1D13A04 Internal Clock Requirements”, lists the internal clocks required for the following S1D13A04 functions.

Table 7-6: S1D13A04 Internal Clock Requirements

Function	Bus Clock (BCLK)	Memory Clock (MCLK)	Pixel Clock (PCLK)	PWM Clock (PWMCLK)	USB Clock (USBCLK)
Register Read/Write	Required	Not Required	Not Required	Not Required[1]	Not Required
Memory Read/Write	Required	Required	Not Required	Not Required[1]	Not Required
Look-Up Table Register Read/Write	Required	Required	Not Required	Not Required[1]	Not Required
Software Power Save	Required	Not Required	Not Required	Not Required[1]	Not Required
LCD Output	Required	Required	Required	Not Required[1]	Not Required
USB Register Read/Write	Required	Not Required	Not Required	Not Required[1]	Required

Note
[1]PWMCLK is an optional clock (see Section 7.1.4, “PWMCLK” on page 85).

8 Registers

This section discusses how and where to access the S1D13A04 registers. It also provides detailed information about the layout and usage of each register.

8.1 Register Mapping

The S1D13A04 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0, the registers may be accessed. The register space is decoded by AB[16:0] and is mapped as follows.

Table 8-1: S1D13A04 Register Mapping

M/R#	Address	Size	Function
1	00000h to 28000h	160K bytes	SRAM memory
0	0000h to 0088h	136 bytes	Configuration registers
0	4000h to 4054h	84 bytes	USB registers
0	8000h to 8019h	25 bytes	2D Acceleration Registers
0	10000h to 1FFFEh	65536 bytes (64K bytes)	2D Accelerator Data Port

8.2 Register Set

The S1D13A04 register set is as follows.

Table 8-2: S1D13A04 Register Set

Register	Pg	Register	Pg
LCD Register Descriptions (Offset = 0h)			
Read-Only Configuration Registers			
REG[00h] Product Information Register	90		
Clock Configuration Registers			
REG[04h] Memory Clock Configuration Register	91	REG[08h] Pixel Clock Configuration Register	92
Panel Configuration Registers			
REG[0Ch] Panel Type & MOD Rate Register	93	REG[10h] Display Settings Register	94
REG[14h] Power Save Configuration Register	96		
Look-Up Table Registers			
REG[18h] Look-Up Table Write Register	98	REG[1Ch] Look-Up Table Read Register	99
Display Mode Registers			
REG[20h] Horizontal Total Register	100	REG[24h] Horizontal Display Period Register	100
REG[28h] Horizontal Display Period Start Position Register	101	REG[2Ch] FPLINE Register	101
REG[30h] Vertical Total Register	102	REG[34h] Vertical Display Period Register	102
REG[38h] Vertical Display Period Start Position Register	103	REG[3Ch] FPFRAME Register	103
REG[40h] Main Window Display Start Address Register	104	REG[44h] Main Window Line Address Offset Register	104
Picture-in-Picture Plus (PIP$^+$) Registers			

Table 8-2: S1D13A04 Register Set

Register	Pg	Register	Pg
REG[50h] PIP+ Window Display Start Address Register	105	REG[54h] PIP+ Window Line Address Offset Register	105
REG[58h] PIP+ Window X Positions Register	106	REG[5Ch] PIP+ Window Y Positions Register	108
Miscellaneous Registers			
REG[60h] Special Purpose Register	110	REG[64h] GPIO Status and Control Register	112
REG[70h] PWM Clock Configuration Register	114	REG[74h] PWMOUT Duty Cycle Register	115
REG[80h] Scratch Pad A Register	116	REG[84h] Scratch Pad B Register	116
REG[88h] Scratch Pad C Register	117		
USB Register Descriptions (Offset = 4000h)			
REG[4000h] Control Register	118	REG[4002h] Interrupt Enable Register 0	119
REG[4004h] Interrupt Status Register 0	120	REG[4006h] Interrupt Enable Register 1	120
REG[4008h] Interrupt Status Register 1	122	REG[4010h] Endpoint 1 Index Register	122
REG[4012h] Endpoint 1 Receive Mailbox Data Register	122	REG[4018h] Endpoint 2 Index Register	123
REG[401Ah] Endpoint 2 Transmit Mailbox Data Register	123	REG[401Ch] Endpoint 2 Interrupt Polling Interval Register	123
REG[4020h] Endpoint 3 Receive FIFO Data Register	123	REG[4022h] Endpoint 3 Receive FIFO Count Register	124
REG[4024h] Endpoint 3 Receive FIFO Status Register	124	REG[4026h] Endpoint 3 Maximum Packet Size Register	124
REG[4028h] Endpoint 4 Transmit FIFO Data Register	125	REG[402Ah] Endpoint 4 Transmit FIFO Count Register	125
REG[402Ch] Endpoint 4 Transmit FIFO Status Register	125	REG[402Eh] Endpoint 4 Maximum Packet Size Register	126
REG[4030h] Endpoint 4 Maximum Packet Size Register	126	REG[4032h] USB Status Register	126
REG[4034h] Frame Counter MSB Register	127	REG[4036h] Frame Counter LSB Register	127
REG[4038h] Extended Register Index	127	REG[403Ah] Extended Register Data	127
REG[403Ah], Index[00h] Vendor ID MSB	128	REG[403Ah], Index[01h] Vendor ID LSB	128
REG[403Ah], Index[02h] Product ID MSB	128	REG[403Ah], Index[03h] Product ID LSB	128
REG[403Ah], Index[04h] Release Number MSB	128	REG[403Ah], Index[05h] Release Number LSB	128
REG[403Ah], Index[06h] Receive FIFO Almost Full Threshold	129	REG[403Ah], Index[07h] Transmit FIFO Almost Empty Threshold	129
REG[403Ah], Index[08h] USB Control	129	REG[403Ah], Index[09h] Maximum Power Consumption	129
REG[403Ah], Index[0Ah] Packet Control	130	REG[403Ah], Index[0Bh] Reserved	130
REG[403Ah], Index[0Ch] FIFO Control	131	REG[4040h] USBFC Input Control Register	131
REG[4042h] Reserved	132	REG[4044h] Pin Input Status / Pin Output Data Register	132
REG[4046h] Interrupt Control Enable Register 0	133	REG[4048h] Interrupt Control Enable Register 1	133
REG[404Ah] Interrupt Control Status/Clear Register 0	134	REG[404Ch] Interrupt Control Status/Clear Register 1	135
REG[404Eh] Interrupt Control Masked Status Register 0	136	REG[4050h] Interrupt Control Masked Status Register 1	136
REG[4052h] USB Software Reset Register	136	REG[4054h] USB Wait State Register	137
2D Acceleration (BitBLT) Register Descriptions (Offset = 8000h)			
REG[8000h] BitBLT Control Register	138	REG[8004h] BitBLT Status Register	139
REG[8008h] BitBLT Command Register	140	REG[800Ch] BitBLT Source Start Address Register	142
REG[8010h] BitBLT Destination Start Address Register	142	REG[8014h] BitBLT Memory Address Offset Register	143
REG[8018h] BitBLT Width Register	143	REG[801Ch] BitBLT Height Register	143
REG[8020h] BitBLT Background Color Register	143	REG[8024h] BitBLT Foreground Color Register	144
2D Acceleration (BitBLT) Data Register Descriptions (Offset = 10000h)			
AB16-AB0 = 10000h-1FFFEh, 2D Accelerator (BitBLT) Data Memory Mapped Region Register			145

8.3 LCD Register Descriptions (Offset = 0h)

Unless specified otherwise, all register bits are set to 0 during power-on.

8.3.1 Read-Only Configuration Registers

Product Information Register
REG[00h] Default = 2Cxx282Ch Read Only

Product Code bits 5-0						Revision Code bits 1-0		n/a	CNF[6:0] Status						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Display Buffer Size bits 7-0								Product Code bits 5-0						Revision Code bits 1-0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 31-26 Product Code
These read-only bits indicate the product code. The product code is 001011 (0Bh).

bits 25-24 Revision Code
These are read-only bits that indicates the revision code. The revision code is 00.

bits 22-16 CNF[6:0] Status
These read-only status bits return the status of the configuration pins CNF[6:0]. CNF[6:0] are latched at the rising edge of RESET#. For a functional description of each configuration bit (CNF[6:0]), see Section 4.4, “Summary of Configuration Options” on page 26.

Note
CNF3 Status (bit 19) always reads back a 1. The CNF3 pin is reserved and must be set to 1.

bits 15-8 Display Buffer Size Bits [7:0]
This is a read-only register that indicates the size of the SRAM display buffer measured in 4K byte increments. The S1D13A04 display buffer is 160K bytes and therefore this register returns a value of 40 (28h).

Value of this register = display buffer size ÷ 4K bytes
= 160K bytes ÷ 4K bytes
= 40 (28h)

bits 7-2 Product Code
These read-only bits indicate the product code. The product code is 001011 (0Bh).

bits 1-0 Revision Code
These are read-only bits that indicates the revision code. The revision code is 00.

8.3.2 Clock Configuration Registers

Memory Clock Configuration Register
REG[04h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a										MCLK Divide Select bits 1-0		Reserved			

bits 5-4 MCLK Divide Select Bits [1:0]
These bits determine the divide used to generate the Memory Clock (MCLK) from the Bus Clock (BCLK).

Table 8-3: MCLK Divide Selection

MCLK Divide Select Bits	BCLK to MCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

bit 0 Reserved.
This bit must be set to 0.

Pixel Clock Configuration Register															
REG[08h]				Default = 00000000h											Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a									PCLK Divide Select bits 2-0			n/a		PCLK Source Select bits 1-0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 6-4 PCLK Divide Select Bits [1:0]
These bits determine the divide used to generate the Pixel Clock (PCLK) from the Pixel Clock Source.

Table 8-4: PCLK Divide Selection

PCLK Divide Select Bits	PCLK Source to PCLK Frequency Ratio
000	1:1
001	2:1
010	3:1
011	4:1
100	8:1
101 - 111	Reserved

bits 1-0 PCLK Source Select Bits [1:0]
These bits determine the source of the Pixel Clock (PCLK).

Table 8-5: PCLK Source Selection

PCLK Source Select Bits	PCLK Source
00	MCLK
01	BCLK
10	CLKI
11	CLKI2

8.3.3 Panel Configuration Registers

Panel Type & MOD Rate Register
REG[0Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a										MOD Rate bits 5-0					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a								Panel Data Format Select	Color/ Mono Panel Select	Panel Data Width bits 1-0		'Direct' HR-TFT Res Select	n/a	Panel Type bits 1-0	

bits 21-16 MOD Rate Bits [5:0]
These bits are for passive LCD panels only.
When these bits are all 0, the MOD output signal (DRDY) toggles every FPFRAME.
For a non-zero value *n*, the MOD output signal (DRDY) toggles every n FPLINE.

bit 7 Panel Data Format Select
When this bit = 0, 8-bit single color passive LCD panel data format 1 is selected. For AC timing see Section 6.5.5, "Single Color 8-Bit Panel Timing (Format 1)" on page 64.
When this bit = 1, 8-bit single color passive LCD panel data format 2 is selected. For AC timing see Section 6.5.6, "Single Color 8-Bit Panel Timing (Format 2)" on page 66.

bit 6 Color/Mono Panel Select
When this bit = 0, a monochrome LCD panel is selected.
When this bit = 1, a color LCD panel is selected.

bits 5-4 Panel Data Width Bits [1:0]
These bits select the data width size of the LCD panel.

Table 8-6: Panel Data Width Selection

Panel Data Width Bits [1:0]	Passive Panel Data Width Size	Active Panel Data Width Size
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	18-bit
11	Reserved	Reserved

bit 3 'Direct' HR-TFT Resolution Select
This bit selects one of two panel resolutions when the 'Direct' HR-TFT interface is selected. This bit has no effect for other panel types.

Table 8-7: Active Panel Resolution Selection

'Direct' HR-TFT Resolution Select Bit	HR-TFT Resolution
0	160x160
1	320x240

bits 1-0 Panel Type Bits[1:0]
These bits select the panel type.

Table 8-8: LCD Panel Type Selection

Panel Type Bits [1:0]	Panel Type
00	STN
01	TFT
10	'Direct' HR-TFT
11	Reserved

Display Settings Register
REG[10h] Default = 00000000h Read/Write

n/a						Pixel Doubling Vertical	Pixel Doubling Horiz.	Display Blank	Dithering Disable	n/a	SW Video Invert	PIP+ Window Enable	n/a	SwivelView Mode Select	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a											Bits-per-pixel Select (actual value: 1, 2, 4, 8 or 16 bpp)				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bit 25 Pixel Doubling Vertical Enable
This bit controls the pixel doubling feature for the vertical dimension or height of the panel (i.e. 160 pixel high data doubled to 320 pixel high panel).
When this bit = 1, pixel doubling in the vertical dimension (height) is enabled.
When this bit = 0, there is no hardware effect.

Note
Pixel Doubling is not designed to support color depths of 1 bit-per-pixel or SwivelView 90° / 270° modes.

bit 24 Pixel Doubling Horizontal Enable
This bit controls the pixel doubling feature for the horizontal dimension or width of the panel (i.e. 160 pixel wide data doubled to 320 pixel wide panel)
When this bit = 1, pixel doubling in the horizontal dimension (width) is enabled.
When this bit = 0, there is no hardware effect.

Note
Pixel Doubling is not designed to support color depths of 1 bit-per-pixel or SwivelView 90° / 270° modes.

bit 23 Display Blank
When this bit = 0, the LCD display pipeline is enabled.
When this bit = 1, the LCD display pipeline is disabled and all LCD data outputs are forced to zero (i.e., the screen is blanked).

bit 22 Dithering Disable
When this bit = 0, dithering on the passive LCD panel is enabled, allowing a maximum of 64K colors (2^{18}) or 64 gray shades in 1/2/4/8 bpp mode. In 16bpp mode, only 64K colors (2^{16}) can also be achieved.
When this bit = 1, dithering on the passive LCD panel is disabled, allowing a maximum of 4096 colors (2^{12}) or 16 gray shades.
The dithering algorithm provides more shades of each primary color.

Note
For a summary of the results of dithering for each color depth, see Table 8-10: "LCD Bit-per-pixel Selection," on page 96.

bit 20 Software Video Invert
When this bit = 0, video data is normal.
When this bit = 1, video data is inverted.

Note
Video data is inverted after the Look-Up Table

bit 19 PIP+ Window Enable
This bit enables a PIP+ window within the main window. The location of the PIP+ window within the landscape window is determined by the PIP+ X Position register (REG[58h]) and PIP+ Y Position register (REG[5Ch]). The PIP+ window has its own Display Start Address register (REG[50h]) and Memory Address Offset register (REG[54h]). The PIP+ window shares the same color depth and SwivelView™ orientation as the main window.
When this bit = 1, the PIP+ window is enabled.
When this bit = 0, the PIP+ window is disabled.

bit 17-16 SwivelView Mode Select Bits [1:0]
These bits select different SwivelView™ orientations:

Table 8-9: SwivelView™ Mode Select Options

SwivelView Mode Select Bits	SwivelView Orientation
00	0° (Normal)
01	90°
10	180°
11	270°

bits 4-0 Bit-per-pixel Select Bits [4:0]
These bits select the color depth (bit-per-pixel) for the displayed data for both the main window and the PIP+ window (if active).

1, 2, 4 and 8 bpp modes use the 18-bit LUT, allowing maximum 64K colors. 16 bpp mode bypasses the LUT, allowing only 64K colors.

Table 8-10: LCD Bit-per-pixel Selection

Bit-per-pixel Select Bits [4:0]	Color Depth (bpp)	Maximum Number of Colors/Shades		Max. No. Of Simultaneously Displayed Colors/Shades
		Passive Panel (Dithering On)	TFT Panel	
00000	Reserved			
00001	1 bpp	64K/64	64K/64	2/2
00010	2 bpp	64K/64	64K/64	4/4
00011	Reserved			
00100	4 bpp	64K/64	64K/64	16/16
00101 - 00111	Reserved			
01000	8 bpp	64K/64	64K/64	256/64
10000	16 bpp	64K/64	64K/64	64K/64
10001 - 11111	Reserved			

Power Save Configuration Register															
REG[14h]				Default = 00000010h										Read/Write	
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								VNDP Status (RO)	Memory Power Save Status (RO)	n/a	Power Save Enable	n/a			'Direct' HR-TFT GPO Control
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bit 7 Vertical Non-Display Period Status (Read-only)
This is a read-only status bit.
When this bit = 0, the LCD panel output is in a Vertical Display Period.
When this bit = 1, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Memory Controller Power Save Status (Read-only)
This read-only status bit indicates the power save state of the memory controller and must be checked before turning off the MCLK source clock.
When this bit = 0, the memory controller is powered up.
When this bit = 1, the memory controller is powered down and the MCLK source can be turned off.

Note
Memory writes are possible during power save mode because the S1D13A04 dynamically enables the memory controller for display buffer writes.

bit 4 Power Save Mode Enable
When this bit = 1, the software initiated power save mode is enabled.
When this bit = 0, the software initiated power save mode is disabled.
At reset, this bit is set to 1. For a summary of Power Save Mode, see Section 15, “Power Save Mode” on page 163.

Note
Memory writes are possible during power save mode because the S1D13A04 dynamically enables the memory controller for display buffer writes.

Power Considerations:
The S1D13A04 may experience higher than normal Quiescent Current immediately after applying power. To prevent this condition, the following start up sequence must be followed:

1. Power-up/Reset the S1D13A04.
2. Initialize all registers.
3. Disable power save mode (set REG[14h] bit 4 to 0)

Note
By default, Power Save Mode is enabled (equal to 1) after power-up/Reset. If it is desirable/necessary to remain in power save mode for any length of time after power-up/Reset, the above described condition can be prevented by performing a R/W access to the embedded memory.

bit 0 ‘Direct’ HR-TFT LCD Interface GPO Control
This bit is for HR-TFT panels only. For all other panel types, this bit has no effect.
When the ‘direct’ HR-TFT LCD interface is selected (REG[0Ch] bits 1-0 = 10), the DRDY pin becomes a general purpose output (GPO). This GPO can be used to control the HR-TFT MOD signal.
When this bit = 0, DRDY (GPO) is forced low.
When this bit = 1, DRDY (GPO) is forced high.

8.3.4 Look-Up Table Registers

Look-Up Table Write Register REG[18h] Default = 00000000h Write Only															
LUT Write Address								LUT Red Write Data						n/a	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUT Green Write Data						n/a		LUT Blue Write Data						n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note
The S1D13A04 has three 256-position, 6-bit wide LUTs, one for each of red, green, and blue (see Section 12, "Look-Up Table Architecture" on page 149).

Note
This is a write-only register and returns 00h if read.

bits 31-24 LUT Write Address Bits [7:0]
These bits form a pointer into the Look-Up Table (LUT) which is used to write the LUT Red, Green, and Blue data. **When the S1D13A04 is set to a host bus interface using little endian (CNF4 = 0), the RGB data is updated to the LUT with the completion of a write to these bits.**

Note
When a value is written to the LUT Write Address Bits, the same value is automatically placed in the LUT Read Address Bits (REG[1Ch] bits 31-24).

bits 23-18 LUT Red Write Data Bits [5:0]
These bits contains the data to be written to the red component of the Look-Up Table. The LUT position is controlled by the LUT Write Address bits (bits 31-24).

bits 15-10 LUT Green Write Data Bits [5:0]
These bits contains the data to be written to the green component of the Look-Up Table. The LUT position is controlled by the LUT Write Address bits (bits 31-24).

bits 7-2 LUT Blue Write Data Bits [5:0]
These bits contains the data to be written to the blue component of the Look-Up Table. The LUT position is controlled by the LUT Write Address bits (bits 31-24). **When the S1D13A04 is set to a host bus interface using big endian (CNF4 = 1), the RGB data is updated to the LUT with the completion of a write to these bits.**

Look-Up Table Read Register															
REG[1Ch]			Default = 00000000h									Write Only (bits 31-24)/Read Only			
LUT Read Address (write only)								LUT Red Read Data						n/a	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUT Green Read Data						n/a		LUT Blue Read Data						n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note

The S1D13A04 has three 256-position, 6-bit wide LUTs, one for each of red, green, and blue (see Section 12, "Look-Up Table Architecture" on page 149).

bits 31-24 LUT Read Address Bits [7:0] **(Write Only)**
This register forms a pointer into the Look-Up Table (LUT) which is used to read LUT data. Red data is read from bits 23-18, green data from bits 15-10, and blue data from bits 7-2.

Note

If a write to the LUT Write Address Bits (REG[18h] bits 31-24) is made, the LUT Read Address bits are automatically updated with the same value.

bits 23-18 LUT Red Read Data Bits [5:0] **(Read Only)**
These bits point to the data from the red component of the Look-Up Table. The LUT position is controlled by the LUT Read Address bits (bits 31-24). This is a read-only register.

bits 15-10 LUT Green Read Data Bits [5:0] **(Read Only)**
These bits point to the data from the green component of the Look-Up Table. The LUT position is controlled by the LUT Read Address bits (bits 31-24). This is a read-only register.

bits 7-2 LUT Blue Read Data Bits [5:0] **(Read Only)**
These bits point to the data from the blue component of the Look-Up Table. The LUT position is controlled by the LUT Read Address bits (bits 31-24). This is a read-only register.

8.3.5 Display Mode Registers

Horizontal Total Register
REG[20h] Default = 00000000h Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a									Horizontal Total bits 6-0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 6-0 Horizontal Total Bits [6:0]
These bits specify the LCD panel Horizontal Total period, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display period and the Horizontal Non-Display period. Since the maximum Horizontal Total is 1024 pixels, the maximum panel resolution supported is 800x600.

REG[20h] bits 6:0 = (Horizontal Total in number of pixels ÷ 8) - 1

Note
[1] For all panels this register must be programmed such that:
HDPS + HDP < HT
HT - HDP ≥ 8MCLK
[2] For passive panels, this register must be programmed such that:
HPS + HPW < HT
[3] See Section 6.5, “Display Interface” on page 54.

Horizontal Display Period Register
REG[24h] Default = 00000000h Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a									Horizontal Display Period bits 6-0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 6-0 Horizontal Display Period Bits [6:0]
These bits specify the LCD panel Horizontal Display period, in 8 pixel resolution. The Horizontal Display period should be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display period.

REG[24h] bits 6:0 = (Horizontal Display Period in number of pixels ÷ 8) - 1

Note
For passive panels, HDP must be a minimum of 32 pixels and must be increased by multiples of 16.

For TFT panels, HDP must be a minimum of 8 pixels and must be increased by multiples of 8.

Note
See Section 6.5, “Display Interface” on page 54.

Horizontal Display Period Start Position Register
REG[28h] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						Horizontal Display Period Start Position bits 9-0									

bits 9-0 Horizontal Display Period Start Position Bits [9:0]
These bits specify a value used in the calculation of the Horizontal Display Period Start Position (in 1 pixel resolution) for TFT and 'direct' HR-TFT panels.

For passive LCD panels these bits must be set to 00h which will result in HDPS = 22.
HDPS = (REG[28h] bits 9-0) + 22

For TFT panels, HDPS is calculated using the following formula.
HDPS = (REG[28h] bits 9-0) + 5

Note
This register must be programmed such that the following formula is valid.
HDPS + HDP < HT

FPLINE Register
REG[2Ch] Default = 00000000h Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								FPLINE Polarity	FPLINE Pulse Width bits 6-0						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n/a						FPLINE Pulse Start Position bits 9-0									

bit 23 FPLINE Pulse Polarity
This bit selects the polarity of the horizontal sync signal. For passive panels, this bit must be set to 1. For TFT panels, this bit is set according to the horizontal sync signal of the panel (typically FPLINE or LP).
When this bit = 0, the horizontal sync signal is active low.
When this bit = 1, the horizontal sync signal is active high.

bits 22-16 FPLINE Pulse Width Bits [6:0]
These bits specify the width of the panel horizontal sync signal, in 1 pixel resolution. The horizontal sync signal is typically FPLINE or LP, depending on the panel type.

REG[2Ch] bits 22-16 = FPLINE Pulse Width in number of pixels - 1

Note
For passive panels, these bits must be programmed such that the following formula is valid.
HPW + HPS < HT

Note
See Section 6.5, "Display Interface" on page 54.

bits 9-0

FPLINE Pulse Start Position Bits [9:0]
These bits specify the start position of the horizontal sync signal, in 1 pixel resolution.

FPLINE Pulse Start Position in pixels = (REG[2Ch] bits 9-0) + 1

Note
For passive panels, these bits must be programmed such that the following formula is valid.
HPW + HPS < HT

Note
See Section 6.5, “Display Interface” on page 54.

Vertical Total Register
REG[30h] Default = 00000000h Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						Vertical Total bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0

Vertical Total Bits [9:0]
These bits specify the LCD panel Vertical Total period, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period. The maximum Vertical Total is 1024 lines.

REG[30h] bits 9:0 = Vertical Total in number of lines - 1

Note
[1] This register must be programmed such that the following formula is valid.
VDPS + VDP < VT
[2] See Section 6.5, “Display Interface” on page 54.

Vertical Display Period Register
REG[34h] Default = 00000000h Read/Write

n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						Vertical Display Period bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0

Vertical Display Period Bits [9:0]
These bits specify the LCD panel Vertical Display period, in 1 line resolution. The Vertical Display period should be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

REG[34h] bits 9:0 = Vertical Display Period in number of lines - 1

Note
[1]This register must be programmed such that the following formula is valid.
VDPS + VDP < VT
[2]See Section 6.5, “Display Interface” on page 54.

Vertical Display Period Start Position Register															
REG[38h]			Default = 00000000h											Read/Write	
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						Vertical Display Period Start Position bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0 Vertical Display Period Start Position Bits [9:0]
These bits specify the Vertical Display Period Start Position for panels in 1 line resolution.

For passive LCD panels these bits must be set to 00h.

For TFT panels, VDPS is calculated using the following formula.
VDPS = REG[38h] bits 9-0

Note
[1]This register must be programmed such that the following formula is valid.
VDPS + VDP < VT
[2]See Section 6.5, “Display Interface” on page 54.

FPFRAME Register															
REG[3Ch]			Default = 00000000h											Read/Write	
n/a								FPFRAME Polarity	n/a				FPFRAME Pulse Width bits 2-0		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						FPFRAME Pulse Start Position bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bit 23 FPFRAME Pulse Polarity
This bit selects the polarity of the vertical sync signal. For passive panels, this bit must be set to 1. For TFT panels, this bit is set according to the horizontal sync signal of the panel (typically FPFRAME, SPS or DY).
When this bit = 0, the vertical sync signal is active low.
When this bit = 1, the vertical sync signal is active high.

bits 18-16 FPFRAME Pulse Width Bits [2:0]
These bits specify the width of the panel vertical sync signal, in 1 line resolution. The vertical sync signal is typically FPFRAME, SPS or DY, depending on the panel type.

REG[3Ch] bits 18-16 = FPFRAME Pulse Width in number of lines - 1

Note
See Section 6.5, “Display Interface” on page 54.

bits 9-0 — FPFRAME Pulse Start Position Bits [9:0]
These bits specify the start position of the vertical sync signal, in 1 line resolution.

For passive panels, these bits must be set to 00h.

For TFT panels, VDPS is calculated using the following formula.
VPS = REG[3Ch] bits 9-0

Note
See Section 6.5, "Display Interface" on page 54.

Main Window Display Start Address Register REG[40h] Default = 00000000h Read/Write															
n/a															bit 16
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Main Window Display Start Address bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 16-0 — Main Window Display Start Address Bits [16:0]
This register specifies the starting address, in DWORDS, for the LCD image in the display buffer for the main window.

Note that this is a double-word (32-bit) address. An entry of 00000h into these registers represents the first double-word of display memory, an entry of 00001h represents the second double-word of the display memory, and so on. Calculate the Display Start Address as follows:

REG[40h] bits 16:0 = image address ÷ 4 (valid only for SwivelView 0°)

Note
For information on setting this register for other SwivelView orientations, see Section 13, "SwivelView™" on page 155.

Main Window Line Address Offset Register REG[44h] Default = 00000000h Read/Write															
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						Main Window Line Address Offset bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0 — Main Window Line Address Offset Bits [9:0]
This register specifies the offset, in DWORDS, from the beginning of one display line to the beginning of the next display line in the main window. **Note that this is a 32-bit address increment.** Calculate the Line Address Offset as follows:

REG[44h] bits 9:0 = display width in pixels ÷ (32 ÷ bpp)

Note
A virtual display can be created by programming this register with a value greater than the formula requires. When a virtual display is created the image width is larger than the display width and the displayed image becomes a window into the larger virtual image.

8.3.6 Picture-in-Picture Plus (PIP$^+$) Registers

PIP$^+$ Display Start Address Register REG[50h] Default = 00000000h Read/Write															
n/a															bit 16
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIP$^+$ Display Start Address bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 16-0 PIP$^+$ Display Start Address Bits [16:0]
These bits form the 17-bit address for the starting double-word of the PIP+ window.

Note that this is a double-word (32-bit) address. An entry of 00000h into these registers represents the first double-word of display memory, an entry of 00001h represents the second double-word of the display memory, and so on.

Note
These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[10h] bit 19).

PIP$^+$ Line Address Offset Register REG[54h] Default = 00000000h Read/Write															
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						PIP$^+$ Line Address Offset bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0 PIP$^+$ Window Line Address Offset Bits [9:0]
These bits are the LCD display's 10-bit address offset from the starting double-word of line "n" to the starting double-word of line "n + 1" for the PIP$^+$window. **Note that this is a 32-bit address increment.**

Note
These bits have no effect unless the PIP$^+$ Window Enable bit is set to 1 (REG[10h] bit 19).

PIP+ X Positions Register REG[58h] Default = 00000000h Read/Write															
n/a						PIP+ X End Position bits 9-0									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						PIP+ X Start Position bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note

The effect of REG[58h] through REG[5Ch] takes place only after REG[5Ch] is written and at the next vertical non-display period.

bits 25-16 PIP+ Window X End Position Bits [9:0]

These bits determine the X end position of the PIP+ window in relation to the origin of the panel. Due to the S1D13A04 SwivelView feature, the X end position may not be a horizontal position value (only true in 0° and 180° SwivelView). For further information on defining the value of the X End Position register, see Section 14, “Picture-in-Picture Plus (PIP+)” on page 160.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the X end position is incremented by *x* pixels where *x* is relative to the current color depth.

Table 8-11: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (x)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

For 90° and 270° SwivelView the X end position is incremented in 1 line increments.

Depending on the color depth, some of the higher bits in this register are unused because the maximum horizontal display width is 1024 pixels.

Note

These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[10h] bit 19).

bits 9-0

PIP+ Window X Start Position Bits [9:0]
These bits determine the X start position of the PIP+ window in relation to the origin of the panel. Due to the S1D13A04 SwivelView feature, the X start position may not be a horizontal position value (only true in 0° and 180° SwivelView). For further information on defining the value of the X Start Position register, see Section 14, “Picture-in-Picture Plus (PIP+)” on page 160.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the X start position is incremented by *x* pixels where *x* is relative to the current color depth.

Table 8-12: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (x)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

For 90° and 270° SwivelView the X start position is incremented in 1 line increments.

Depending on the color depth, some of the higher bits in this register are unused because the maximum horizontal display width is 1024 pixels.

Note

These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[10h] bit 19).

PIP+ Y Positions Register REG[5Ch] Default = 00000000h Read/Write															
n/a						PIP+ Y End Position bits 9-0									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						PIP+ Y Start Position bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note

1 The effect of REG[58h] through REG[5Ch] takes place only after REG[5Ch] is written and at the next vertical non-display period.

2 For host bus interfaces using little endian (CNF4 = 0), a write to bits 31-24 causes the PIP+ Window Y End Position to take effect.
For host bus interfaces using big endian (CNF4 = 1), a write to bits 7-0 causes the PIP+ Window Y End Position to take effect.

bits 25-16 PIP+ Window Y End Position Bits [9:0]
These bits determine the Y end position of the PIP+ window in relation to the origin of the panel. Due to the S1D13A04 SwivelView feature, the Y end position may not be a vertical position value (only true in 0° and 180° SwivelView). For further information on defining the value of the Y End Position register, see Section 14, “Picture-in-Picture Plus (PIP+)” on page 160.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the Y end position is incremented in 1 line increments. For 90° and 270° SwivelView the Y end position is incremented by *y* pixels where *y* is relative to the current color depth.

Table 8-13: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (y)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

Depending on the color depth, some of the higher bits in this register are unused because the maximum vertical display height is 1024 pixels.

Note

These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[10h] bit 19).

bits 9-0

PIP$^+$ Window Y Start Position Bits [9:0]
These bits determine the Y start position of the PIP$^+$ window in relation to the origin of the panel. Due to the S1D13A04 SwivelView feature, the Y start position may not be a vertical position value (only true in 0° and 180° SwivelView). For further information on defining the value of the Y Start Position register, see Section 14, “Picture-in-Picture Plus (PIP+)” on page 160.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the Y start position is incremented in 1 line increments. For 90° and 270° SwivelView the Y start position is incremented by *y* pixels where *y* is relative to the current color depth.

Table 8-14: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (y)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

Depending on the color depth, some of the higher bits in this register are unused because the maximum vertical display height is 1024 pixels.

Note

These bits have no effect unless the PIP$^+$ Window Enable bit is set to 1 (REG[10h] bit 19).

8.3.7 Miscellaneous Registers

Special Purpose Register REG[60h] Default = 00000000h Read/Write															
n/a								Reserved							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								2D Byte Swap	Display Data Word Swap	Display Data Byte Swap	n/a		Latch Byte Select	n/a	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 23-16 Reserved.
These bits must be set to 0.

bit 7 2D Byte Swap
This bit enables the word data sent to/read from the 2D BitBLT port to be swapped (byte 0 and byte 1 are swapped).

Note
This bit is only used when the S1D13A04 is configured for Big Endian (CNF4 = 1 at RESET#). If configured for Little Endian (CNF4 = 0), this bit has no effect.

bit 6 Display Data Word Swap
The display pipe fetches 32-bits of data from the display buffer. This bit enables the lower 16-bit word and the upper 16-bit word to be swapped before sending them to the LCD display. If the Display Data Byte Swap bit is also enabled, then the byte order of the fetched 32-bit data is reversed.

Note
This bit is only used when the S1D13A04 is configured for Big Endian (CNF4 = 1 at RESET#). If configured for Little Endian (CNF4 = 0), this bit has no effect.

bit 5

Display Data Byte Swap
The display pipe fetches 32-bit of data from the display buffer. This bit enables byte 0 and byte 1 to be swapped, and byte 2 and byte 3 to be swapped, before sending them to the LCD display. If the Display Data Word Swap bit is also enabled, then the byte order of the fetched 32-bit data is reversed.

Note
This bit is only used when the S1D13A04 is configured for Big Endian (CNF4 = 1 at RESET#). If configured for Little Endian (CNF4 = 0), this bit has no effect.

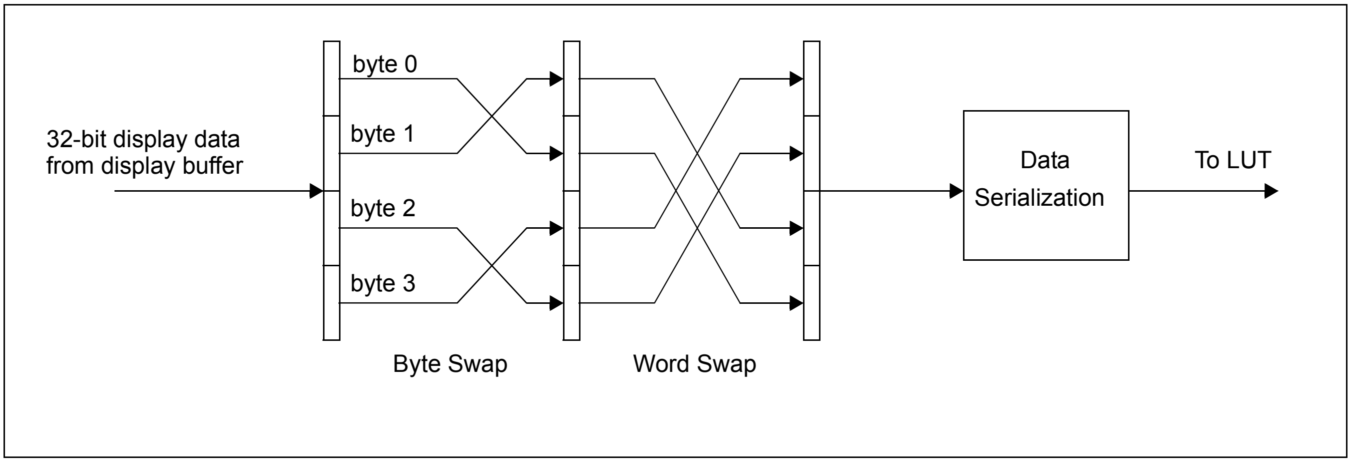


Figure 8-1: Display Data Byte/Word Swap

bit 2

Latch Byte Select
When this bit = 1, REG[5Ch] is latched in reverse order.
When this bit = 0, there is no hardware effect.

GPIO Status and Control Register															
REG[64h]			Default = 20000000h											Read/Write	
GPIO7 Input Enable	GPIO6 Input Enable	GPIO5 Input Enable	GPIO4 Input Enable	GPIO3 Input Enable	GPIO2 Input Enable	GPIO1 Input Enable	GPIO0 Input Enable	GPIO7 Config	GPIO6 Config	GPIO5 Config	GPIO4 Config	GPIO3 Config	GPIO2 Config	GPIO1 Config	GPIO0 Config
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note
The GPIO pins default as inputs after power-up and must be configured using the bits in this register.

Note
For information on GPIO pin mapping when the 'direct' HR-TFT LCD interface is selected, see Table 4-9: "LCD Interface Pin Mapping," on page 28.

bits 31-24 GPIO[7:0] Pin Input Enable bits
These bits are used to enable the input function of each GPIO pin. They must be changed to a 1 after power-on reset to enable the input function of the corresponding GPIO pin (default is 0).

Note
The default for GPIO5 Pin Input Enable is 1.

bits 23-16 GPIO[7:0] Pin IO Configuration
When this bit = 0 (default), the corresponding GPIO pin is configured as an input pin.
When this bit = 1, the corresponding GPIO pin is configured as an output pin.

Note
The input function of each GPIO pin must be enabled using the GPIO[7:0] Pin Input Enable bits (bits 31-24) before the input configuration takes effect.

bit 7 GPIO7 Pin IO Status
When GPIO7 is configured as an output, writing a 1 to this bit drives GPIO7 high and writing a 0 to this bit drives GPIO7 low.
When GPIO7 is configured as an input, a read from this bit returns the status of GPIO7.

bit 6 GPIO6 Pin IO Status
When GPIO6 is configured as an output, writing a 1 to this bit drives GPIO6 high and writing a 0 to this bit drives GPIO6 low.
When GPIO6 is configured as an input, a read from this bit returns the status of GPIO6.

bit 5 GPIO5 Pin IO Status
When GPIO5 is configured as an output, writing a 1 to this bit drives GPIO5 high and writing a 0 to this bit drives GPIO5 low.
When GPIO5 is configured as an input, a read from this bit returns the status of GPIO5.

bit 4	GPIO4 Pin IO Status When GPIO4 is configured as an output, writing a 1 to this bit drives GPIO4 high and writing a 0 to this bit drives GPIO4 low. When GPIO4 is configured as an input, a read from this bit returns the status of GPIO4.
bit 3	GPIO3 Pin IO Status When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO3 is configured as an output, writing a 1 to this bit drives GPIO3 high and writing a 0 to this bit drives GPIO3 low. When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO3 is configured as an input, a read from this bit returns the status of GPIO3. When the ‘Direct’ HR-TFT LCD interface is enabled (REG[0Ch] bits 1:0 = 10), GPIO0 outputs the SPL signal automatically and writing to this bit has no effect.
bit 2	GPIO2 Pin IO Status When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO2 is configured as an output, writing a 1 to this bit drives GPIO2 high and writing a 0 to this bit drives GPIO2 low. When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO2 is configured as an input, a read from this bit returns the status of GPIO2. When the ‘Direct’ HR-TFT LCD interface is enabled (REG[0Ch] bits 1:0 = 10), GPIO0 outputs the REV signal automatically and writing to this bit has no effect.
bit 1	GPIO1 Pin IO Status When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO1 is configured as an output, writing a 1 to this bit drives GPIO1 high and writing a 0 to this bit drives GPIO1 low. When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO1 is configured as an input, a read from this bit returns the status of GPIO1. When the ‘Direct’ HR-TFT LCD interface is enabled (REG[0Ch] bits 1:0 = 10), GPIO0 outputs the CLS signal automatically and writing to this bit has no effect.
bit 0	GPIO0 Pin IO Status When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO0 is configured as an output, writing a 1 to this bit drives GPIO0 high and writing a 0 to this bit drives GPIO0 low. When the ‘Direct’ HR-TFT LCD interface is not selected (REG[0Ch] bits 1:0) and GPIO0 is configured as an input, a read from this bit returns the status of GPIO0. When the ‘Direct’ HR-TFT LCD interface is enabled (REG[0Ch] bits 1:0 = 10), GPIO0 outputs the PS signal automatically and writing to this bit has no effect.

PWM Clock Configuration Register															
REG[70h]				Default = 00000000h										Read/Write	
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a								PWM Clock Divide Select bits 3-0				PWM Clock Force High	PWMCLK Source Select bits 1-0		PWM Clock Enable
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

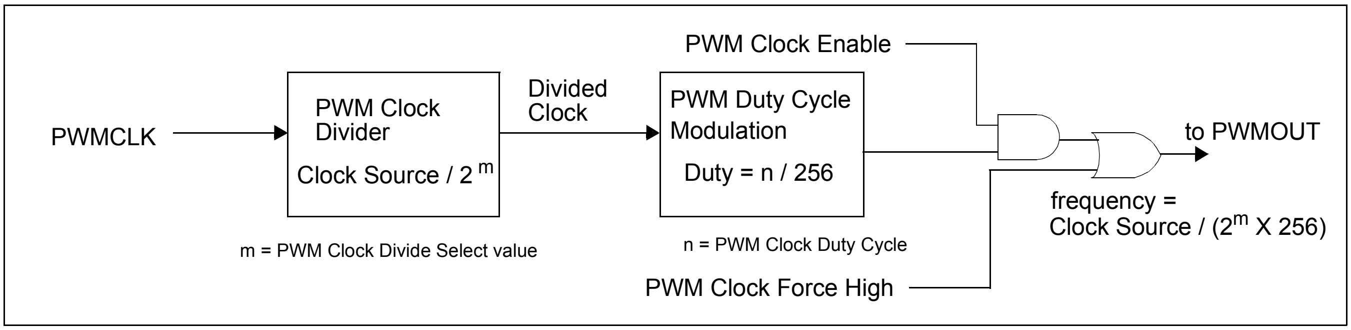


Figure 8-2: PWM Clock Block Diagram

Note

For further information on PWMCLK, see Section 7.1.4, “PWMCLK” on page 85.

bits 7-4 PWM Clock Divide Select Bits [3:0]
The value of these bits represents the power of 2 by which the selected PWM clock source is divided.

Table 8-15: PWM Clock Divide Select Options

PWM Clock Divide Select Bits [3:0]	PWM Clock Divide Amount
0h	1
1h	2
2h	4
3h	8
4h	16
5h	32
6h	64
7h	128
8h	256
9h	512
Ah	1024
Bh	2048
Ch	4096
Dh	8192
Eh	16384
Fh	32768

Note

This divided clock is further divided by 256 before it is output at PWMOUT.

bit 3 PWM Clock Force High
When this bit = 0, the PWMOUT pin function is controlled by the PWM Clock enable bit.
When this bit = 1, the PWMOUT pin is forced to high.

bit 1 PWMCLK Source Select Bits [1:0]
These bits determine the source of PWMCLK.

Table 8-16: PWMCLK Source Selection

PWMCLK Source Select Bits	PWMCLK Source
00	CLKI
01	CLKI2
10	BCLK
11	PCLK

Note
For further information on the PWMCLK source select, see Section 7.2, "Clock Selection" on page 86.

bit 0 PWM Clock Enable
When this bit = 0, PWMOUT output acts as a general purpose output pin controllable by bit 3 of REG[70h].
When this bit = 1, the PWM Clock circuitry is enabled.

Note
The PWM Clock circuitry is disabled when Power Save Mode is enabled.

PWMOUT Duty Cycle Register							
REG[74h]	Default = 00000000h						Read/Write
n/a							
31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PWMOUT Duty Cycle bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PWMOUT Duty Cycle Bits [7:0]
This register determines the duty cycle of the PWMOUT output.

Table 8-17: PWMOUT Duty Cycle Select Options

PWMOUT Duty Cycle [7:0]	PWMOUT Duty Cycle
00h	Always Low
01h	High for 1 out of 256 clock periods
02h	High for 2 out of 256 clock periods
...	...
FFh	High for 255 out of 256 clock periods

Scratch Pad A Register REG[80h] Default = not applicable Read/Write															
Scratch Pad A bits 31-24															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Scratch Pad A bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 31-0 Scratch Pad A Bits [31:0]
This register contains general purpose read/write bits. These bits have no effect on hardware.

Note
The contents of the Scratch Pad A register defaults to an un-defined state after initial power-up. Any data written to this register remains intact when the S1D13A04 is reset, **as long as the chip is not powered off**.

Scratch Pad B Register REG[84h] Default = not applicable Read/Write															
Scratch Pad B bits 31-24															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Scratch Pad B bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 31-0 Scratch Pad B Bits [31:0]
This register contains general purpose read/write bits. These bits have no effect on hardware.

Note
The contents of the Scratch Pad B register defaults to an un-defined state after initial power-up. Any data written to this register remains intact when the S1D13A04 is reset, **as long as the chip is not powered off**.

Scratch Pad C Register															
REG[88h]			Default = not applicable											Read/Write	
Scratch Pad C bits 31-24															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Scratch Pad C bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 31-0 Scratch Pad C Bits [31:0]
This register contains general purpose read/write bits. These bits have no effect on hardware.

Note
The contents of the Scratch Pad C register defaults to an un-defined state after initial power-up. Any data written to this register remains intact when the S1D13A04 is reset, **as long as the chip is not powered off**.

8.4 USB Registers (Offset = 4000h)

The S1D13A04 USB device occupies a 48 byte local register space which can be accessed by the CPU on the local host interface.

To access the USB registers:

1. A valid USBCLK must be provided.
2. The USBClk Enable bit (REG[4000h] bit 7) must be set to 1 and the USB Setup bit (REG[4000h] bit 2) must be set to 1. Both bits should be set together.

If any of the above conditions are not true, the USB registers must not be accessed.

Control Register REG[4000h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
USBClk Enable	Software EOT	USB Enable	Endpoint 4 Stall	Endpoint 3 Stall	USB Setup	Reserved	Reserved
7	6	5	4	3	2	1	0

bit 7 USBClk Enable.
This bit allows the USBClk to be enabled/disabled allowing the S1D13A04 to save power when the USBClk is not required. This bit should be initially set with the USB Setup bit. However, it can be disabled/re-enabled individually.
When this bit = 1, the USBClk is enabled.
When this bit = 0, the USBClk is disabled.

Note
The USB Registers must not be accessed when this bit is 0.

bit 6 Software EOT
This bit determines the response to an IN request to Endpoint 4 when the transmit FIFO is empty. If this bit is asserted, the S1D13A04 responds to an IN request to Endpoint 4 with an ACK and a zero length packet if the FIFO is empty. If this bit is not asserted, the S1D13A04 responds to an IN request from Endpoint 4 with an NAK if the FIFO is empty, indicating that it expects to transmit more data. This bit is automatically cleared when the S1D13A04 responds to the host with a zero length packet when the FIFO is empty.

bit 5 USB Enable
Any device or configuration descriptor reads from the host will be acknowledged with a NAK until this bit is set. This allows time for the local CPU to set up the interrupt polling register, maximum packet size registers, and other configuration registers (e.g. Product ID and Vendor ID) before the host reads the descriptors.

Note
As the device and configuration descriptors cannot be read by the host until the USB Enable bit is set, the device enumeration process will not complete and the device will not be recognized on the USB.

bit 4 Endpoint 4 Stall.
If this bit is set, host bulk reads from the transmit FIFO will result in a STALL acknowledge by the S1D13A04. No data will be returned to the USB host.

bit 3 Endpoint 3 Stall.
If this bit is set, host bulk writes to the receive FIFO will result in a STALL acknowledge by the S1D13A04. Receive data will be discarded.

bit 2 USB Setup
This bit is used by software to select between GPIO and USB functions for multifunction GPIO pins (GPIO[7:4]). This bit should be set at the same time as the USBClk Enable bit.
When this bit = 1, the USB function is selected.
When this bit = 0, the GPIO function is selected.

Note
The USB Registers must not be accessed when this bit is 0.

bit 1 Reserved.
This bit must be set to 0.

bit 0 Reserved.
This bit must be set to 0.

Interrupt Enable Register 0 REG[4002h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
Suspend Request Interrupt Enable	SOF Interrupt Enable	reserved	Endpoint 4 Interrupt Enable	Endpoint 3 Interrupt Enable	Endpoint 2 Interrupt Enable	Endpoint 1 Interrupt Enable	n/a
7	6	5	4	3	2	1	0

bit 7 Suspend Request Interrupt Enable.
When set, this bit enables an interrupt to occur when the USB host is requesting the S1D13A04 USB device to enter suspend mode.

bit 6 SOF Interrupt Enable.
When set, this bit enables an interrupt to occur when a start-of-frame packet is received by the S1D13A04.

bit 5 Reserved.
This bit must be set to 0.

bit 4 Endpoint 4 Interrupt Enable.
When set, this bit enables an interrupt to occur when a USB Endpoint 4 Data Packet has been sent by the S1D13A04.

bit 3 Endpoint 3 Interrupt Enable.
When set, this bit enables an interrupt to occur when a USB Endpoint 3 Data Packet has been received by the S1D13A04.

bit 2 Endpoint 2 Interrupt Enable.
When set, this bit enables an interrupt to occur when the USB Endpoint 2 Transmit Mailbox registers have been read by the USB host.

bit 1 Endpoint 1 Interrupt Enable.
When set, this bit enables an interrupt to occur when the USB Endpoint 1 Receive Mailbox registers have been written to by the USB host.

Interrupt Status Register 0
REG[4004h] Default = 00h Read/Write

15	14	13	12	11	10	9	8
n/a							
Suspend Request Interrupt Status	SOF Interrupt Status	Reserved	Endpoint 4 Interrupt Status	Endpoint 3 Interrupt Status	Endpoint 2 Interrupt Status	Endpoint 1 Interrupt Status	Upper Interrupt Active (read only)
7	6	5	4	3	2	1	0

bit 7 Suspend Request Interrupt Status.
This bit indicates when a suspend-request has been received by the S1D13A04. Writing a 1 clears this bit.

bit 6 SOF Interrupt Status.
This bit indicates when a start-of-frame packet has been received by the S1D13A04. Writing a 1 clears this bit.

bit 5 Reserved.
This bit must be set to 0.

bit 4 Endpoint 4 Interrupt Status.
This bit indicates when a USB Endpoint 4 Data packet has been sent by the S1D13A04. Writing a 1 clears this bit.

bit 3 Endpoint 3 Interrupt Status (Receive FIFO Valid).
This bit indicates when a USB Endpoint 3 Data packet has been received by the S1D13A04. No more packets to endpoint 3 will be accepted until this bit is cleared. Writing a 1 clears this bit.

bit 2 Endpoint 2 Interrupt Status.
This bit indicates when the USB Endpoint 2 Mailbox registers have been read by the USB host. Writing a 1 clears this bit.

bit 1 Endpoint 1 Interrupt Status (Receive Mailbox Valid).
This bit indicates when the USB Endpoint 1 Mailbox registers have been written to by the USB host. Writing a 1 clears this bit.

bit 0 Upper Interrupt Active (read only).
At least one interrupt status bit is set in register REG[4008h].

Interrupt Enable Register 1
REG[4006h] Default = 00h Read/Write

15	14	13	12	11	10	9	8
n/a							
n/a						Transmit FIFO Almost Empty Interrupt Enable	Receive FIFO Almost Full Interrupt Enable
7	6	5	4	3	2	1	0

bit 1 Transmit FIFO Almost Empty Interrupt Enable.
When set, this bit enables an interrupt to be generated when the Transmit FIFO Almost Empty status bit is set.

Note
The Transmit FIFO Almost Empty threshold must be set greater than zero, as the FIFO count must drop below the threshold to cause an interrupt.

bit 0 Receive FIFO Almost Full Interrupt Enable.
When set, this bit enables an interrupt to be generated when the Receive FIFO Almost Full status bit is set.

Note
The Receive FIFO Almost Full threshold must be set less than 64, as the FIFO count must rise above the threshold to cause an interrupt.

Interrupt Status Register 1 REG[4008h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a						Transmit FIFO Almost Empty Status	Receive FIFO Almost Full Status
7	6	5	4	3	2	1	0

bit 1 Transmit FIFO Almost Empty Status.
This bit is set when the number of bytes in the Transmit FIFO is equal to the Transmit FIFO Almost Empty Threshold, and another byte is sent to the USB bus from the FIFO. Writing a 1 clears this bit.

bit 0 Receive FIFO Almost Full Status.
This bit is set when the number of bytes in the Receive FIFO is equal to the Receive FIFO Almost Full Threshold, and another byte is received from the USB bus into the FIFO. Writing a 1 clears this bit.

Endpoint 1 Index Register REG[4010h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a					Endpoint 1 Index bits 2-0 (RO)		
7	6	5	4	3	2	1	0

bits 2-0 Endpoint 1 Index Register Bits [2:0].
This register determines which Endpoint 1 Receive Mailbox is accessed when the Endpoint 1 Receive Mailbox Data register is read. This register is automatically incremented after the Endpoint 1 Receive Mailbox Data register is read. This index register wraps around to zero when it reaches the maximum count (7).

Endpoint 1 Receive Mailbox Data Register REG[4012h] Default = 00h Read Only							
n/a							
15	14	13	12	11	10	9	8
Endpoint 1 Receive Mailbox Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Endpoint 1 Receive Mailbox Data Bits [7:0].
This register is used to read data from one of the receive mailbox registers. Data is returned from the register selected by the Endpoint 1 Index Register. The eight receive mailbox registers are written by a USB bulk transfer to endpoint 1, and can be used to pass messages from the USB host to the local CPU. The format and content of the messages are user defined. If enabled, USB writes to this register can generate an interrupt.

Endpoint 2 Index Register							
REG[4018h]	Default = 00h						Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a					Endpoint 2 Index bits 2-0		
7	6	5	4	3	2	1	0

bits 2-0 Endpoint 2 Index Register Bits [2:0].
This register determines which Endpoint 2 Transmit Mailbox is accessed when the Endpoint 2 Transmit Mailbox Data register is read or written. This register is automatically incremented after the Endpoint 2 Transmit Mailbox Data port is read or written. This index register wraps around to zero when it reaches the maximum count (7).

Endpoint 2 Transmit Mailbox Data Register							
REG[401Ah]	Default = 00h						Read/Write
n/a							
15	14	13	12	11	10	9	8
Endpoint 2 Transmit Mailbox Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Endpoint 2 Transmit Mailbox Data Bits [7:0].
This register is used to read or write one of the transmit mailbox registers. The register being accessed is selected by the Endpoint 2 Index register. The eight Transmit Mailbox registers are written by the local CPU and are read by a USB transfer from endpoint 2. The format and content of the messages are user defined. If enabled, USB reads from this register can generate an interrupt.

Endpoint 2 Interrupt Polling Interval Register							
REG[401Ch]	Default = FFh						Read/Write
n/a							
15	14	13	12	11	10	9	8
Interrupt Polling Interval bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Interrupt Polling Interval Bits [7:0].
This register specifies the Endpoint 2 interrupt polling interval in milliseconds. It can be read by the host through the endpoint 2 descriptor.

Endpoint 3 Receive FIFO Data Register							
REG[4020h]	Default = 00h						Read Only
n/a							
15	14	13	12	11	10	9	8
Endpoint 3 Receive FIFO Data bits 7-0							
7	6	5	4	3	2	1	0

bits7-0 Endpoint 3 Receive FIFO Data Bits [7:0].
This register is used by the local CPU to read USB receive FIFO data. The FIFO data is written by the USB host using bulk or isochronous transfers to endpoint 3.

Endpoint 3 Receive FIFO Count Register REG[4022h] Default = 00h Read Only							
n/a							
15	14	13	12	11	10	9	8
Receive FIFO Count bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Receive FIFO Count Bits [7:0].
This register returns the number of receive FIFO entries containing valid entries. Values range from 0 (empty) to 64 (full).

Endpoint 3 Receive FIFO Status Register REG[4024h] Default = 01h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a			Receive FIFO Flush	Receive FIFO Overflow	Receive FIFO Underflow	Receive FIFO Full (read only)	Receive FIFO Empty (read only)
7	6	5	4	3	2	1	0

bit 4 Receive FIFO Flush
Writing to this bit causes the receive FIFO to be flushed. Reading this bit always returns a 0.

bit 3 Receive FIFO Overflow
If set, this bit indicates that an attempt was made by the USB host to write to the receive FIFO when the receive FIFO was full. Writing a 1 clears this bit.

bit 2 Receive FIFO Underflow
If set, this bit indicates that an attempt was made to read the receive FIFO when the receive FIFO was empty. Writing a 1 clears this bit.

bit 1 Receive FIFO Full
If set, this bit indicates that the receive FIFO is full.

bit 0 Receive FIFO Empty
If set, this bit indicates that the receive FIFO is empty.

Endpoint 3 Maximum Packet Size Register REG[4026h] Default = 08h Read/Write							
n/a							
15	14	13	12	11	10	9	8
Endpoint 3 Max Packet Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Endpoint 3 Max Packet Size Bits [7:0].
This register specifies the maximum packet size for endpoint 3 in units of 8 bytes (default = 64 bytes). It can be read by the host through the endpoint 3 descriptor.

Endpoint 4 Transmit FIFO Data Register							
REG[4028h]	Default = 00h						Write Only
n/a							
15	14	13	12	11	10	9	8
Transmit FIFO Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Transmit FIFO Data Bits [7:0].
This register is used by the local CPU to write data to the transmit FIFO. The FIFO data is read by the USB host using bulk or isochronous transfers from endpoint 4.

Endpoint 4 Transmit FIFO Count Register							
REG[402Ah]	Default = 00h						Read Only
n/a							
15	14	13	12	11	10	9	8
Transmit FIFO Count bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Transmit FIFO Count Bits [7:0].
This register returns the number of transmit FIFO entries containing valid entries. Values range from 0 (empty) to 64 (full).

Endpoint 4 Transmit FIFO Status Register							
REG[402Ch]	Default = 01h						Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a		Transmit FIFO Valid	Transmit FIFO Flush	Transmit FIFO Overflow	Reserved	Transmit FIFO Full (read only)	Transmit FIFO Empty (read only)
7	6	5	4	3	2	1	0

bit 5 Transmit FIFO Valid.
If set, this bit allows the data in the Transmit FIFO to be read by the next read from the host. This bit is automatically cleared by a host read. This bit is only used if bit 0 in USB[403Ah] Index [0Ch] is set.

bit 4 Transmit FIFO Flush.
Writing to this bit causes the transmit FIFO to be flushed. Reading this bit always returns a 0.

bit 3 Transmit FIFO Overflow.
If set, this bit indicates that an attempt was made by the local CPU to write to the transmit FIFO when the transmit FIFO was full. Writing a 1 clears this bit.

bit 2 Reserved.

bit 1 Transmit FIFO Full (read only).
If set, this bit indicates that the transmit FIFO is full.

bit 0 Transmit FIFO Empty (read only).
If set, this bit indicates that the transmit FIFO is empty.

Endpoint 4 Maximum Packet Size Register REG[402Eh] Default = 08h Read/Write							
n/a							
15	14	13	12	11	10	9	8
Endpoint 4 Max Packet Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Endpoint 4 Max Packet Size Bits [7:0].
This register specifies the maximum packet size for endpoint 4 in units of 8 bytes (default = 64 bytes). It can be read by the host through the endpoint 4 descriptor.

Revision Register REG[4030h] Default = 01h Read Only							
n/a							
15	14	13	12	11	10	9	8
Chip Revision bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Chip Revision Bits [7:0].
This register returns current silicon revision number of the USB client.

USB Status Register REG[4032h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
Suspend Control	USB Endpoint 4 STALL	USB Endpoint 4 NAK	USB Endpoint 4 ACK	USB Endpoint 3 STALL	USB Endpoint 3 NAK	USB Endpoint 3 ACK	Endpoint 2 Valid
7	6	5	4	3	2	1	0

bit 7 Suspend Control.
If set, this bit indicates that there is a pending suspend request. Writing a 1 clears this bit and causes the S1D13A04 USB device to enter suspended mode.

bit 6 USB Endpoint 4 STALL.
The last USB IN token could not be serviced because the endpoint was stalled (REG[4000h] bit 4 set), and was acknowledged with a STALL. Writing a 1 clears this bit.

bit 5 USB Endpoint 4 NAK.
The last USB packet transmitted (IN packet) encountered a FIFO underrun condition, and was acknowledged with a NAK. Writing a 1 clears this bit.

bit 4 USB Endpoint 4 ACK.
The last USB packet transmitted (IN packet) was successfully acknowledged with an ACK from the USB host. Writing a 1 clears this bit.

bit 3 USB Endpoint 3 STALL.
The last USB packet received (OUT packet) could not be accepted because the endpoint was stalled (REG[4000h] bit 3 set), and was acknowledged with a STALL. Writing a 1 clears this bit.

bit 2 USB Endpoint 3 NAK.
The last USB packet received (OUT packet) could not be accepted, and was acknowledged with a NAK. Writing a 1 clears this bit.

bit 1 USB Endpoint 3 ACK.
The last USB packet received (OUT packet) was successfully acknowledged with an ACK. Writing a 1 clears this bit.

bit 0 Endpoint 2 Valid.
When this bit is set, the 8-byte endpoint 2 mailbox registers have been written by the local CPU, but not yet read by the USB host. The local CPU should not write into these registers while this bit is set.

Frame Counter MSB Register							
REG[4034h]	Default = 00h						Read Only
n/a							
15	14	13	12	11	10	9	8
n/a					Frame Counter bits 10-8		
7	6	5	4	3	2	1	0

Frame Counter LSB Register							
REG[4036h]	Default = 00h						Read Only
n/a							
15	14	13	12	11	10	9	8
Frame Counter bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 Frame Counter Bits [10:0]
This register contains the frame counter from the most recent start-of-frame packet.

Extended Register Index							
REG[4038h]	Default = 00h						Read/Write
n/a							
15	14	13	12	11	10	9	8
Extended Register Index bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Extended Register Index Bits [7:0]
This register selects which extended data register is accessed when the REG[403Ah] is read or written.

Extended Register Data							
REG[403Ah]	Default = 04h						Read/Write
n/a							
15	14	13	12	11	10	9	8
Extended Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Extended Data Bits [7:0]
This port provides access to one of the extended data registers. The index of the current register is held in REG[4038h].

Vendor ID MSB REG[403Ah], Index[00h]			Default = 04h				Read/Write
Vendor ID bits 15-8							
7	6	5	4	3	2	1	0

Vendor ID LSB REG[403Ah], Index[01h]			Default = B8h				Read/Write
Vendor ID bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Vendor ID Bits [15:0]
These registers determine the Vendor ID returned in a “Get Device Descriptor” request.

Product ID MSB REG[403Ah], Index[02h]			Default = 88h				Read/Write
Product ID bits 15-8							
7	6	5	4	3	2	1	0

Product ID LSB REG[403Ah], Index[03h]			Default = 21h				Read/Write
Product ID bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Product ID Bits [15:0]
These registers determine the Product ID returned in a “Get Device Descriptor” request.

Release Number MSB REG[403Ah], Index[04h]			Default = 01h				Read/Write
Release Number bits 15-8							
7	6	5	4	3	2	1	0

Release Number LSB REG[403Ah], Index[05h]			Default = 00h				Read/Write
Release Number bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Release Number Bits [15:0]
These registers determine the device release number returned in a “Get Device Descriptor” request.

Receive FIFO Almost Full Threshold REG[403Ah], Index[06h] Default = 3Ch Read/Write							
n/a		Receive FIFO Almost Full Threshold bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 Receive FIFO Almost Full Threshold Bits [5:0]
This register determines the threshold at which the receive FIFO almost full status bit is set.

Note
The Receive FIFO Almost Full threshold must be set less than 64, as the FIFO count must rise above the threshold to cause an interrupt.

Transmit FIFO Almost Empty Threshold REG[403Ah], Index[07h] Default = 04h Read/Write							
n/a		Transmit FIFO Almost Empty Threshold bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 Transmit FIFO Almost Empty Threshold Bits [5:0].
This register determines the threshold at which the transmit FIFO almost empty status bit is set.

Note
The Transmit FIFO Almost Empty threshold must be set greater than zero, as the FIFO count must drop below the threshold to cause an interrupt.

USB Control REG[403Ah], Index[08h] Default = 01h Read/Write							
n/a							USB String Enable
7	6	5	4	3	2	1	0

bit 0 USB String Enable.
When set, this bit allows the default Vendor and Product ID String Descriptors to be returned to the host. When this bit is cleared, the string index values in the Device Descriptor are set to zero.

Maximum Power Consumption REG[403Ah], Index[09h] Default = FAh Read/Write							
Maximum Current bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Maximum Current Bits [7:0].
The amount of current drawn by the peripheral from the USB port in increments of 2 mA. The S1D13A04 reports this value to the host controller in the configuration descriptor. The default and maximum value is 500 mA (FAh * 2 mA).

In order to comply with the USB specification the following formula must apply:
REG[403Ah] index[09h] ≤ FAh.

Packet Control REG[403Ah], Index[0Ah] Default = 00h Read/Write							
EP4 Data Toggle	EP3 Data Toggle	EP2 Data Toggle	EP1 Data Toggle	Reserved	Reserved	n/a	Reserved
7	6	5	4	3	2	1	0

bit 7 EP4 Data Toggle Bit.
Contains the value of the Data Toggle bit to be sent in response to the next IN token to endpoint 4 from the USB host.

Note
When a write is made to this bit, the value cannot be read back before a minimum of 12 USBCLK.

bit 6 EP3 Data Toggle Bit.
Contains the value of the Data Toggle bit expected in the next DATA packet to endpoint 3 from the USB host.

Note
When a write is made to this bit, the value cannot be read back before a minimum of 12 USBCLK.

bit 5 EP2 Data Toggle Bit.
Contains the value of the Data Toggle bit to be sent in response to the next IN token to endpoint 2 from the USB host.

Note
When a write is made to this bit, the value cannot be read back before a minimum of 12 USBCLK.

bit 4 EP1 Data Toggle Bit.
Contains the value of the Data Toggle bit expected in the next DATA packet to endpoint 1 from the USB host.

Note
When a write is made to this bit, the value cannot be read back before a minimum of 12 USBCLK.

bit 3 Reserved.
This bit must be set to 0.

bit 2 Reserved.
This bit must be set to 0.

bit 0 Reserved.
This bit must be set to 0.

Reserved REG[403Ah], Index[0Bh] Default = 00h Read/Write							
n/a							Reserved
7	6	5	4	3	2	1	0

bit 0 Reserved.
This bit must be set to 0.

FIFO Control							
REG[403Ah], Index[0Ch]		Default = 00h					Read/Write
n/a							Transmit FIFO Valid Mode
7	6	5	4	3	2	1	0

bit 0 Transmit FIFO Valid Mode.
When set, this bit causes a NAK response to a host read request from the transmit FIFO (EP4) unless the FIFO Valid bit (in register EP4STAT) is set. When this bit is cleared, any data waiting in the transmit FIFO will be sent in response to a host read request, and the FIFO Valid bit is ignored.

USBFC Input Control Register							
REG[4040h]		Default = 0Dh					Read/Write
n/a							
15	14	13	12	11	10	9	8
n/a	USCMPEN	Reserved	Reserved	ISO	WAKEUP	Reserved	Reserved
7	6	5	4	3	2	1	0

These bits control inputs to the USB module.

bit 6 USCMPEN
This bit controls the USB differential input receiver.
0 = differential input receiver disabled
1 = differential input receiver enabled

bits 5 Reserved.
This bit must be set to 0.

bits 4 Reserved.
This bit must be set to 0.

bit 3 ISO
This bits selects between isochronous and bulk transfer modes for the FIFOs (Endpoint 3 and Endpoint 4).
0 = Isochronous transfer mode
1 = Bulk transfer mode

bit 2 WAKEUP
This active low bit initiates a USB remote wake-up.
0 = initiate USB remote wake-up
1 = no action

bit 1 Reserved.
This bit must be set to 0.

bit 0 Reserved.
This bit must be set to 0.

Reserved REG[4042h]							
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

Pin Input Status / Pin Output Data Register REG[4044h] Default = depends on USB input pin state Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a						USBDETECT Input Pin Status (read only)	USBPUP Output Pin Status
7	6	5	4	3	2	1	0

These bits can generate interrupts.

bit 1 USBDETECT Input Pin Status
This read-only bit indicates the status of the USBDETECT input pin after a steady-state period of 0.5 seconds.

bit 0 USBPUP Output Pin Status
This bit controls the state of the USBPUP output pin.

This bit must be set to 1 to enable the USB interface and USB registers. See the *S1D13A04 Programming Notes and Examples*, document number X37-A-G-003-xx for further information on this bit.

Interrupt Control Enable Register 0 REG[4046h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a	USB Host Connected	Reserved	Reserved	Reserved	Reserved	USBRESET	Reserved
7	6	5	4	3	2	1	0

These bits enable interrupts from the corresponding bit of the Interrupt Control Status/Clear Register 0.
0 = corresponding interrupt bit disabled (masked).
1 = corresponding interrupt bit enabled.

Interrupt Control Enable Register 1 REG[4048h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a	USB Host Disconnect	Reserved	Device Configured	Reserved	Reserved	Reserved	INT
7	6	5	4	3	2	1	0

These bits enable interrupts from the corresponding bit of the Interrupt Control Status/Clear Register 1.
0 = corresponding interrupt bit disabled (masked).
1 = corresponding interrupt bit enabled.

Interrupt Control Status/Clear Register 0 REG[404Ah] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a	USB Host Connected	Reserved	Reserved	Reserved	Reserved	USBRESET	Reserved
7	6	5	4	3	2	1	0

On reads, these bits represent the interrupt status for interrupts caused by low-to-high transitions on the corresponding signals.
0 (read) = no low-to-high event detected on the corresponding signal.
1 (read) = low-to-high event detected on the corresponding signal.

On writes, these bits clear the corresponding interrupt status bit.
0 (write) = corresponding interrupt status bit unchanged.
1 (write) = corresponding interrupt status bit cleared to zero.

These bits must always be cleared via a write to this register before first use. This will ensure that any changes on input pins during system initialization do not generate erroneous interrupts. The interrupt bits are used as follows.

bit 6 USB Host Connected
Indicates the USB device is connected to a USB host.

bit 5 Reserved.
Must be set to 0.

bit 4 Reserved.
Must be set to 0.

bit 3 Reserved.
Must be set to 0.

bit 2 Reserved.
Must be set to 0.

bit 1 USBRESET
Indicates the USB device is reset using the RESET# pin or using the USB port reset.

bit 0 Reserved.
Must be set to 0.

Interrupt Control Status/Clear Register 1 REG[404Ch] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a	USB Host Disconnected	Reserved	Device Configured	Reserved	Reserved	Reserved	INT
7	6	5	4	3	2	1	0

On reads, these bits represent the interrupt status for interrupts caused by high-to-low transitions on the corresponding signals.
0 (read) = no high-to-low event detected on the corresponding signal.
1 (read) = high-to-low event detected on the corresponding signal.

On writes, these bits clear the corresponding interrupt status bit.
0 (write) = corresponding interrupt status bit unchanged.
1 (write) = corresponding interrupt status bit cleared to zero.

These bits must always be cleared via a write to this register before first use. This will ensure that any changes on input pins during system initialization do not generate erroneous interrupts. The interrupt bits are used as follows.

bit 6 USB Host Disconnected
Indicates the USB device is disconnected from a USB host.

bit 5 Reserved.
Must be set to 0.

bit 4 Device Configured.
Indicates the USB device has been configured by the USB host.

bit 3 Reserved.
Must be set to 0.

bit 2 Reserved.
Must be set to 0.

bit 1 Reserved.
Must be set to 0.

bit 0 INT
Indicates an interrupt request originating from within the USB registers (REG[4000h] to REG[403Ah]).

Interrupt Control Masked Status Register 0							
REG[404Eh]	Default = 00h						Read Only
n/a							
15	14	13	12	11	10	9	8
n/a	USB Host Connected	Reserved	Reserved	Reserved	Reserved	USBRESET	Reserved
7	6	5	4	3	2	1	0

These read-only bits represent the logical AND of the corresponding Interrupt Control Status/Clear Register 0 (REG[404Ah])and the Interrupt Control Enable Register 0 (REG[4046h]).

Interrupt Control Masked Status Register 1							
REG[4050h]	Default = 00h						Read Only
n/a							
15	14	13	12	11	10	9	8
n/a	USB Host Disconnected	Reserved	Device Configured	Reserved	Reserved	Reserved	INT
7	6	5	4	3	2	1	0

These read-only bits represent the logical AND of the corresponding Interrupt Control Status/Clear Register 1 (REG[404Ch]) and the Interrupt Control Enable Register 1 (REG[4048h]).

USB Software Reset Register							
REG[4052h]	Default = 00h						Write Only
n/a							
15	14	13	12	11	10	9	8
USB Software Reset (Code = 10100100) bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 USB Software Reset Bits [7:0] **(Write Only)**
When the specific code of 10100100b is written to these bits the USB module of the S1D13A04 is reset. Use of the above code avoids the possibility of accidently resetting the USB.

USB Wait State Register REG[4054h] Default = 00h Read/Write							
n/a							
15	14	13	12	11	10	9	8
n/a						USB Wait State bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 USB Wait State Bits [1:0]
This register controls the number of wait states the S1D13A04 uses for its internal USB support. For all bus interfaces supported by the S1D13A04 **these bits must be set to 01**.

8.5 2D Acceleration (BitBLT) Registers (Offset = 8000h)

These registers control the S1D13A04 2D Acceleration engine. For detailed BitBLT programming instructions, see the *S1D13A04 Programming Notes and Examples*, document number X37A-G-003-xx.

BitBLT Control Register
REG[8000h] Default = 00000000h Read/Write

n/a													Color Format Select	Dest Linear Select	Source Linear Select
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a															BitBLT Enable (WO)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bit 18 BitBLT Color Format Select
This bit selects the color format that the 2D operation is applied to.
When this bit = 0, 8 bpp (256 color) format is selected.
When this bit = 1, 16 bpp (64K color) format is selected.

bit 17 BitBLT Destination Linear Select
When this bit = 1, the Destination BitBLT is stored as a contiguous linear block of memory.
When this bit = 0, the Destination BitBLT is stored as a rectangular region of memory. The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.

bit 16 BitBLT Source Linear Select
When this bit = 1, the Source BitBLT is stored as a contiguous linear block of memory.
When this bit = 0, the Source BitBLT is stored as a rectangular region of memory.
The BitBLT Memory Address Offset register (REG[8014h]) determines the address offset from the start of one line to the next line.

bit 0 BitBLT Enable
This bit is write only.
Setting this bit to 1 begins the 2D BitBLT operation. **This bit must not be set to 0 while a BitBLT operation is in progress.**

Note
To determine the status of a BitBLT operation use the BitBLT Busy Status bit (REG[8004h] bit 0).

BitBLT Status Register REG[8004h] Default = 00000000h Read Only															
n/a			Number of Used FIFO Entries					n/a			Number of Free FIFO Entries (0 means full)				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a									FIFO Not Empty	FIFO Half Full	FIFO Full Status	n/a			BitBLT Busy Status
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 28-24 Number of Used FIFO Entries Bits [4:0]
These bits indicate the minimum number of FIFO entries currently in use (there may be more values in internal pipeline stages).

bits 20-16 Number of Free FIFO Entries Bits [4:0]
These bits indicate the number of empty FIFO entries available. If these bits return a 0, the FIFO is full.

bit 6 BitBLT FIFO Not-Empty Status
This is a read-only status bit.
When this bit = 0, the BitBLT FIFO is empty.
When this bit = 1, the BitBLT FiFO has at least one data.
To reduce system memory read latency, software can monitor this bit prior to a BitBLT read burst operation.

The following table shows the number of words available in BitBLT FIFO under different status conditions.

Table 8-18: BitBLT FIFO Words Available

BitBLT FIFO Full Status (REG[8004h] Bit 4)	BitBLT FIFO Half Full Status (REG[8004h] Bit 5)	BitBLT FIFO Not Empty Status (REG[8004h] Bit 6)	Number of Words available in BitBLT FIFO
0	0	0	0
0	0	1	1 to 6
0	1	1	7 to 14
1	1	1	15 to 16

bit 5 BitBLT FIFO Half Full Status
This is a read-only status bit.
When this bit = 1, the BitBLT FIFO is half full or greater than half full.
When this bit = 0, the BitBLT FIFO is less than half full.

bit 4 BitBLT FIFO Full Status
This is a read-only status bit.
When this bit = 1, the BitBLT FIFO is full.
When this bit = 0, the BitBLT FIFO is not full.

bit 0 BitBLT Busy Status
This bit is a read-only status bit.
When this bit = 1, the BitBLT operation is in progress.
When this bit = 0, the BitBLT operation is complete.

Note
During a BitBLT Read operation, the BitBLT engine does not attempt to keep the FIFO full. If the FIFO becomes full, the BitBLT operation stops temporarily as data is read out of the FIFO. The BitBLT will restart only when less than 14 values remain in the FIFO.

BitBLT Command Register															
REG[8008h]			Default = 00000000h												Read/Write
n/a												BitBLT ROP Code bits 3-0			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a												BitBLT Operation bits 3-0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 19-16 BitBLT Raster Operation Code/Color Expansion Bits [3:0]
ROP Code for Write BitBLT and Move BitBLT. Bits 2-0 also specify the start bit position for Color Expansion.

Table 8-19 : BitBLT ROP Code/Color Expansion Function Selection

BitBLT ROP Code Bits [3:0]	Boolean Function for Write BitBLT and Move BitBLT	Boolean Function for Pattern Fill	Start Bit Position for Color Expansion
0000	0 (Blackness)	0 (Blackness)	bit 0
0001	~S . ~D or ~(S + D)	~P . ~D or ~(P + D)	bit 1
0010	~S . D	~P . D	bit 2
0011	~S	~P	bit 3
0100	S . ~D	P . ~D	bit 4
0101	~D	~D	bit 5
0110	S ^ D	P ^ D	bit 6
0111	~S + ~D or ~(S . D)	~P + ~D or ~(P . D)	bit 7
1000	S . D	P . D	bit 0
1001	~(S ^ D)	~(P ^ D)	bit 1
1010	D	D	bit 2
1011	~S + D	~P + D	bit 3
1100	S	P	bit 4
1101	S + ~D	P + ~D	bit 5
1110	S + D	P + D	bit 6
1111	1 (Whiteness)	1 (Whiteness)	bit 7

Note
S = Source, D = Destination, P = Pattern.
~ = NOT, . = Logical AND, + = Logical OR, ^ = Logical XOR

bits 3-0 BitBLT Operation Bits [3:0]
Specifies the 2D Operation to be carried out based on the following table.

Table 8-20 : BitBLT Operation Selection

BitBLT Operation Bits [3:0]	BitBLT Operation
0000	Write BitBLT with ROP.
0001	Read BitBLT.
0010	Move BitBLT in positive direction with ROP.
0011	Move BitBLT in negative direction with ROP.
0100	Transparent Write BitBLT.
0101	Transparent Move BitBLT in positive direction.
0110	Pattern Fill with ROP.
0111	Pattern Fill with transparency.
1000	Color Expansion.
1001	Color Expansion with transparency.
1010	Move BitBLT with Color Expansion.
1011	Move BitBLT with Color Expansion and transparency.
1100	Solid Fill.
Other combinations	Reserved

BitBLT Source Start Address Register REG[800Ch] Default = 00000000h Read/Write															
n/a											BitBLT Source Start Address bits 20-16				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BitBLT Source Start Address bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 20-0 BitBLT Source Start Address Bits [20:0]
A 21-bit register that specifies the source start address for the BitBLT operation.
If data is sourced from the CPU, then bit 0 is used for byte alignment within a 16-bit word and the other address bits are ignored. In pattern fill operation, the BitBLT Source Start Address is defined by the following equation.

Value programmed to the Source Start Address Register =
Pattern Base Address + Pattern Line Offset + Pixel Offset.

The following table shows how Source Start Address Register is defined for 8 and 16 bpp color depths.

Table 8-21 : BitBLT Source Start Address Selection

Color Format	Pattern Base Address[20:0]	Pattern Line Offset[2:0]	Pixel Offset[3:0]
8 bpp	BitBLT Source Start Address[20:6]	BitBLT Source Start Address[5:3]	BitBLT Source Start Address[2:0]
16 bpp	BitBLT Source Start Address[20:7]	BitBLT Source Start Address[6:4]	BitBLT Source Start Address[3:0]

Note
For further information on the BitBLT Source Start Address register, see the *S1D13A04 Programming Notes and Examples*, document number X37A-G-003-xx.

BitBLT Destination Start Address Register REG[8010h] Default = 00000000h Read/Write															
n/a											BitBLT Destination Start Address bits 20-16				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BitBLT Destination Start Address bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 20-0 BitBLT Destination Start Address Bits [20:0]
A 21-bit register that specifies the destination start address for the BitBLT operation.

BitBLT Memory Address Offset Register															
REG[8014h]			Default = 00000000h												Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a					BitBLT Memory Address Offset bits 10-0										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 10-0 BitBLT Memory Address Offset Bits [10:0]
These bits are the display's 11-bit address offset from the starting word of line *n* to the starting word of line *n + 1*. They are used only for address calculation when the BitBLT is configured as a rectangular region of memory. They are not used for the displays.

BitBLT Width Register															
REG[8018h]			Default = 00000000h												Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						BitBLT Width bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0 BitBLT Width Bits [9:0]
A 10-bit register that specifies the BitBLT width in pixels - 1.

BitBLT width in pixels = (ContentsOfThisRegister) + 1

BitBLT Height Register															
REG[801Ch]			Default = 00000000h												Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
n/a						BitBLT Height bits 9-0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 9-0 BitBLT Height Bits [9:0]
A 10-bit register that specifies the BitBLT height in lines - 1.

BitBLT height in lines = (ContentsOfThisRegister) + 1

BitBLT Background Color Register															
REG[8020h]			Default = 00000000h												Read/Write
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BitBLT Background Color bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-0 BitBLT Background Color Bits [15:0]
This register specifies the BitBLT background color for Color Expansion or key color for Transparent BitBLT. For 16 bpp color depths (REG[8000h] bit 18 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8000h] bit 18 = 0), bits 7-0 are used.

Note
For Big Endian implementations, see the *S1D13A04 Programming Notes and Examples*, document number X37A-G-003-xx.

BitBLT Foreground Color Register REG[8024h] Default = 00000000h Read/Write															
n/a															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BitBLT Foreground Color bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-0 BitBLT Foreground Color Bits [15:0]
This register specifies the BitBLT foreground color for Color Expansion or Solid Fill. For 16 bpp color depths (REG[8000h] bit 18 = 1), bits 15-0 are used. For 8 bpp color depths (REG[8000h] bit 18 = 0), bits 7-0 are used.

Note
For Big Endian implementations, see the *S1D13A04 Programming Notes and Examples*, document number X37A-G-003-xx.

8.6 2D Accelerator (BitBLT) Data Register Descriptions

The 2D Accelerator (BitBLT) data registers decode AB15-AB0 and require AB16 = 1. The BitBLT data registers are 32-bit wide. Byte access to the BitBLT data registers is not allowed.

2D Accelerator (BitBLT) Data Memory Mapped Region Register AB16-AB0 = 10000h-1FFFEh, even addresses															Read/Write
BitBLT Data bits 31-16															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BitBLT Data bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-0 BitBLT Data Bits [15:0]
This register specifies the BitBLT data. This register is loosely decoded from 10000h to 1FFFEh.

9 2D Accelerator (BitBLT) Engine

9.1 Overview

The S1D13A04 is designed with a built-in 2D BitBLT engine which increases the performance of Bit Block Transfers (BitBLT). It supports 8 and 16 bit-per-pixel color depths.

The BitBLT engine supports rectangular and linear addressing modes for source and destination in a positive direction for all BitBLT operations except the move BitBLT which also supports in a negative direction.

The BitBLT operations support byte alignment of all types. The BitBLT engine has a dedicated BitBLT IO access space. This allows the BitBLT engine to support simultaneous BitBLT and host side operations.

9.2 BitBLT Operations

The S1D13A04 2D BitBLT engine supports the following BitBLTs. For detailed information on using the individual BitBLT operations, refer to the S1D13A04 Programming Notes and Examples, document number X37A-G-003-xx.

- Write BitBLT.
- Move BitBLT.
- Solid Fill BitBLT.
- Pattern Fill BitBLT.
- Transparent Write BitBLT.
- Transparent Move BitBLT.
- Read BitBLT.
- Color Expansion BitBLT.
- Move BitBLT with Color Expansion.

Note
For details on the BitBLT registers, see Section 8.5, “2D Acceleration (BitBLT) Registers (Offset = 8000h)” on page 138.

10 Frame Rate Calculation

The following formula is used to calculate the display frame rate.

$$\text{FrameRate} = \frac{f_{PCLK}}{(HT) \times (VT)}$$

Where:

f_{PCLK} = PClk frequency (Hz)

HT = Horizontal Total
= ((REG[20h] bits 6-0) + 1) x 8 Pixels

VT = Vertical Total
= ((REG[30h] bits 9-0) + 1) Lines

11 Display Data Formats

The following diagrams show the display mode data formats for a little-endian system.

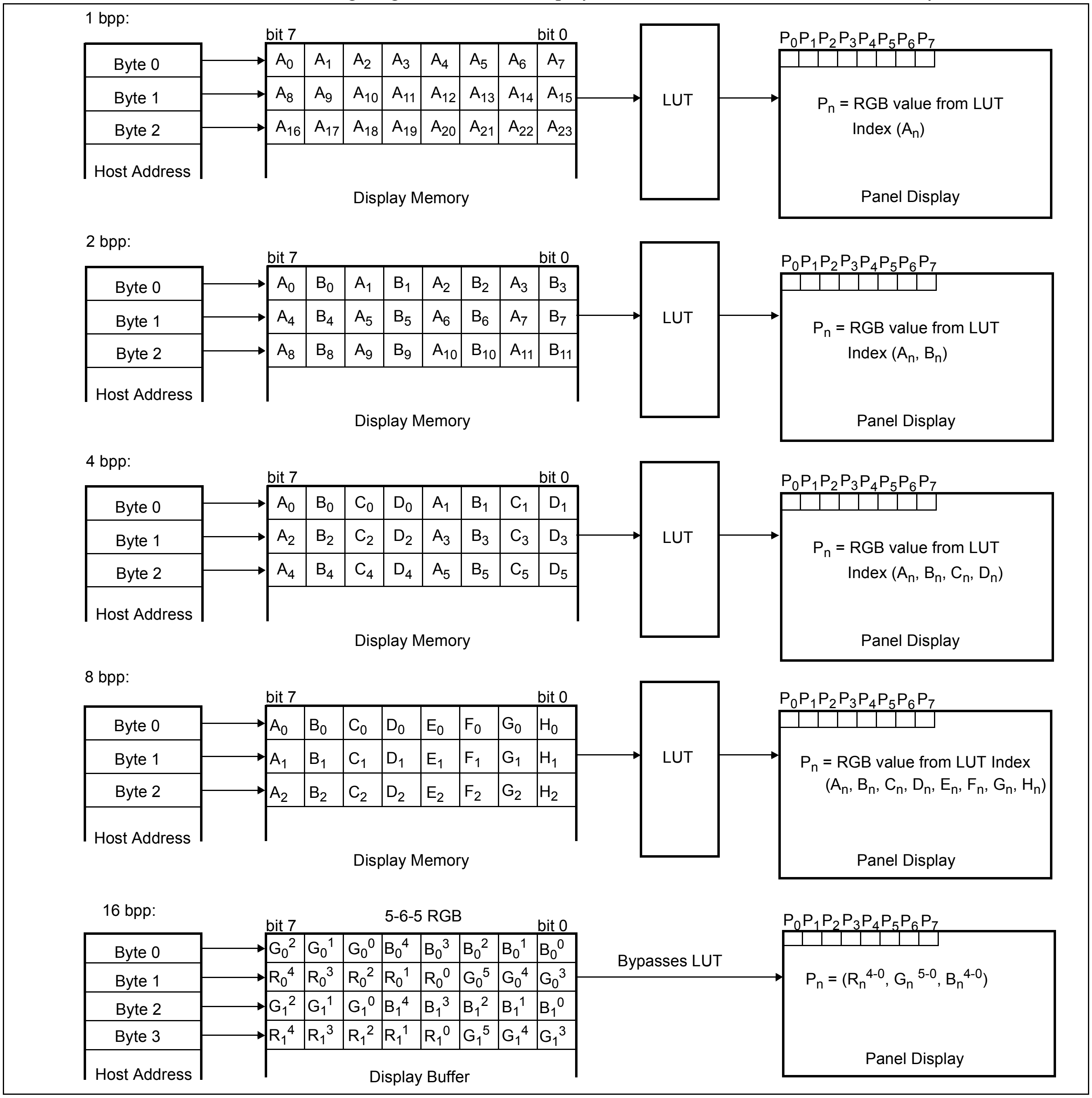


Figure 11-1: 4/8/16 Bit-Per-Pixel Display Data Memory Organization

Note

1. The Host-to-Display mapping shown here is for a little endian system.
2. For 16 bpp format, R_n, G_n, B_n represent the red, green, and blue color components.

12 Look-Up Table Architecture

The following figures are intended to show the display data output path only.

Note
When Video Data Invert is enabled the video data is inverted after the Look-Up Table.

12.1 Monochrome Modes

The green Look-Up Table (LUT) is used for all monochrome modes.

1 Bit-per-pixel Monochrome Mode

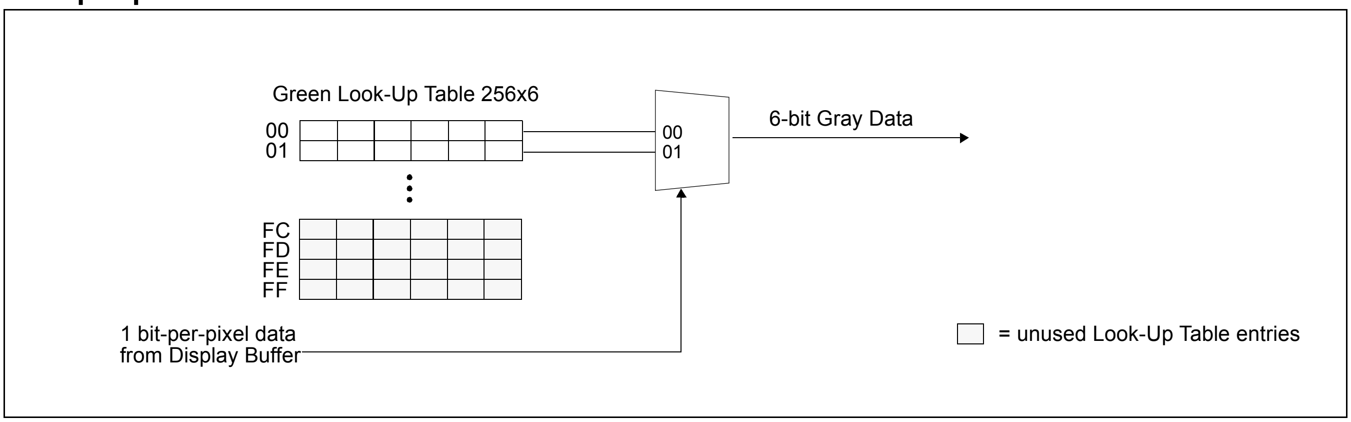


Figure 12-1: 1 Bit-per-pixel Monochrome Mode Data Output Path

2 Bit-per-pixel Monochrome Mode

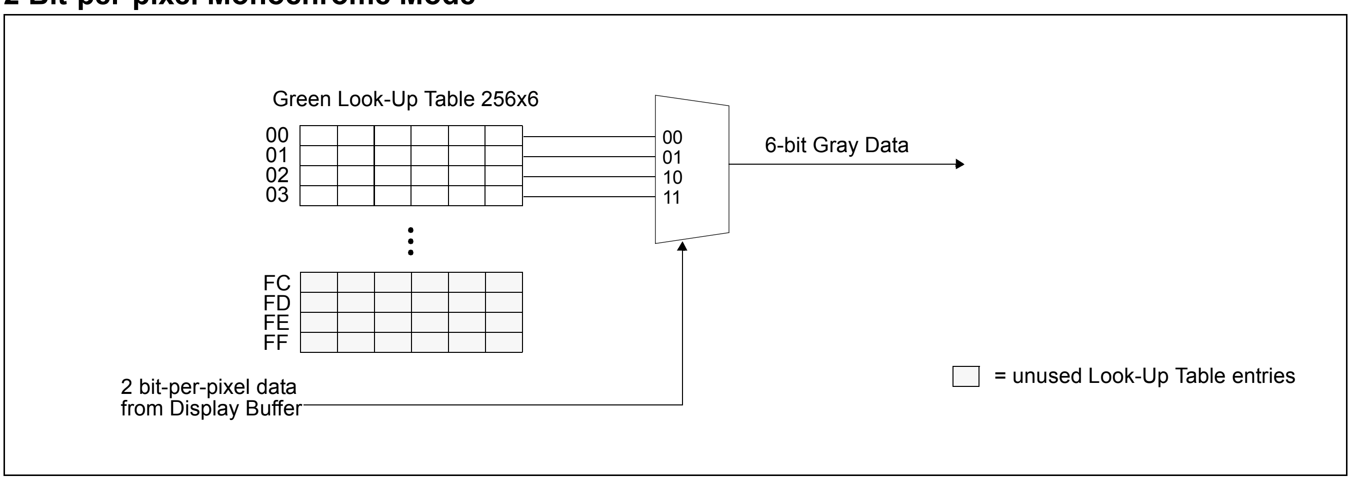


Figure 12-2: 2 Bit-per-pixel Monochrome Mode Data Output Path

4 Bit-per-pixel Monochrome Mode

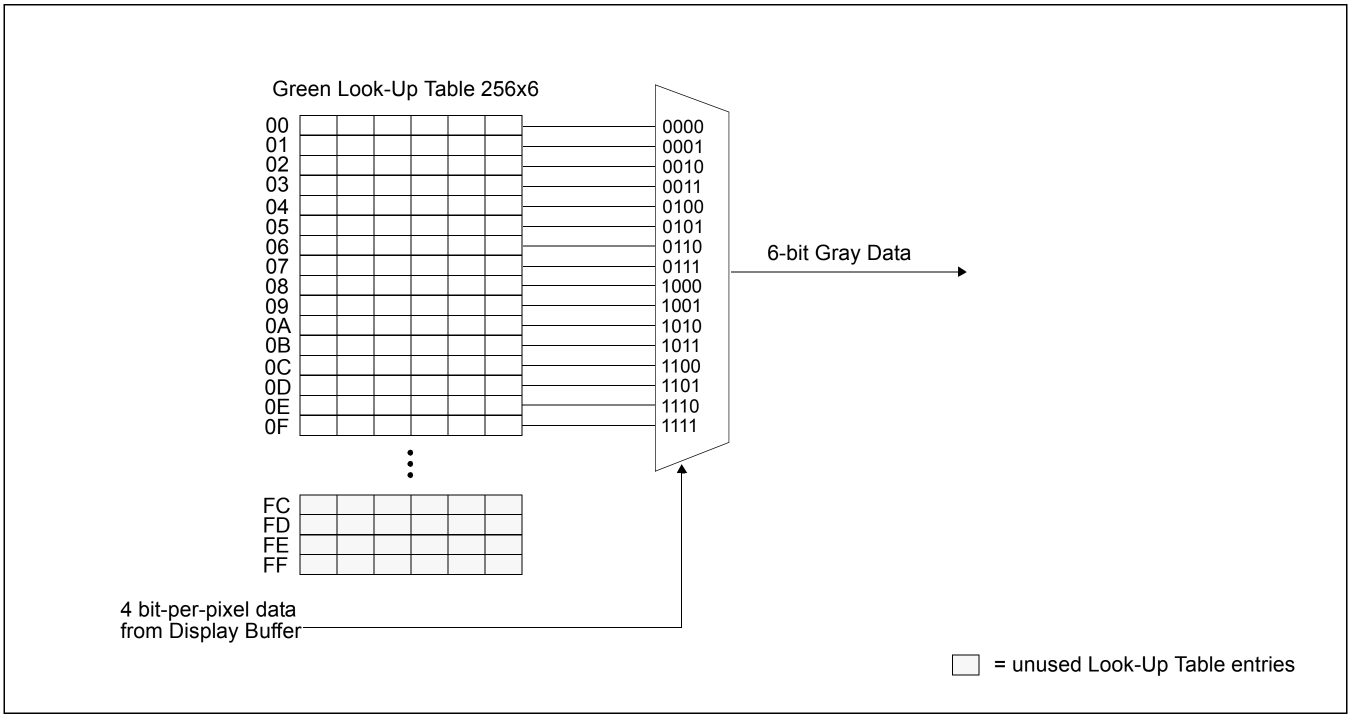


Figure 12-3: 4 Bit-per-pixel Monochrome Mode Data Output Path

8 Bit-per-pixel Monochrome Mode

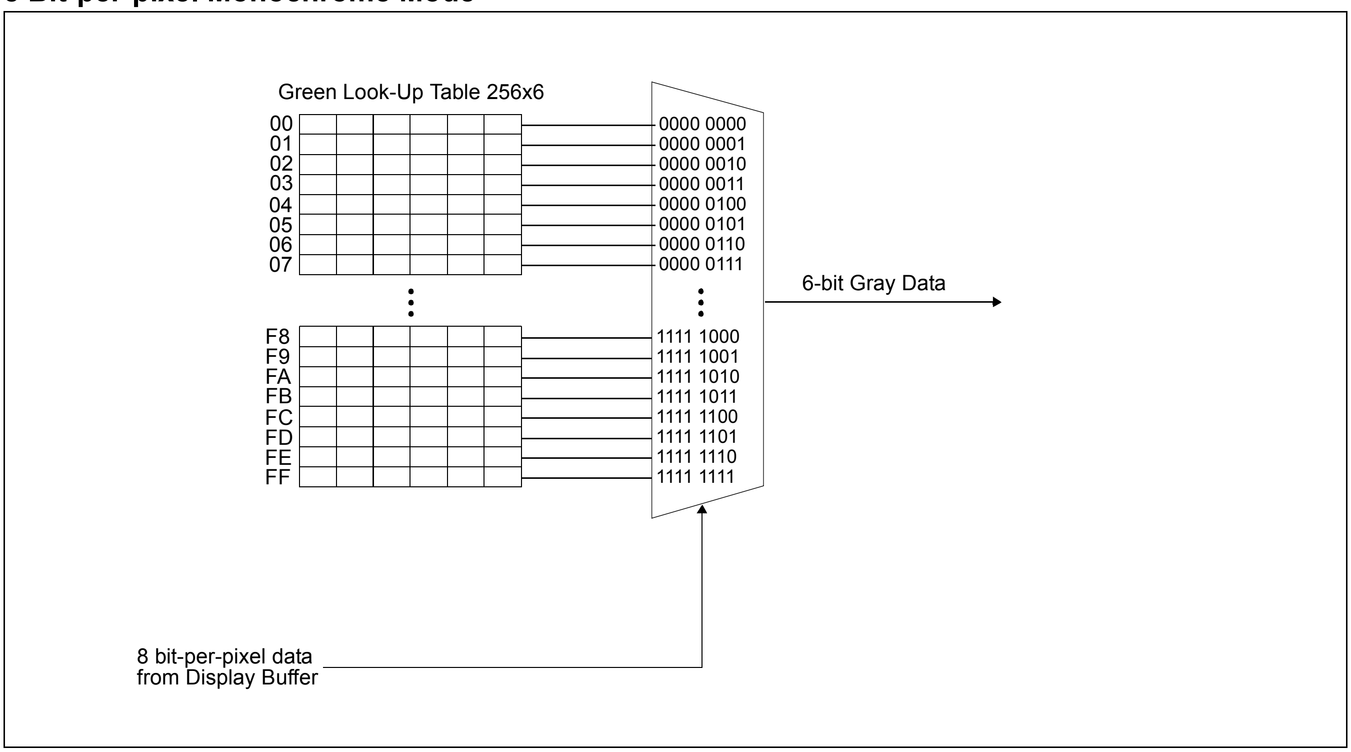


Figure 12-4: 8 Bit-per-pixel Monochrome Mode Data Output Path

16 Bit-Per-Pixel Monochrome Mode

The LUT is bypassed and the green data is directly mapped for this color depth– “Display Data Formats” on page 148..

12.2 Color Modes

1 Bit-Per-Pixel Color

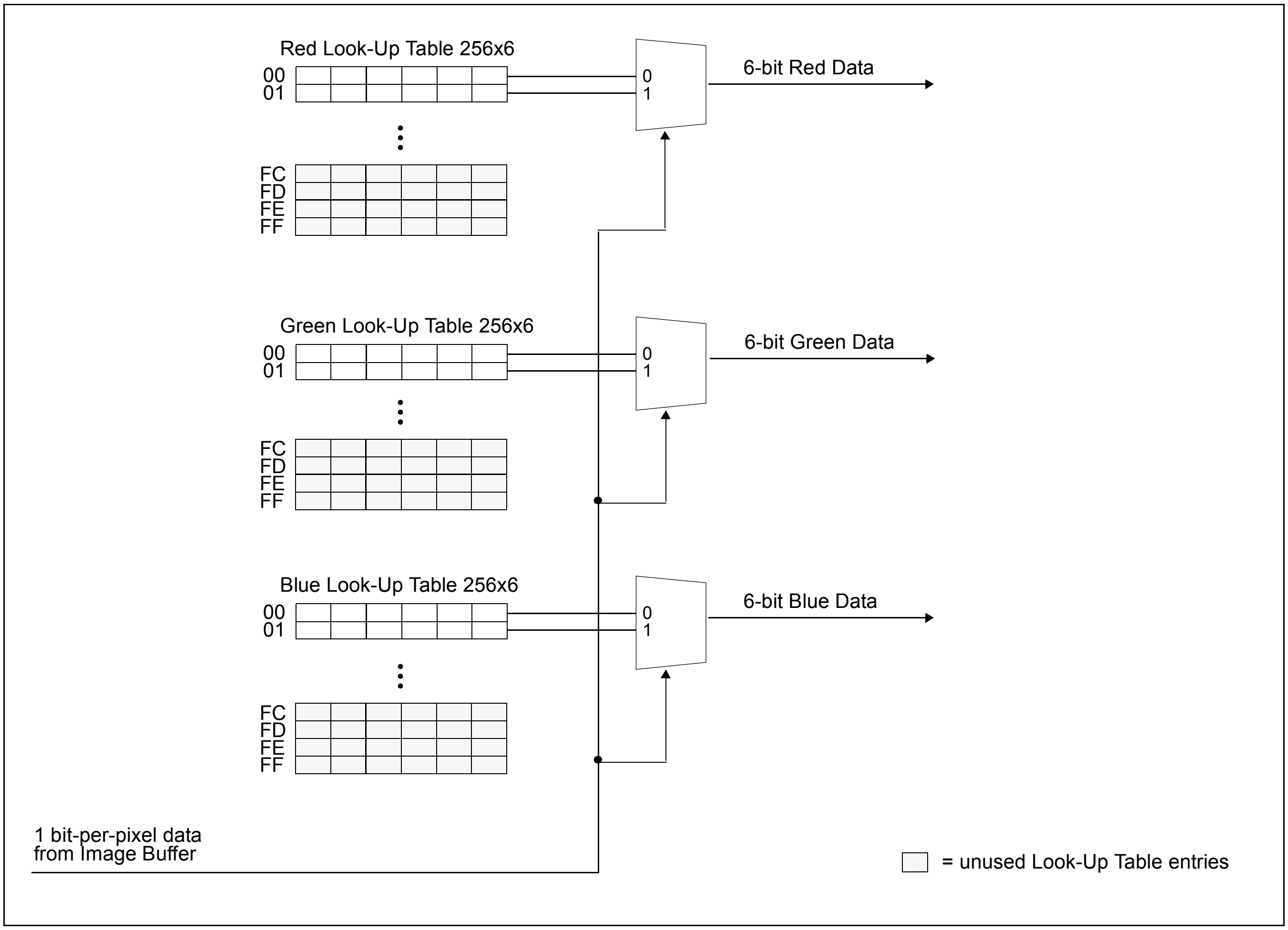


Figure 12-5: 1 Bit-Per-Pixel Color Mode Data Output Path

2 Bit-Per-Pixel Color

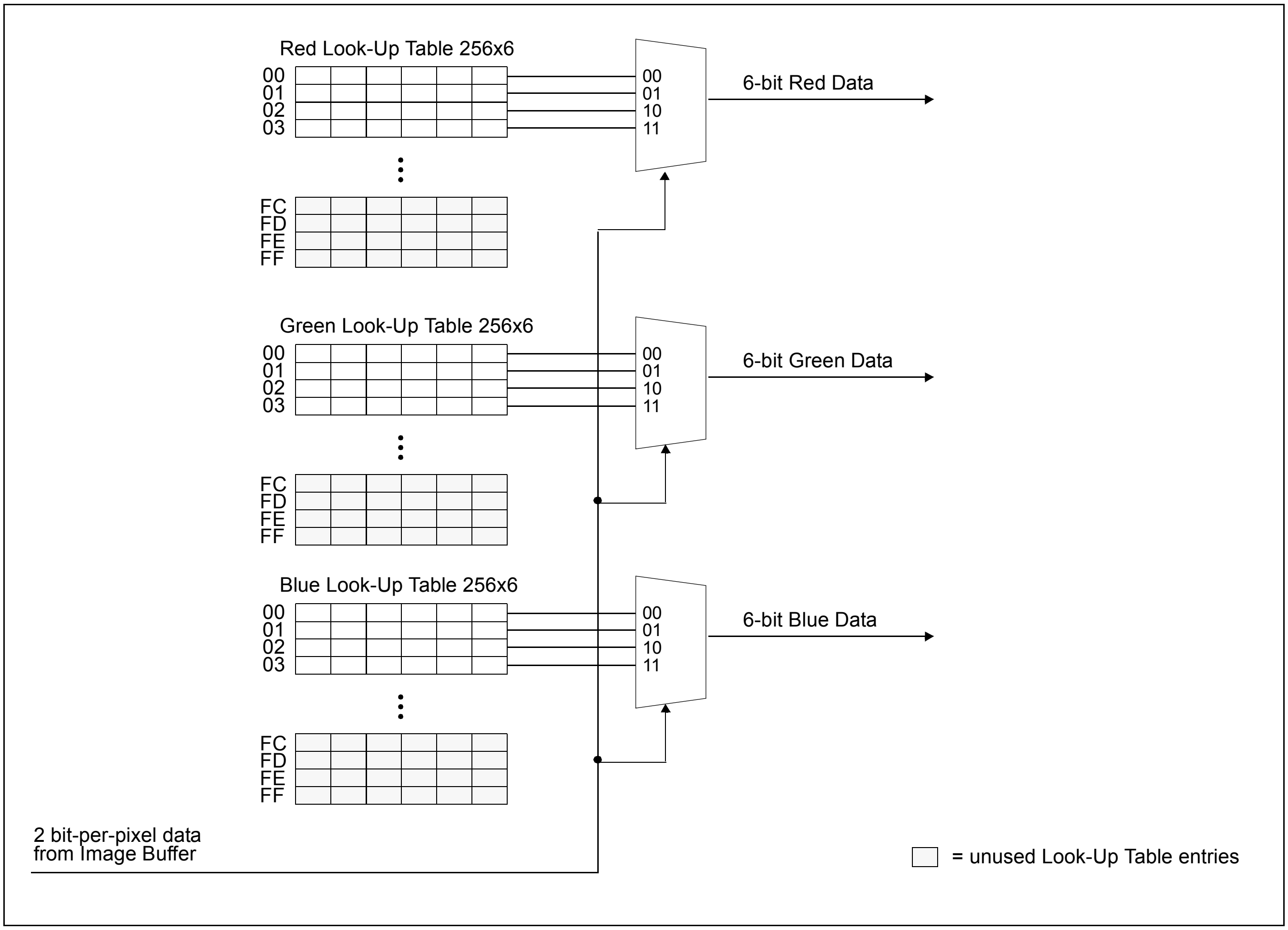


Figure 12-6: 2 Bit-Per-Pixel Color Mode Data Output Path

4 Bit-Per-Pixel Color

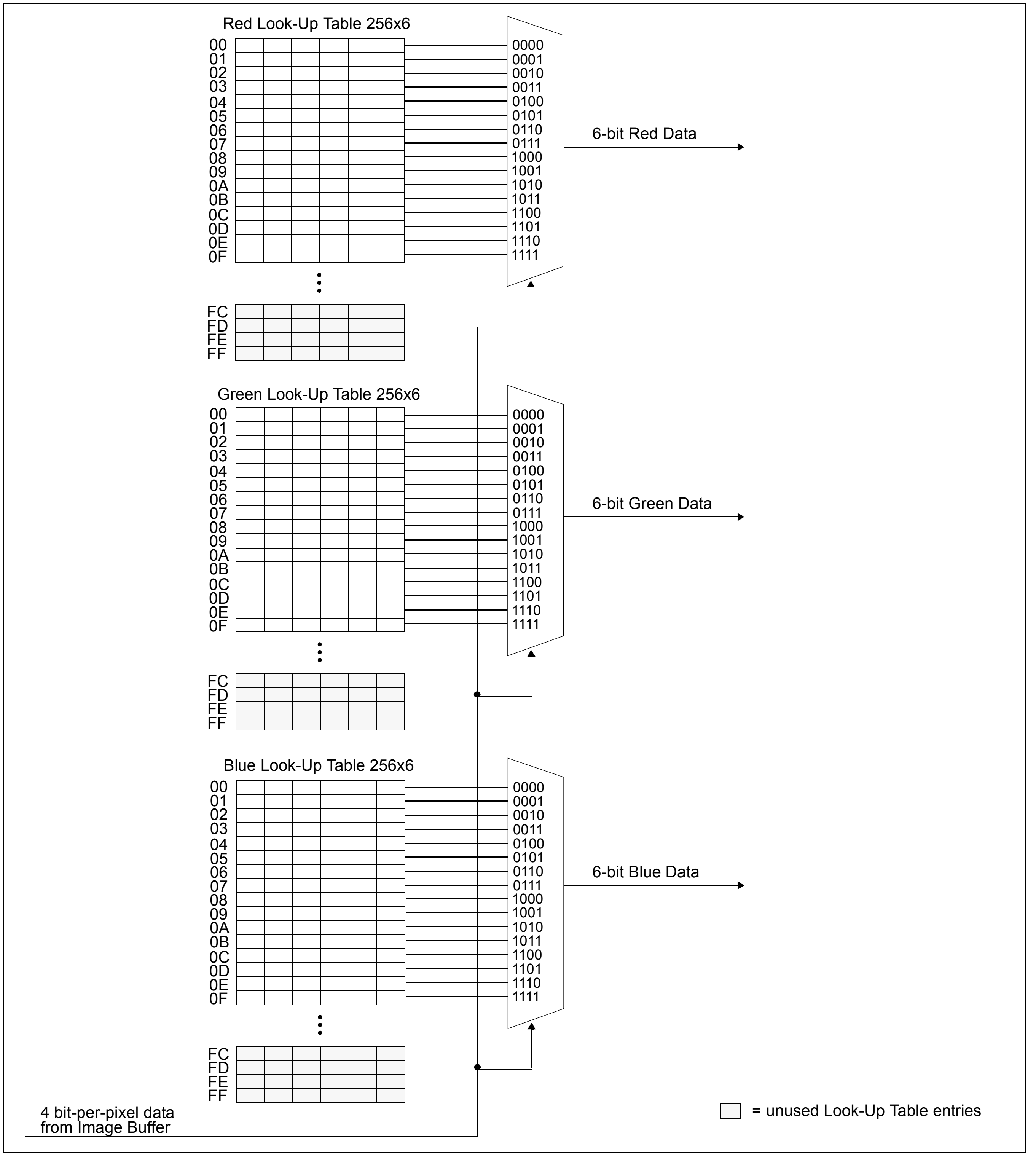


Figure 12-7: 4 Bit-Per-Pixel Color Mode Data Output Path

8 Bit-per-pixel Color Mode

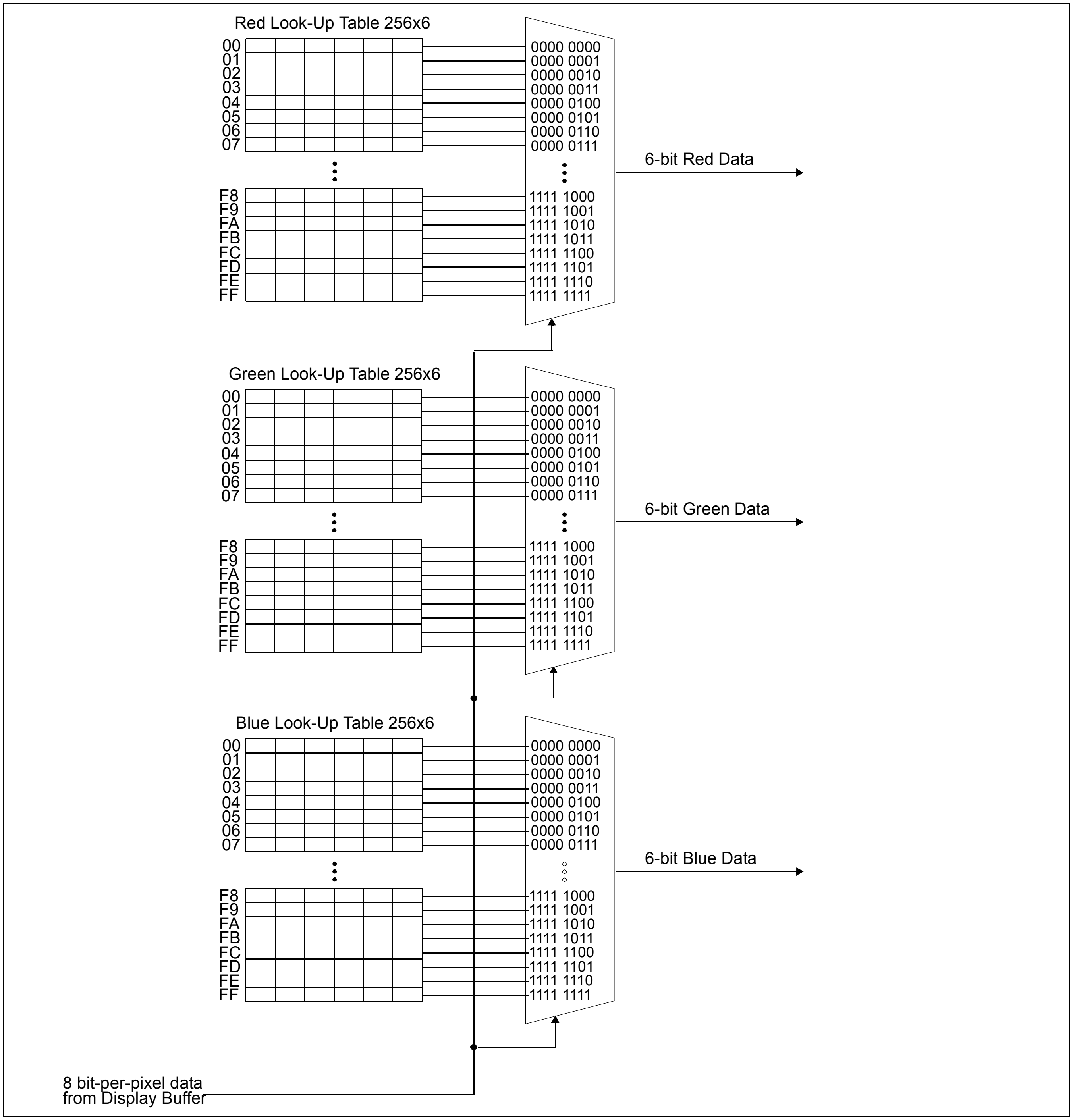


Figure 12-8: 8 Bit-per-pixel Color Mode Data Output Path

16 Bit-Per-Pixel Color Mode

The LUT is bypassed and the color data is directly mapped for this color depth– “Display Data Formats” on page 148.

13 SwivelView™

13.1 Concept

Most computer displays are refreshed in landscape orientation – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView™ is designed to rotate the displayed image on an LCD by 90°, 180°, or 270° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView™ offers a performance advantage over software rotation of the displayed image.

The image is not actually rotated in the display buffer since there is no address translation during CPU read/write. The image is rotated during display refresh.

Note

The Pixel Doubling feature of the S1D13A04 is not available in 90° and 270° SwivelView rotations.

13.2 90° SwivelView™

90° SwivelView™ requires the Memory Clock (MCLK) to be at least 1.25 times the frequency of the Pixel Clock (PCLK), i.e. MCLK ≥ 1.25PCLK.

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13A04 in the following sense: A–B–C–D. The display is refreshed by the S1D13A04 in the following sense: B-D-A-C.

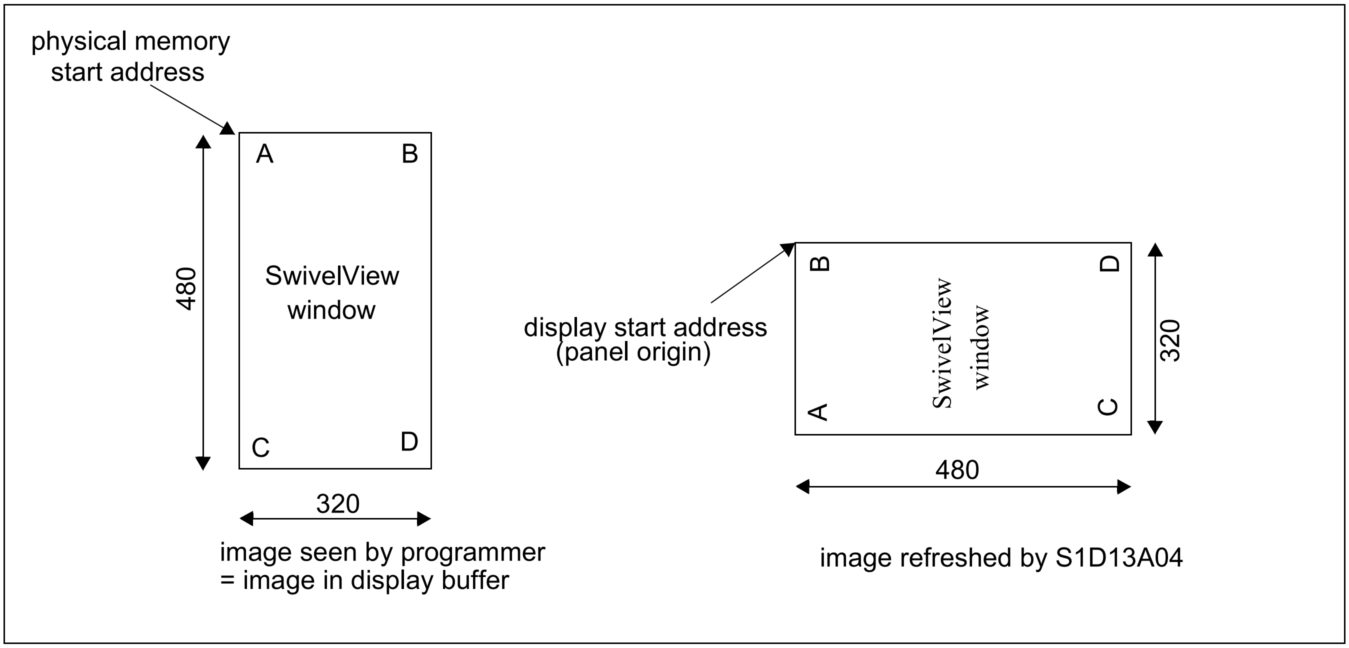


Figure 13-1: Relationship Between The Screen Image and the Image Refreshed in 90° SwivelView.

13.2.1 Register Programming

Enable 90° SwivelView™ Mode

Set SwivelView™ Mode Select bits (REG[10h] bits 17:16) to 01.

Display Start Address

The display refresh circuitry starts at pixel “B”, therefore the Main Window Display Start Address register (REG[40h]) must be programmed with the address of pixel “B”. To calculate the value of the address of pixel “B” use the following formula (assumes 8 bpp color depth).

REG[40h] bits 16:0 = ((image address + (panel height x bpp ÷ 8)) ÷ 4) - 1
= ((0 + (320 pixels x 8 bpp ÷ 8)) ÷ 4) -1
= 79 (4Fh)

Line Address Offset

The Main Window Line Address Offset register (REG[44h]) is based on the display width and programmed using the following formula.

REG[44h] bits 9:0 = display width in pixels ÷ (32 ÷ bpp)
= 320 pixels ÷ (32 ÷ 8 bpp)
= 80 (50h)

13.3 180° SwivelView™

The following figure shows how the programmer sees a 480x320 landscape image and how the image is being displayed. The application image is written to the S1D13A04 in the following sense: A–B–C–D. The display is refreshed by the S1D13A04 in the following sense: D-C-B-A.

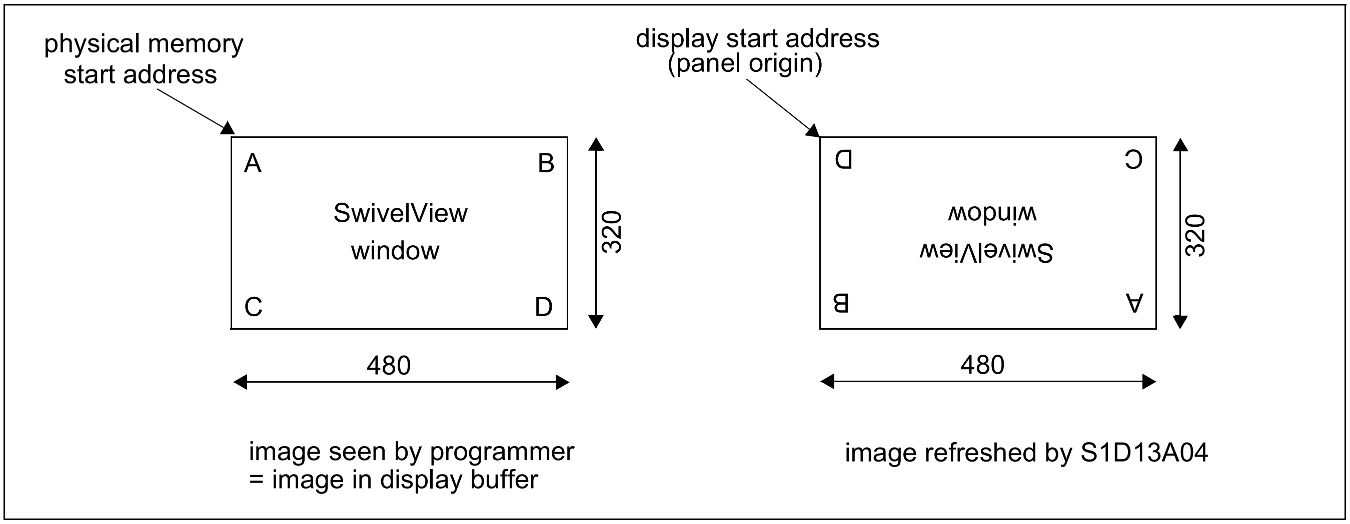


Figure 13-2: Relationship Between The Screen Image and the Image Refreshed in 180° SwivelView.

13.3.1 Register Programming

Enable 180° SwivelView™ Mode

Set SwivelView™ Mode Select bits (REG[10h] bits 17:16) to 10.

Display Start Address

The display refresh circuitry starts at pixel "D", therefore the Main Window Display Start Address register (REG[40h]) must be programmed with the address of pixel "D". To calculate the value of the address of pixel "D" use the following formula (assumes 8 bpp color depth).

REG[40h] bits 16:0
= ((image address + (offset x (panel height - 1) + panel width) x bpp ÷ 8) ÷ 4) - 1
= ((0 + (480 pixels x 319 pixels + 480 pixels) x 8 bpp ÷ 8) ÷ 4) - 1
= 38399 (95FFh)

Line Address Offset

The Main Window Line Address Offset register (REG[44h]) is based on the display width and programmed using the following formula.

REG[44h] bits 9:0 = display width in pixels ÷ (32 ÷ bpp)
= 480 pixels ÷ (32 ÷ 8 bpp)
= 120 (78h)

13.4 270° SwivelView™

270° SwivelView™ requires the Memory Clock (MCLK) to be at least 1.25 times the frequency of the Pixel Clock (PCLK), i.e. MCLK ≥ 1.25PCLK.

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13A04 in the following sense: A–B–C–D. The display is refreshed by the S1D13A04 in the following sense: C-A-D-B.

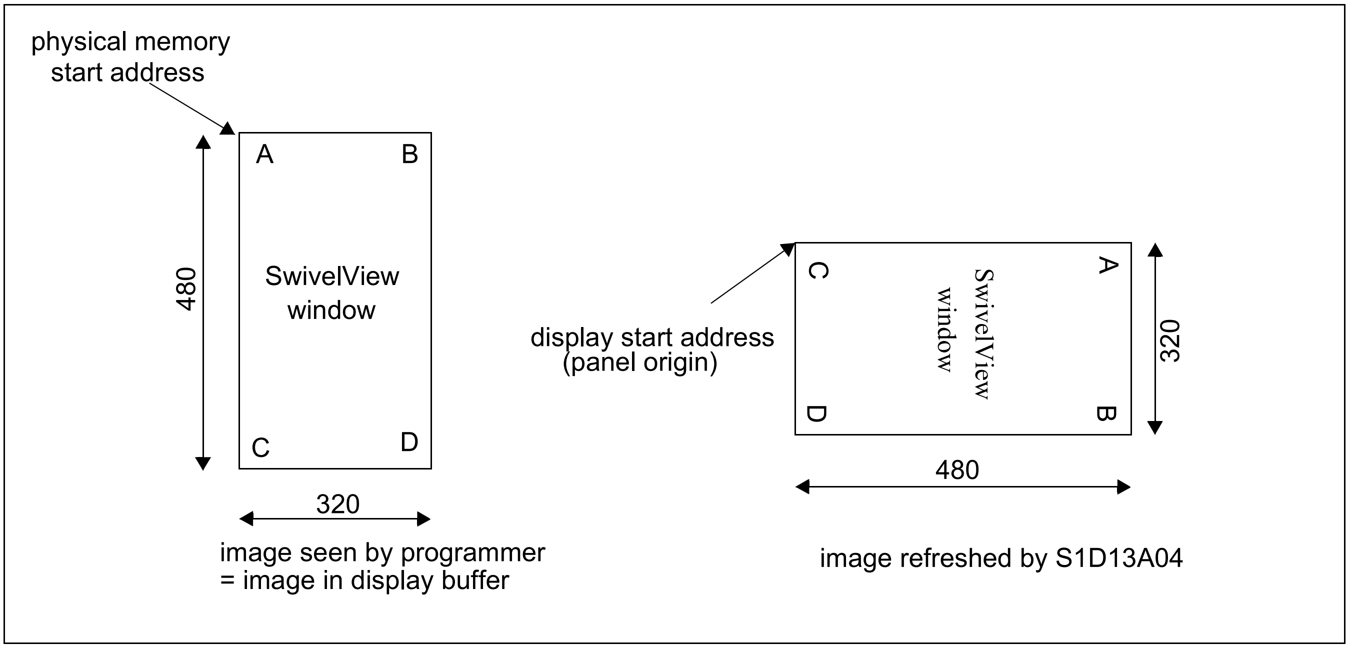


Figure 13-3: Relationship Between The Screen Image and the Image Refreshed in 270° SwivelView.

13.4.1 Register Programming

Enable 270° SwivelView™ Mode

Set SwivelView™ Mode Select bits (REG[10h] bits 17:16) to 11.

Display Start Address

The display refresh circuitry starts at pixel “C”, therefore the Main Window Display Start Address register (REG[40h]) must be programmed with the address of pixel “C”. To calculate the value of the address of pixel “C” use the following formula (assumes 8 bpp color depth).

REG[40h] bits 16:0 = (image address + ((panel width - 1) x offset x bpp ÷ 8) ÷ 4)
= (0 + ((480 pixels - 1) x 320 pixels x 8 bpp ÷ 8) ÷ 4)
= 38320 (95B0h)

Line Address Offset

The Main Window Line Address Offset register (REG[44h]) is based on the display width and programmed using the following formula.

REG[44h] bits 9:0 = display width in pixels ÷ (32 ÷ bpp)
= 320 pixels ÷ (32 ÷ 8 bpp)
= 80 (50h)

14 Picture-in-Picture Plus (PIP$^+$)

14.1 Concept

Picture-in-Picture Plus (PIP$^+$) enables a secondary window (or PIP$^+$ window) within the main display window. The PIP$^+$ window may be positioned anywhere within the virtual display and is controlled through the PIP$^+$ Window control registers (REG[50h] through REG[5Ch]). The PIP$^+$ window retains the same color depth and SwivelView orientation as the main window.

The following diagram shows an example of a PIP$^+$ window within a main window and the registers used to position it.

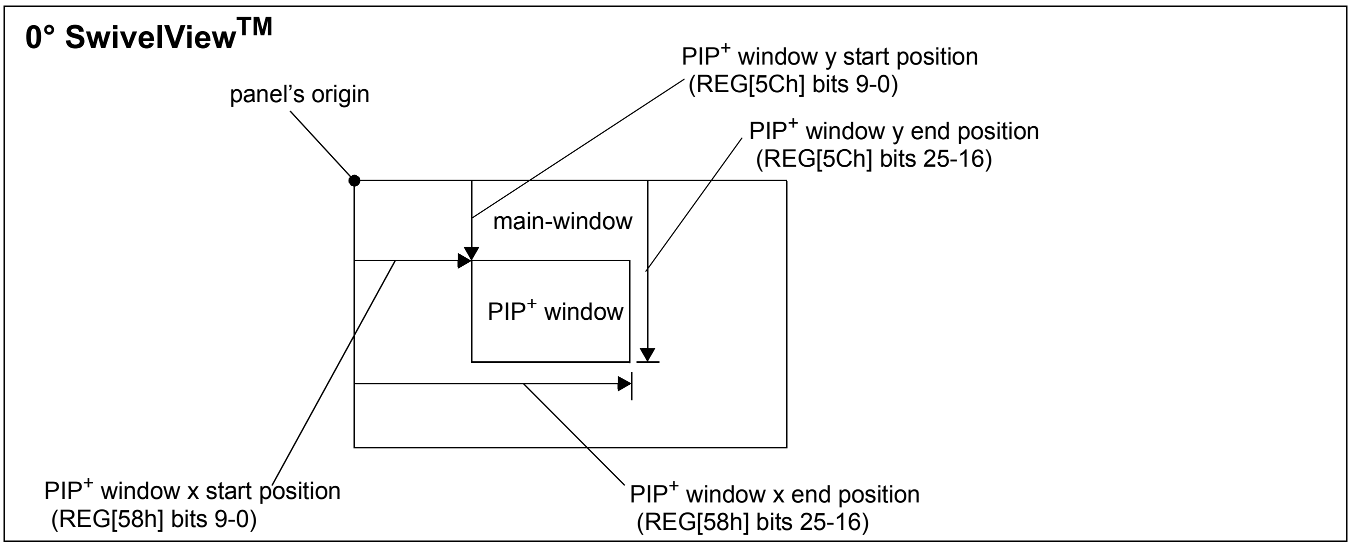


Figure 14-1: Picture-in-Picture Plus with SwivelView disabled

14.2 With SwivelView Enabled

14.2.1 SwivelView 90°

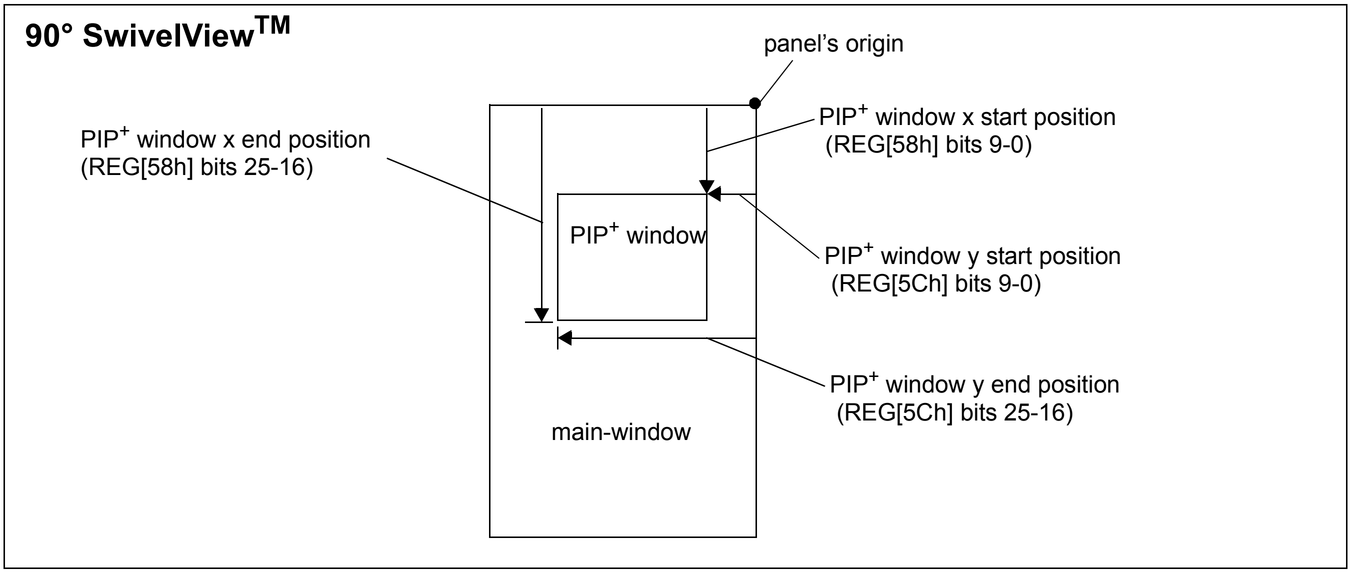


Figure 14-2: Picture-in-Picture Plus with SwivelView 90° enabled

14.2.2 SwivelView 180°

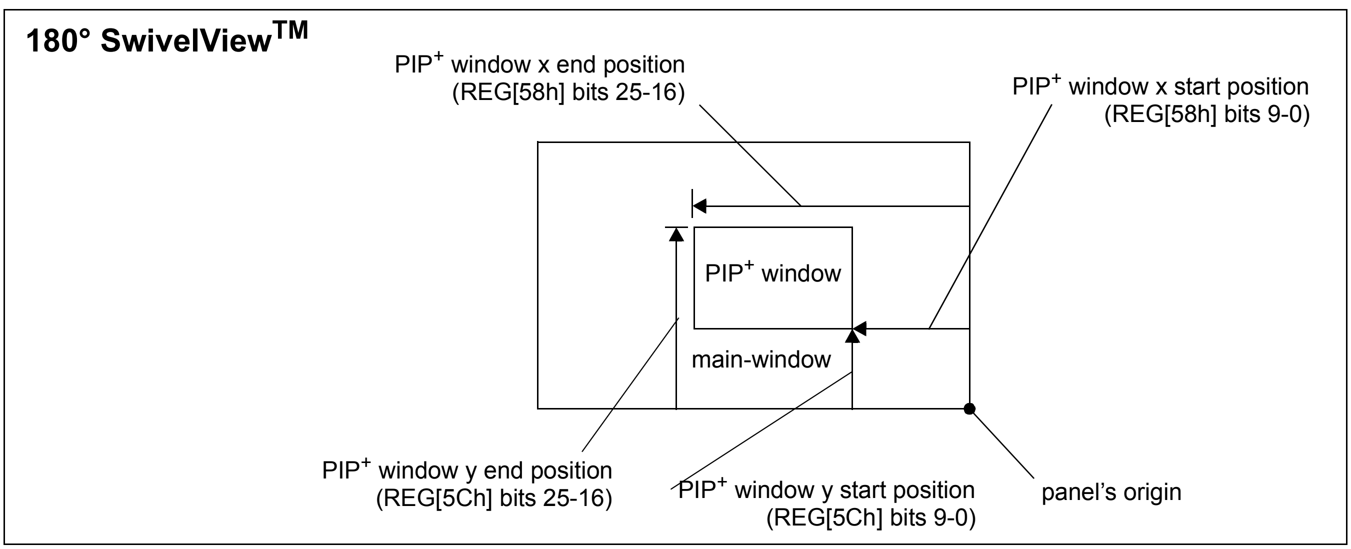


Figure 14-3: Picture-in-Picture Plus with SwivelView 180° enabled

14.2.3 SwivelView 270°

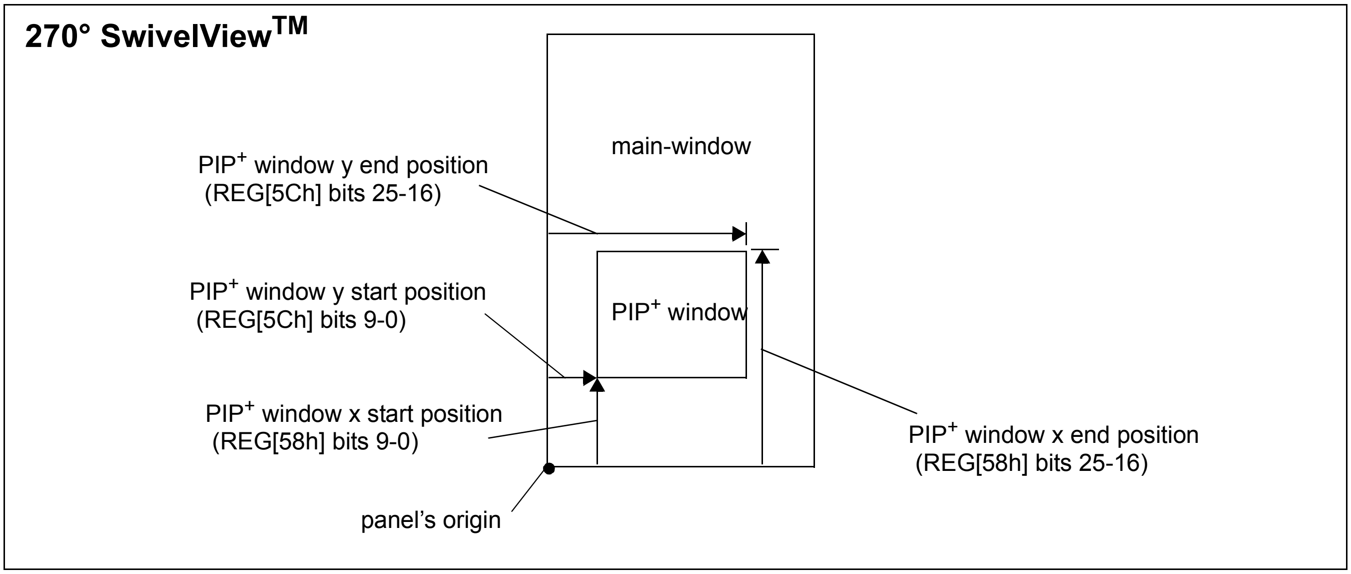


Figure 14-4: Picture-in-Picture Plus with SwivelView 270° enabled

15 Power Save Mode

A software initiated Power Save Mode is incorporated into the S1D13A04 to accommodate the need for power reduction in the hand-held devices market. This mode is enable via the Power Save Mode Enable bit (REG[14h] bit 4).

Software Power Save Mode saves power by powering down the control signals and stopping display refresh accesses to the display buffer. For programming information on disabling the clocks, see the *S1D13A04 Programming Notes and Examples*, document number X37A-G-003-xx.

Table 15-1: Power Save Mode Function Summary

	Software Power Save	Normal
IO Access Possible?	Yes	Yes
Memory Writes Possible?	Yes[1]	Yes
Memory Reads Possible?	No[1]	Yes
Look-Up Table Registers Access Possible?	Yes	Yes
USB Registers Access Possible?	No	Yes
Display Active?	No	Yes
LCD I/F Outputs	Forced Low	Active
PWMCLK	Stopped	Active
Access Possible for GPIO pins configured for HR-TFT?	Forced Low	Active
Access Possible for GPIO Pins configured as GPIOs?	Yes[2]	Yes
USB Running?	No	Yes

Note

[1] When power save mode is enabled, the memory controller is powered down and the status of the memory controller is indicated by the Memory Controller Power Save Status bit (REG[14h] bit 6). However, memory writes are possible during power save mode because the S1D13A04 dynamically enables the memory controller for display buffer writes. **This ability does not increase power consumption.**

[2]GPIOs can be accessed, and if configured as outputs can be changed.

After reset, the S1D13A04 is always in Power Save Mode. Software must initialize the chip (i.e. programs all registers) and then clear the Power Save Mode Enable bit. For further details, see the register description for REG[14h] bit 4.

16 Mechanical Data

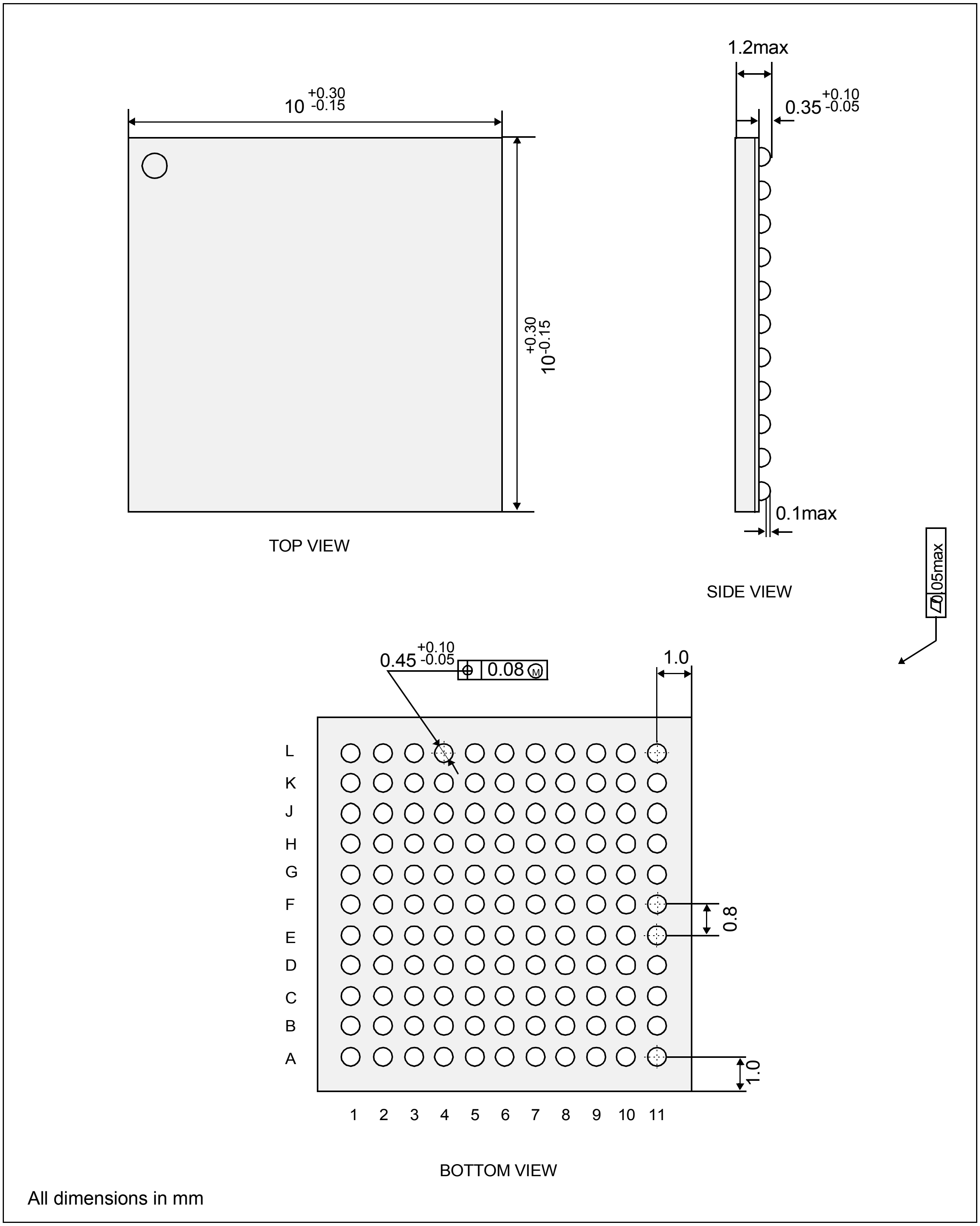
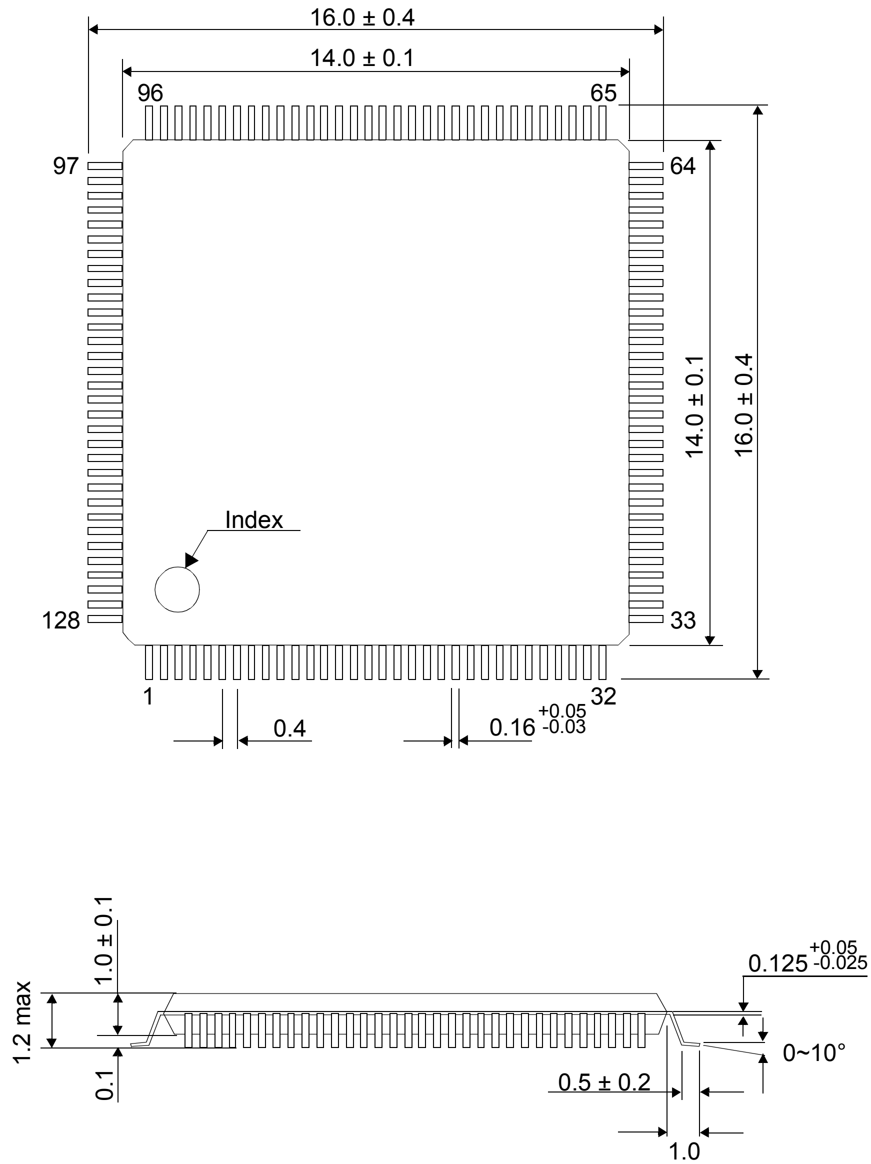


Figure 16-1: Mechanical Data PFBGA 121-pin Package



All dimensions in mm

Figure 16-2: Mechanical Data TQFP15 128-pin Package

17 Change Record

X37A-A-001-07 Revision 7.6 - Issued: March 14, 2018

- updated Sales and Technical Support Section
- Updated some formatting

X37A-A-001-07 Revision 7.5 - Issued: December 18, 2008

- all changes from the previous revision are in Red
- section 18 - updated Sales and Technical Support addresses

X37A-A-001-07 Revision 7.4 - Issued: February 13, 2008

- all changes from the previous revision are in Red
- Release as revision 7.4 to align with Japan numbering
- section 18 References - remove references to obsolete application notes and change "Interfacing to the Motorola MCF5307..." to "Interfacing to the Freescale MCF5307..."

X37A-A-001-07 Revision 7.03 - Issued: September 17, 2007

- all changes from the previous revision are in Red
- section 17, updated the References
- section 18, updated the Sales and Technical Support addresses

X37A-A-001-07 Revision 7.02 - Issued: August 10, 2007

- all changes from the previous revision are in Red
- section 4.3.1, corrected the PFBGA and TQFP Pin# listing for the AB[17:1] pin description
- section 4.3.2, clarified the TQFP Pin# listing for the FPDAT[17:0] pin description

X37A-A-001-07 Revision 7.01 - Issued: June 13, 2007

- all changes from the previous revision are in Red
- section 4.3.1, corrected the PFBGA Pin# listing for the DB[15:0] pin description
- section 19, updated the Sales and Technical Support information

X37A-A-001-07 Revision 7.0 - Issued: July 7, 2006

- all changes from the previous revision are in Red
- add section 6.2 RESET# Timing

18 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html