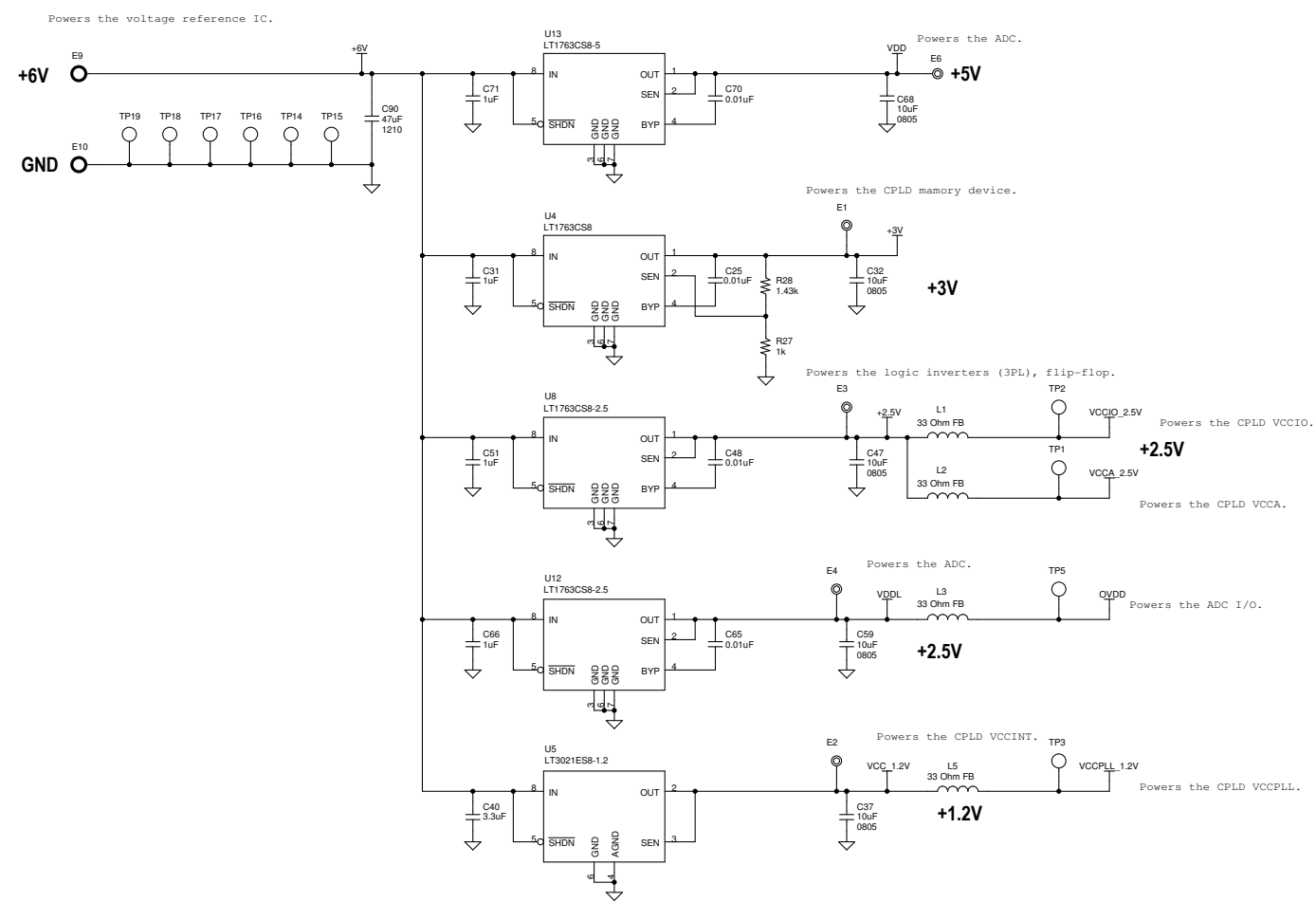


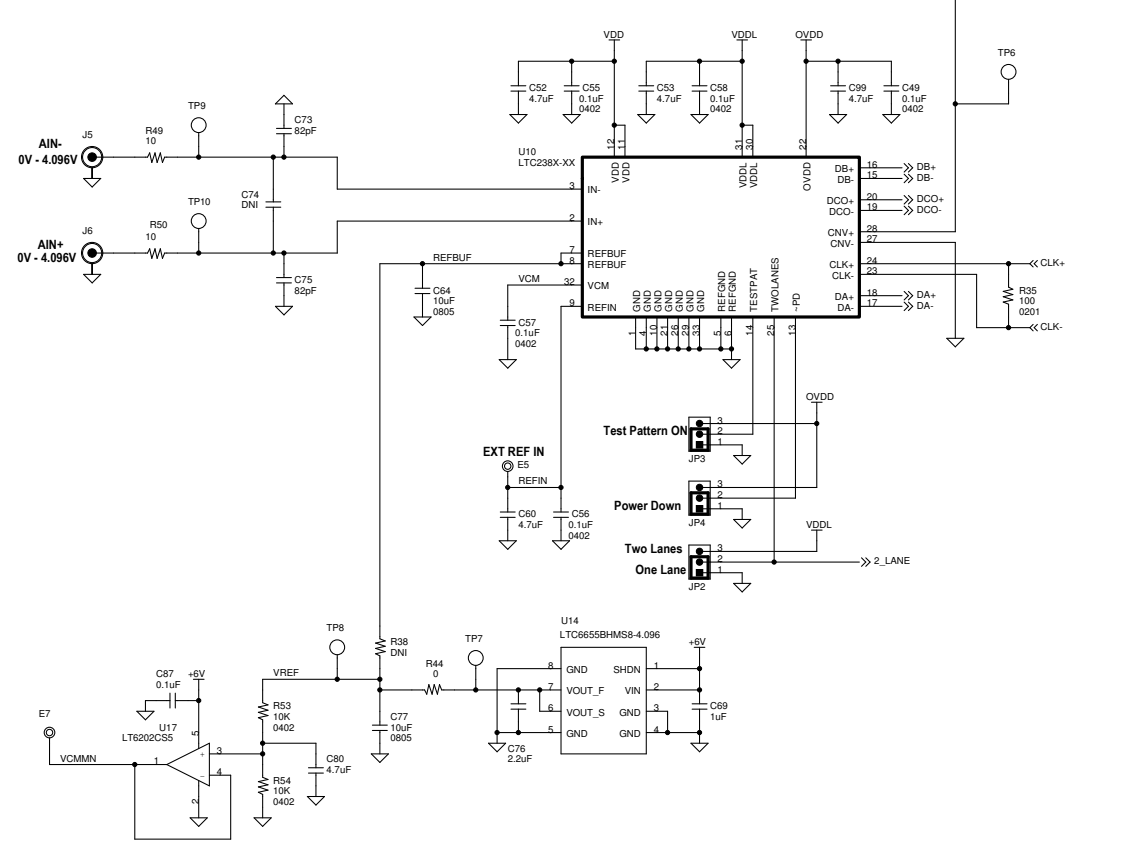
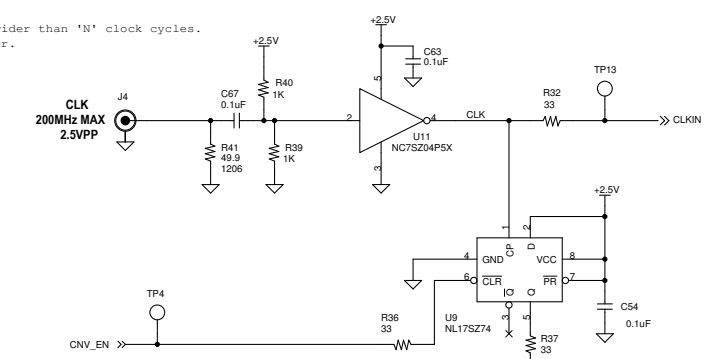
REVISION HISTORY				
ECO	REV	DESCRIPTION	APPROVED	DATE
	0	PRODUCTION	DOUG S.	08-26-13



* ASSY U10 BITS MspS R33 R34

-A	LTC2387CUH-18	18	15	1K	DNI
-B	LTC2387CUH-16	16	15	DNI	1K
-C	LTC2386CUH-18	18	10	1K	DNI
-D	LTC2386CUH-16	16	10	DNI	1K
-E	LTC2385CUH-18	18	5	1K	DNI
-F	LTC2385CUH-16	16	5	DNI	1K

This circuit conditions the edges of the CNV pulse as follows:
 The rising edge of CNV is driven by a rising edge of CLKIN.
 The falling edge of CNV is driven by a falling edge of CNV_EN, so it is wider than 'N' clock cycles.
 The circuit serves to eliminate jitter on the CNV pulse due to CPLD jitter.
 The rising edge of the CNV pulse is thus driven by CLKIN, not CNV_EN.



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS, 0603.
 ALL CAPACITORS ARE IN MICROFARADS, 0603

CUSTOMER NOTICE		APPROVALS		LINEAR TECHNOLOGY		
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.		PCB DES.	D. STUETZLE	1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 www.linear.com Fax: (408)434-0507 LTC Confidential-For Customer Use Only		
		APP ENG.	D. STUETZLE			
		THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		SCALE = NONE	TITLE: SCHEMATIC 18-Bit, 15Mps SAR ADC	
				DATE:	Wednesday, May 27, 2015	SHEET 1 OF 2

