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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E24RG68060LWAM450-R

Overview:

- 2.4-inch TFT: 240x320 (42.72x60.26)
- 16/18- bit RGB
- 8/9/16/18-bit MCU
- 3-line/4-line Serial Interface
- White LED back-light
- Transmissive/ Normally Black
- 4-wire Resistive Touch Screen
- 450 NITS
- Controller: ST7789V
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.4" TFT-LCD contains 240X320 pixels, and can display up to 65K/262K colors

Features

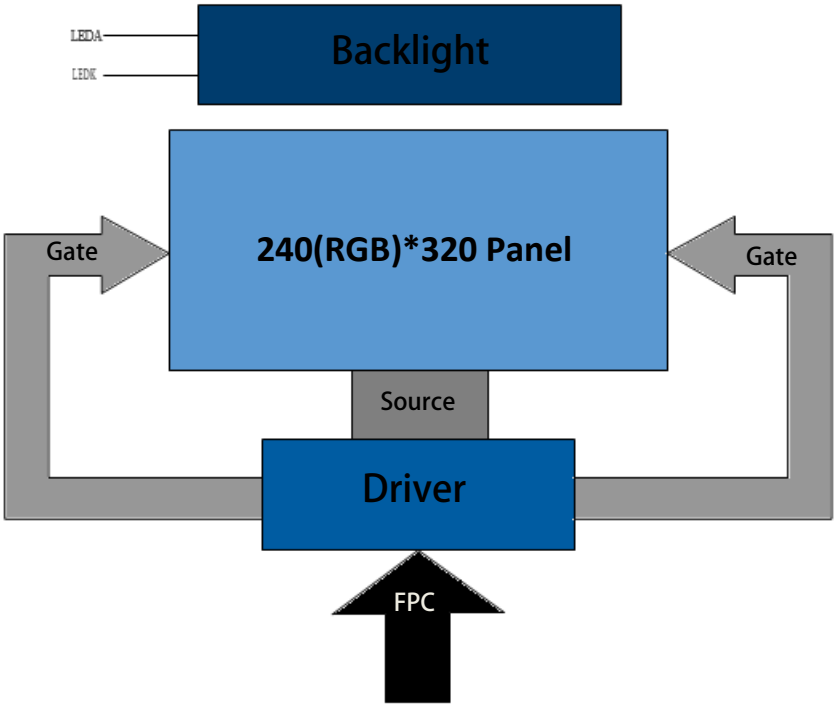
Low Input Voltage: 3.3V (TYP)
Display Colors of TFT LCD: 65K/262K colors
TFT Interface:
8/9/16/18Bit MCU;
16/18Bit RGB
3-line/4-line Serial Interface

General Information Items	Specification	Unit	Note
	Main Panel		
Display area (AA)	36.72(H)*48.96(V) (2.4inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*320	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.051(H)*0.051(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7789V	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

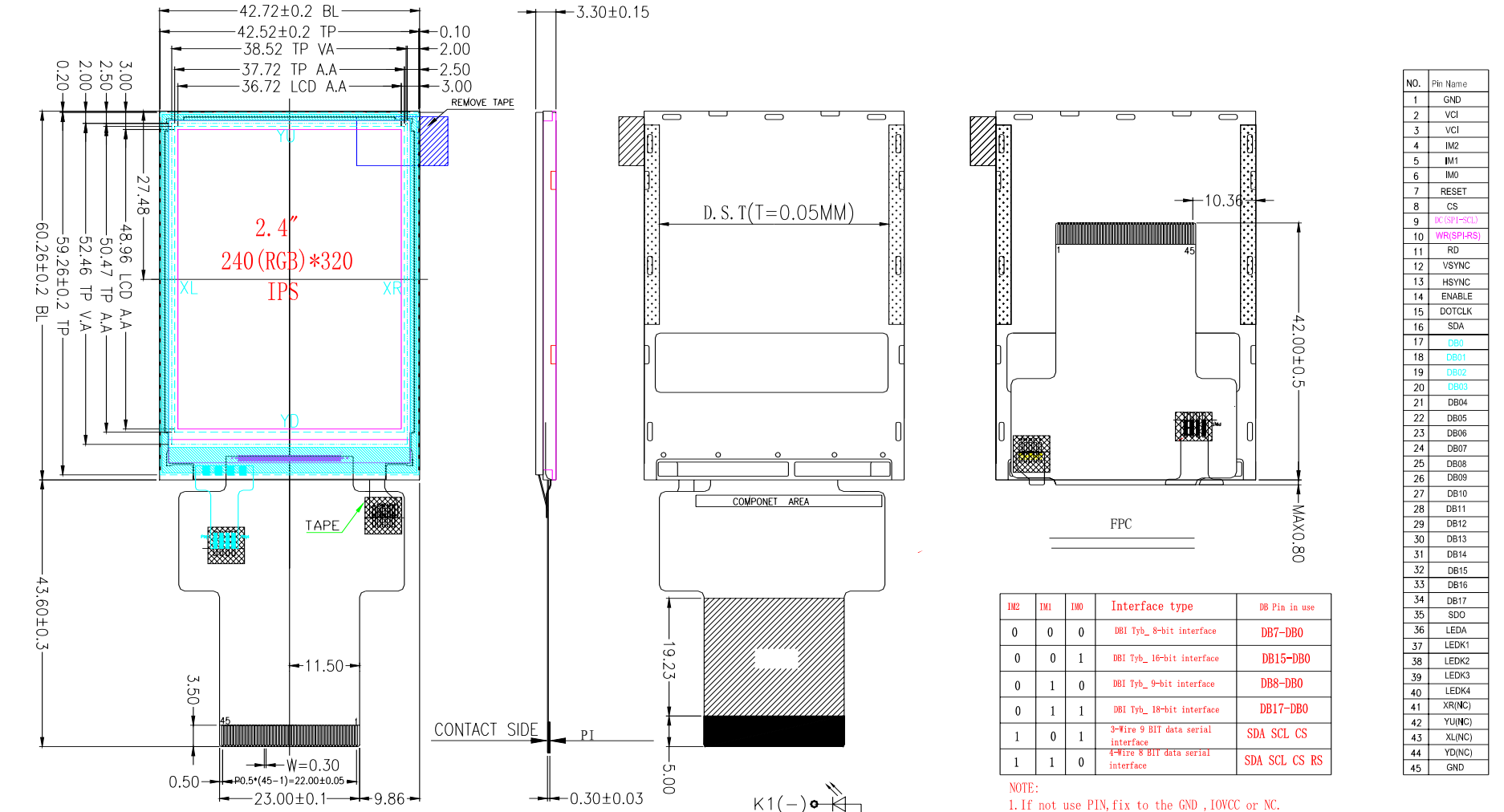
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Horizontal(H)		42.72		mm	-
	Vertical(V)		60.26		mm	-
	Depth(D)		3.3		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline Dimensions



BLU CIRCUIT DIAGRAM

NO.	Pin Name
1	GND
2	VCI
3	VCI
4	IM2
5	IM1
6	IM0
7	RESET
8	CS
9	DC(SPI-SCL)
10	WR(SPI-RS)
11	RD
12	VSYNC
13	HSYNC
14	ENABLE
15	DOTCLK
16	SDA
17	DB0
18	DB01
19	DB02
20	DB03
21	DB04
22	DB05
23	DB06
24	DB07
25	DB08
26	DB09
27	DB10
28	DB11
29	DB12
30	DB13
31	DB14
32	DB15
33	DB16
34	DB17
35	SDO
36	LEDA
37	LEDK1
38	LEDK2
39	LEDK3
40	LEDK4
41	XR(NC)
42	YU(NC)
43	XL(NC)
44	YD(NC)
45	GND

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 8-bit interface	DB7-DB0
0	0	1	DBI Tyb_ 16-bit interface	DB15-DB0
0	1	0	DBI Tyb_ 9-bit interface	DB8-DB0
0	1	1	DBI Tyb_ 18-bit interface	DB17-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDA SCL CS
1	1	0	4-Wire 8 BIT data serial interface	SDA SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.
2. If use RGB mode must select serial interface

NOTES:
1. DISPLAY TYPE: 2.4", TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: IPS NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. DRIVER IC: ST7789V (COG)
5. VCI: 3.3V
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 4 LED, 80mA, 3.2±0.3V
8. RoHS COMPLIANT.

ReV.	Revision content description	Date
A	FIRST	2013/03/29

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TOLERANCE( )		DRAWING NAME		
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3 X.XX±0.2	Drawn		Unit
		Checked		mm
Scale 1:1		Approve		Page 1/1

3. Input Terminal Pin Assignment

Recommended TFT Connector: FH12S-45S-0.5SH(55) | Recommended RTP Connector: FH33-4S-1SH(10)

NO.	Symbol	Description	I/O
1	GND	Ground.	P
2	VCI	Supply voltage (3.3V)	P
3	VCI	Supply voltage (3.3V)	P
4	IM2	MPU parallel interface bus and serial interface select if use RGB interface must select serial interface. Fix this pin at VCI and GND	I
5	IM1		I
6	IM0		I
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin (“Low” enable). Fix this pin at VCI or GND when not in use.	I
9	DC(SPI-SCL)	Display data/command selection pin in parallel interface. This pin is used to be serial interface clock. D/CX=’1’: display data or parameter. D/CX=’0’: command data. If not used, please fix this pin at VCI or GND.	I
10	WR(SPI_RS,SDA2)	The data is applied on the rising edge of the SCL signal. Second Data lane in 2 data lane serial interface. If not used, fix this pin at VCI or GND.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at VCI or GND when not in use.	I
12	VSYNC	Frame synchronizing signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
13	HSYNC	Line synchronizing signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
14	ENABLE	Data enable signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
15	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
16	SDA1	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
17-34	DV0-DB17	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND level when not in use.	I/O
35	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. If not used, let this pin open.	O
36	LEDA	Anode pin of backlight.	P
37	LEDK1	Cathode pin of backlight.	P
38	LEDK2	Cathode pin of backlight.	P
39	LEDK3	Cathode pin of backlight.	P
40	LEDK4	Cathode pin of backlight.	P
41	XR	Touch panel right glass terminal.	A/D
42	YU	Touch panel top film terminal.	A/D
43	XL	Touch panel lift glass terminal.	A/D
44	YD	Touch panel bottom film terminal.	A/D
45	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Transmittance (with Polarizer)		T(%)		--	4.65	--	%	(3)
Transmittance (without Polarizer)		T(%)		--	14.6	--	%	(3)
Contrast Ratio		CR	Θ=0 Normal viewing angle	600	800	--		(1)(2)
Response time	Rising	TR		--	16	21	msec	(4)
	Falling	TF			19	24		
Color gamut		S (%)		--	70	--	%	(5)
Color Filter Chromaticity	White	W_X		0.290	0.310	0.330		(1)(5) CF glass
		W_Y		0.316	0.336	0.356		
	Red	R_X		0.627	0.647	0.667		
		R_Y		0.297	0.317	0.337		
	Green	G_X		0.255	0.275	0.295		
		G_Y		0.562	0.582	0.602		
	Blue	B_X		0.120	0.140	0.160		
		B_Y		0.068	0.088	0.108		
Viewing angle	Hor.	ΘL	CR>10	--	80	--		(1)(6) Ref only
		ΘR		--	80	--		
	Ver.	ΘU		--	80	--		
		ΘD		--	80	--		
Option View Direction		FREE						

4.2 Measuring conditions

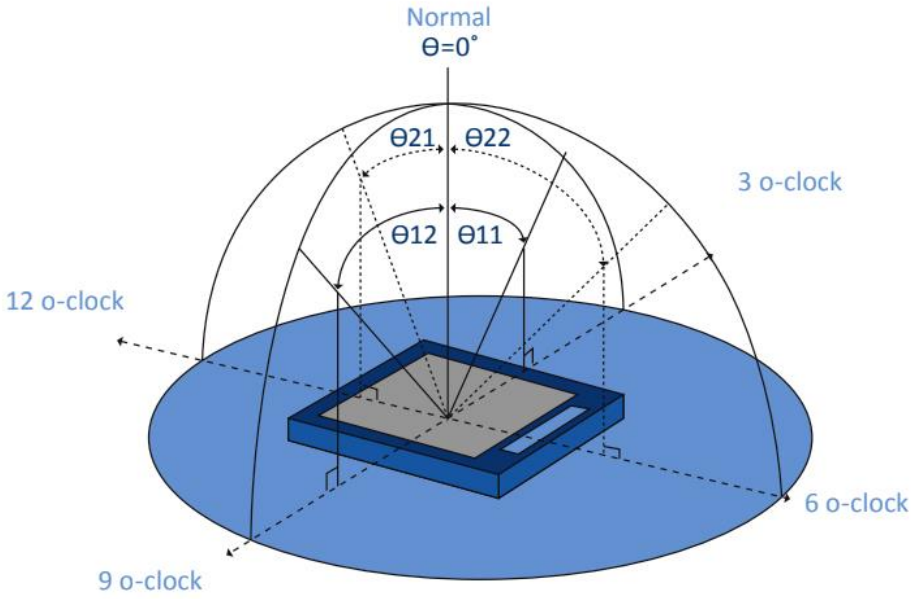
Measuring surrounding: dark room
Ambient temperature: 25±2 ℃
15min. warm-up time.

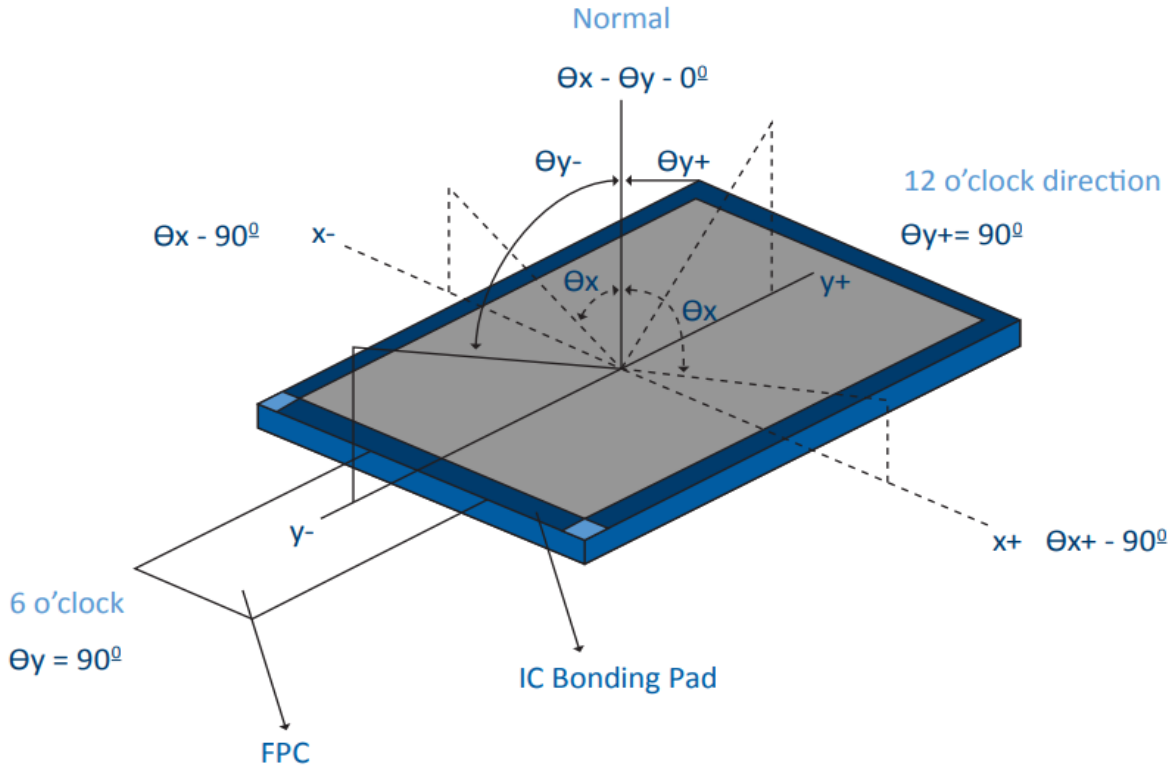
4.3 Measuring Equipment

FPM520 of Westar Display technologies, INC, which utilized SR-3 for Chromaticity and BM-SA for other optical characteristics.

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

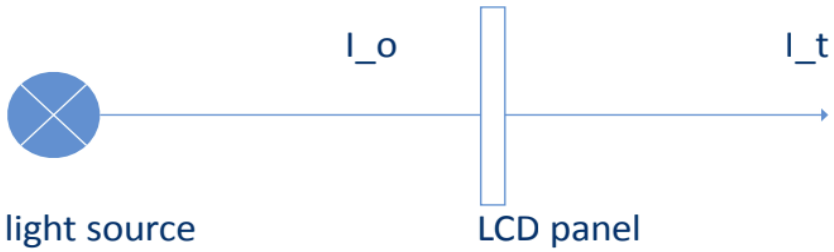




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

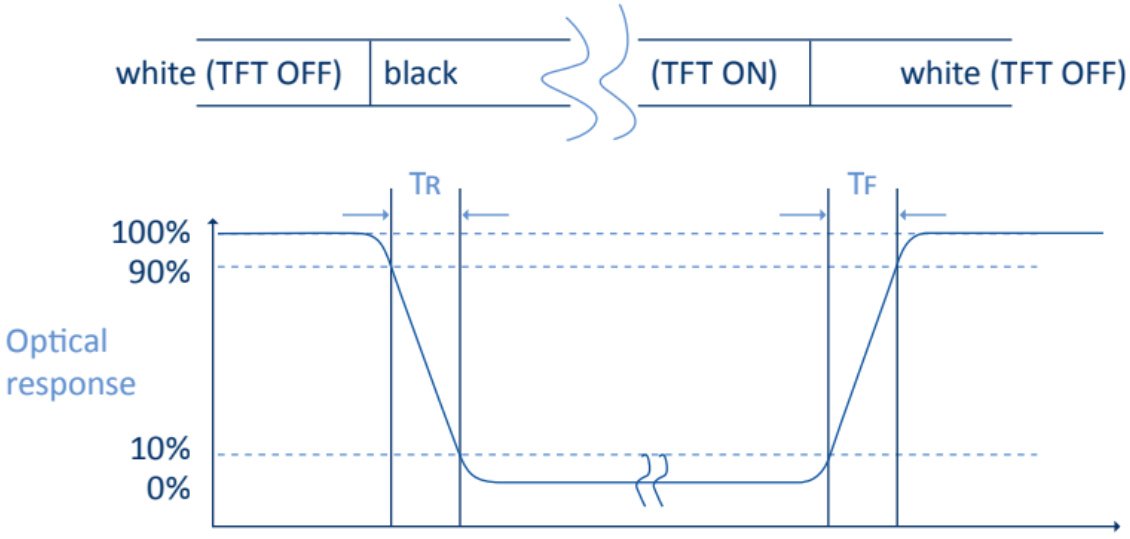


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

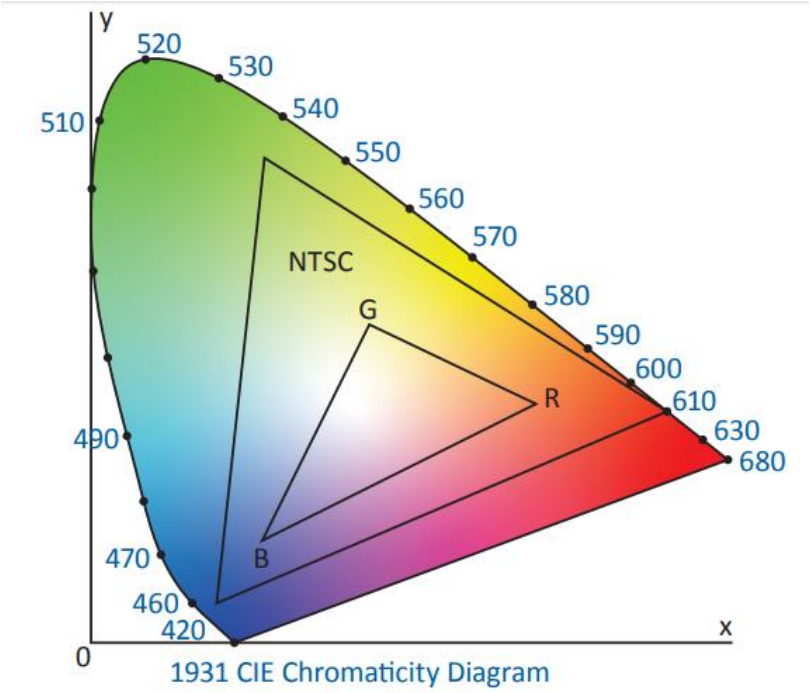
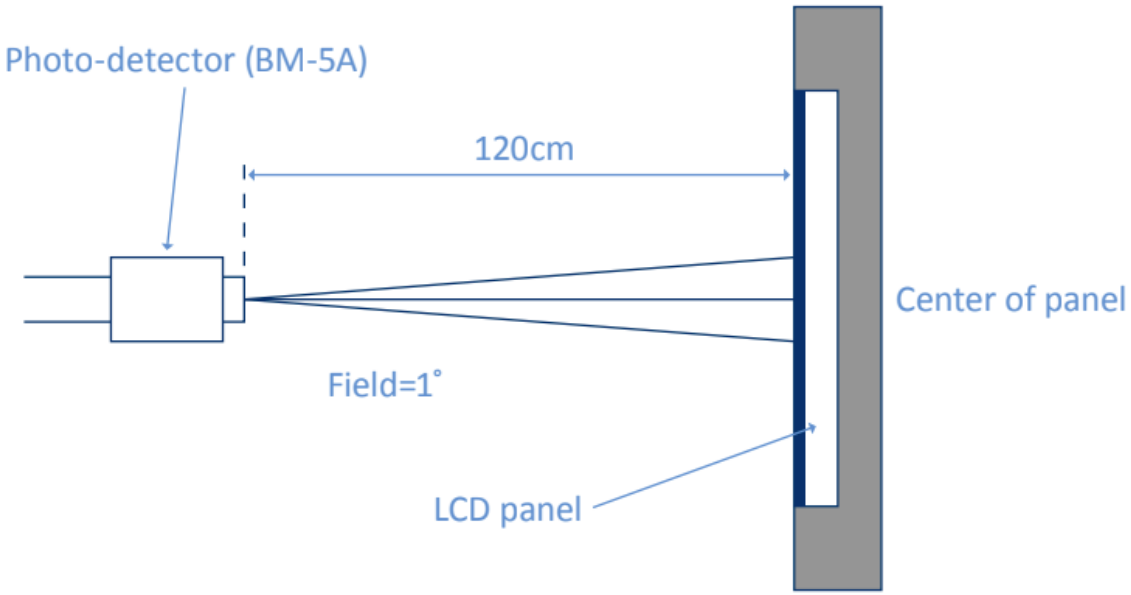


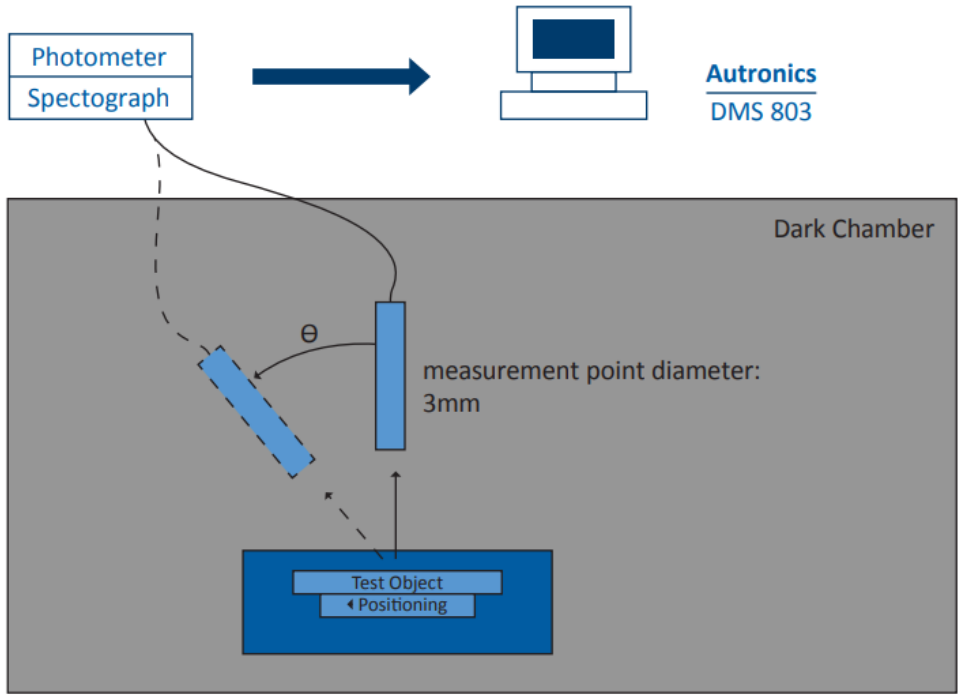
Fig. 1931 CIE chromacity diagram

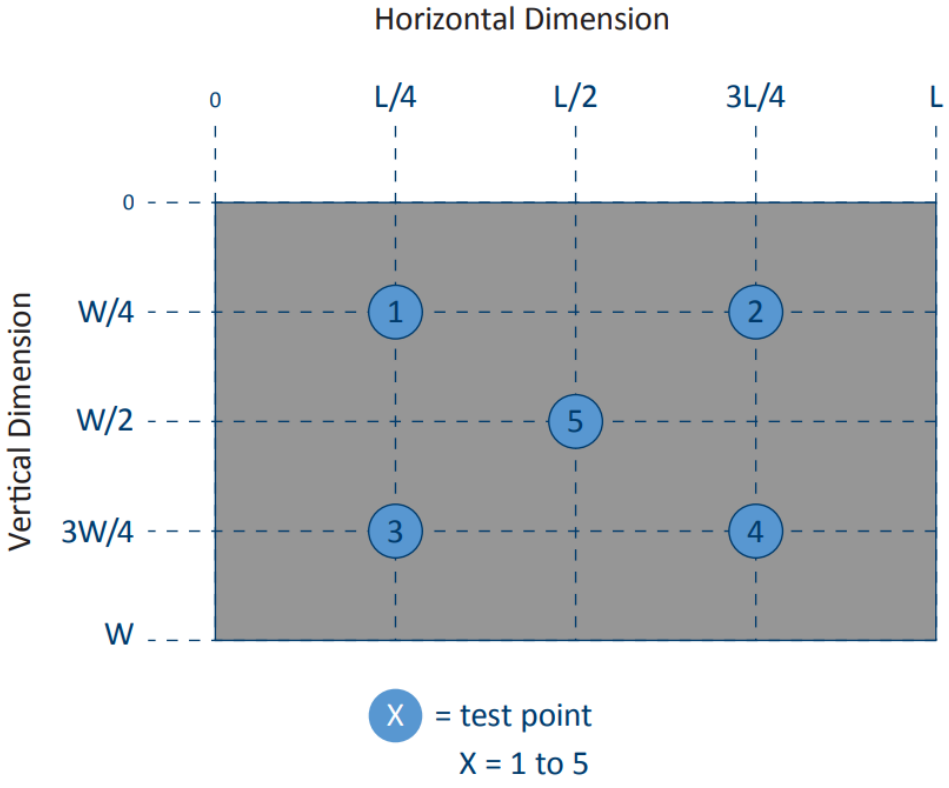
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Interface Operation Voltage	VDDIO	-0.3	4.6	V
Operating temperature	TOP	-20	+70	℃
Storage temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.6	3.3	4.2	V	
Interface Operation Voltage	VDDIO	1.65	1.8	4.2	V	
Normal Mode Current Consumption	IDD	--	8	--	mA	
Level input voltage	VIH	0.7 VDDIO		VDDIO	V	
	VIL	GND		0.3 VDDIO	V	
Level output voltage	VOH	0.8 VDDIO		VDDIO	V	
	VOL	GND		0.2 VDDIO	V	

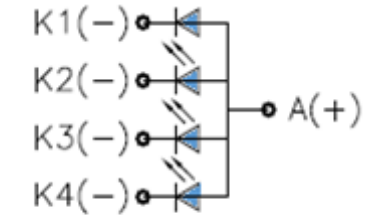
5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	60	80	--	mA	
Forward Voltage	VF	--	3.2	--	V	
LCM Luminance	LV	450	--	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 4 chips White LED

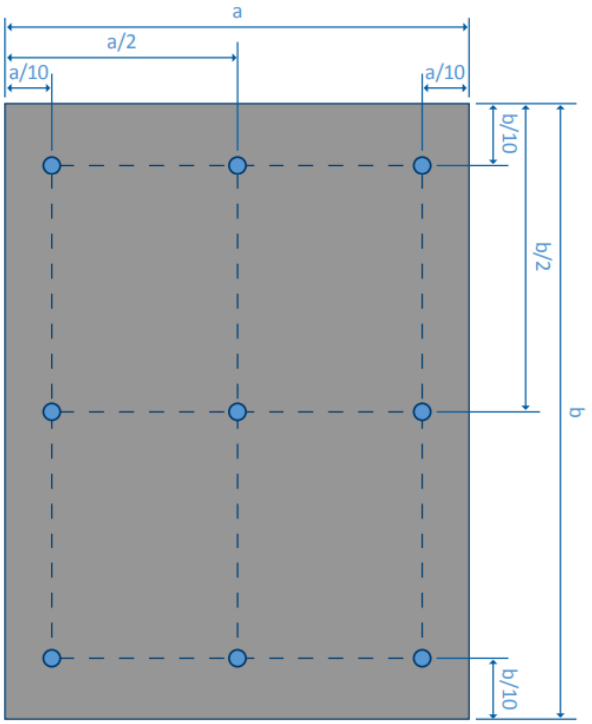
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



BLU CIRCUIT DIAGRAM

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristic

6.1 RGB Interface Timing Characteristics

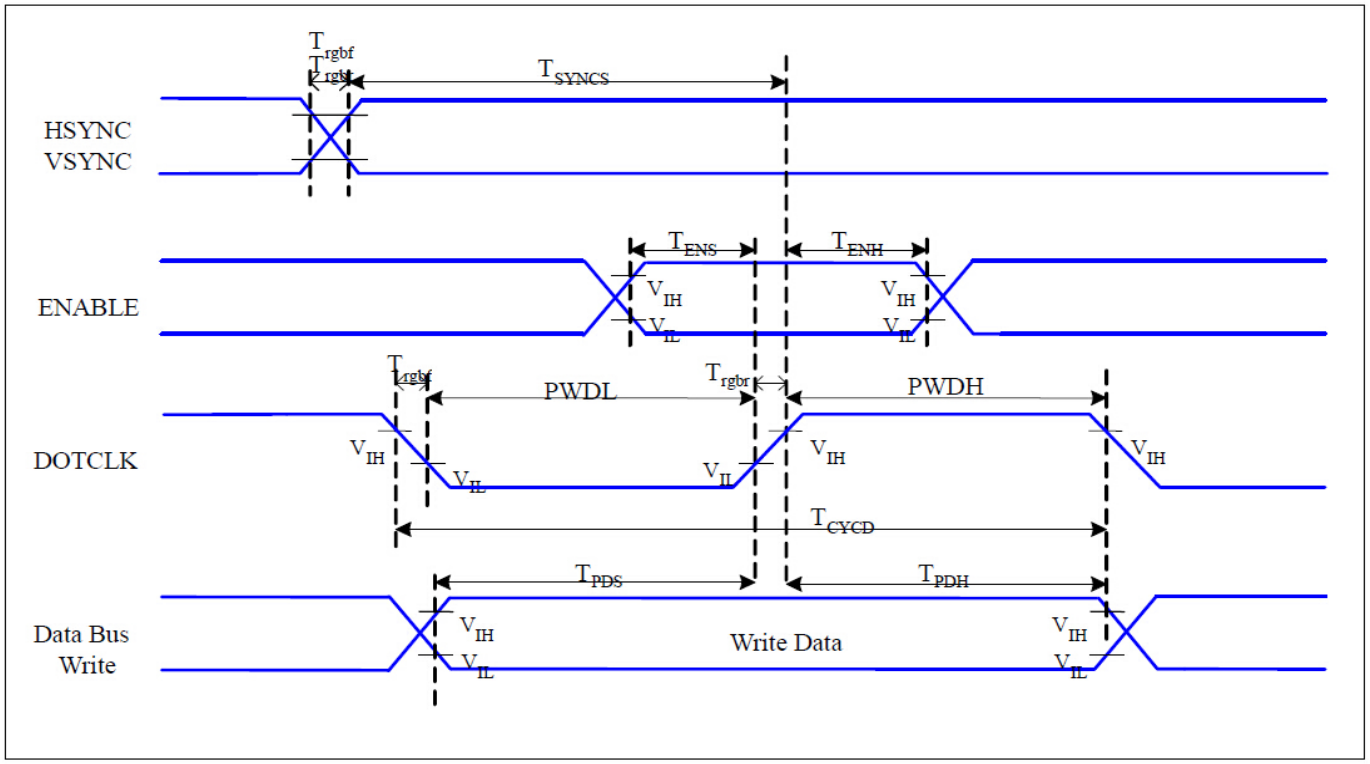


Figure 6.1: RGB Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	100	-	ns	
	T_{RGHR}, T_{RGH}	DOTCLK Rise/Fall Time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

Table 6.1: 18/16 Bit RGB Interface Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	100	-	ns	
	T_{RGHR}, T_{RGH}	DOTCLK Rise/Fall Time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

Table 6.2: 6 Bit RGB Interface Timing Characteristics

6.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080 system)

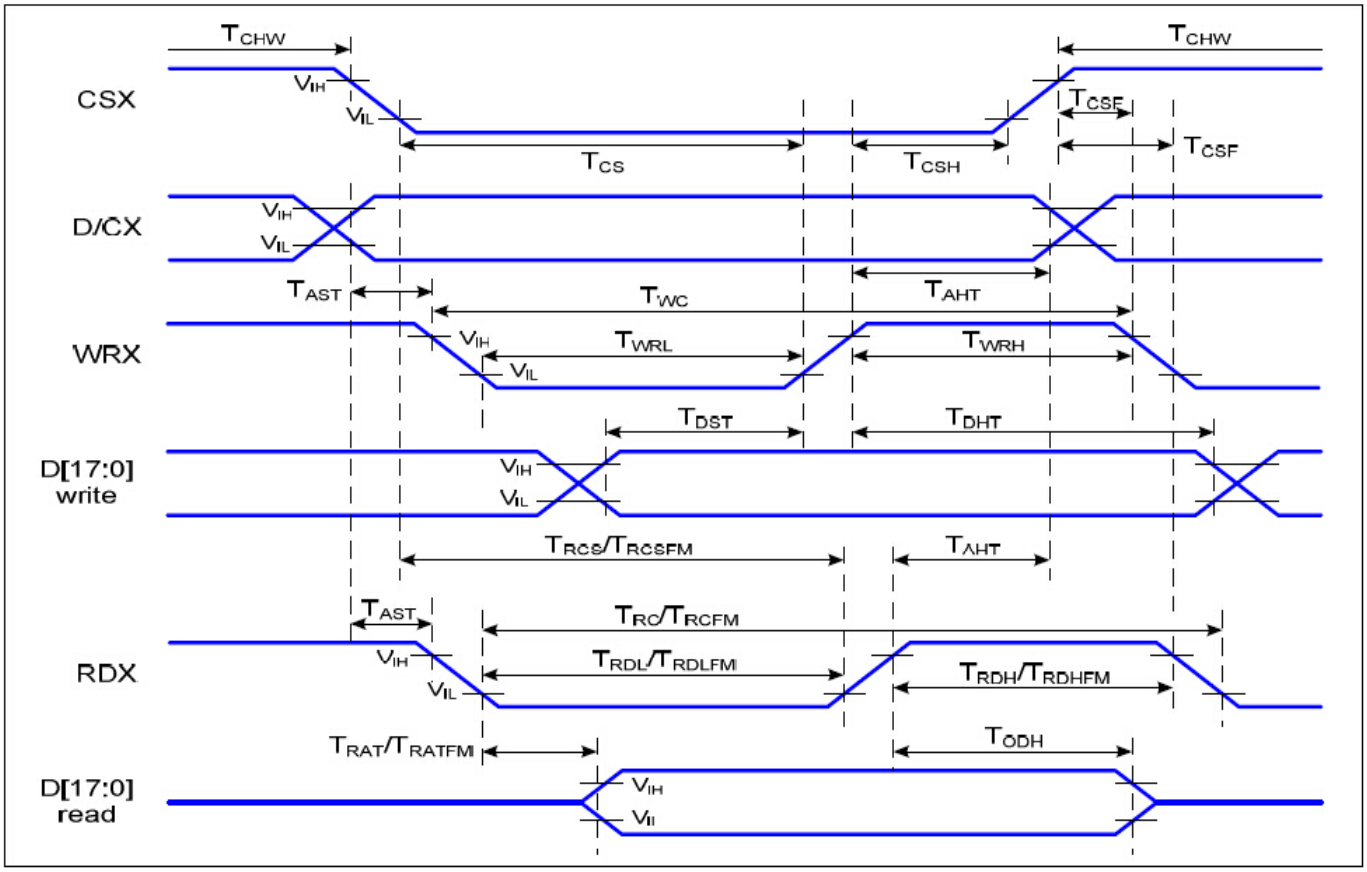
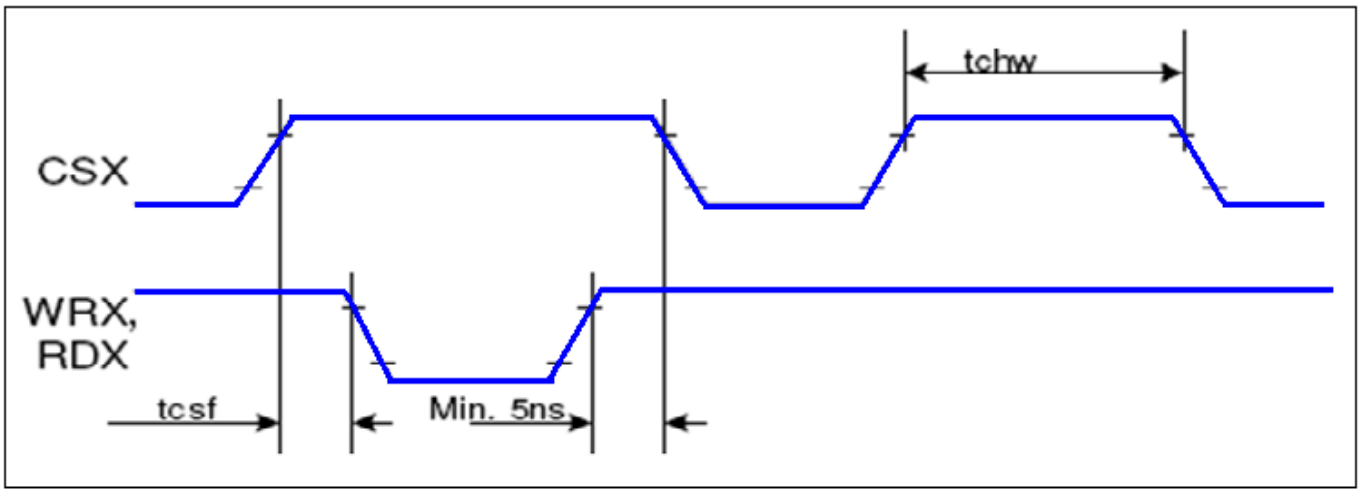


Figure 6.2: 8080 MCU Parallel Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0	-	ns	
	T_{AHT}	Address hold time (Write/Read)	0	-	ns	
CSX	T_{CHW}	Chip select “H” pulse width	0	-	ns	
	T_{CS}	Chip select setup time (Write)	15	-	ns	
	T_{RCS}	Chip select setup time (Read ID)	45	-	ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T_{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T_{CSH}	Chip select hold time	10	-	ns	
WRX	T_{WC}	Write cycle	66	-	ns	
	T_{WRH}	Control pulse “H” duration	15	-	ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90	-	ns	
	T_{RDL}	Control pulse “L” duration	45	-	ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90	-	ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355	-	ns	
D[17:0] D[15:0], D[8:0], D[7:0]	T_{DST}	Write data setup time	10	-	ns	For max CL=30pF For min CL=8pF
	T_{DHT}	Write data hold time	10	-	ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ROD}	Output disable time	20	80	ns	

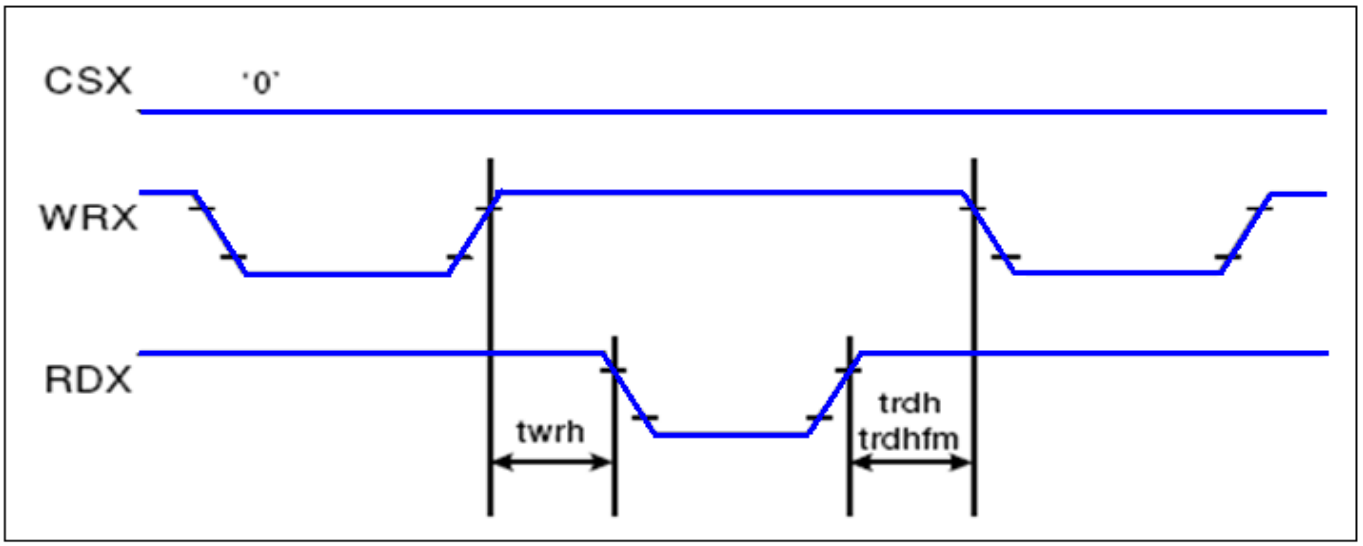
Table 6.3: 8080 Parallel Interface Characteristics

CSX timings:

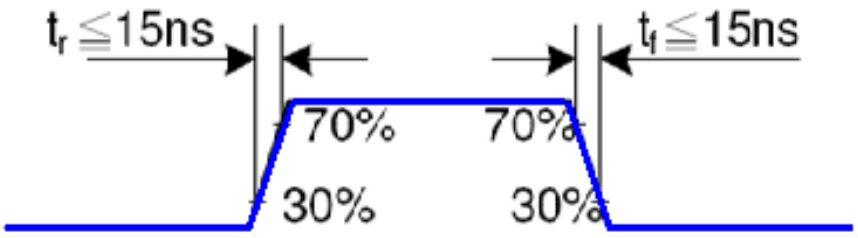


Note: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

Write to read or read to write timings:



Note: Ta = -30 to 70 C, IOVCC = 1.65V to 2.8V, VCI = 2.6V to 3.3V, GND = 0V.



6.3 Display Serial Interface Characteristics (3-line SPI system)

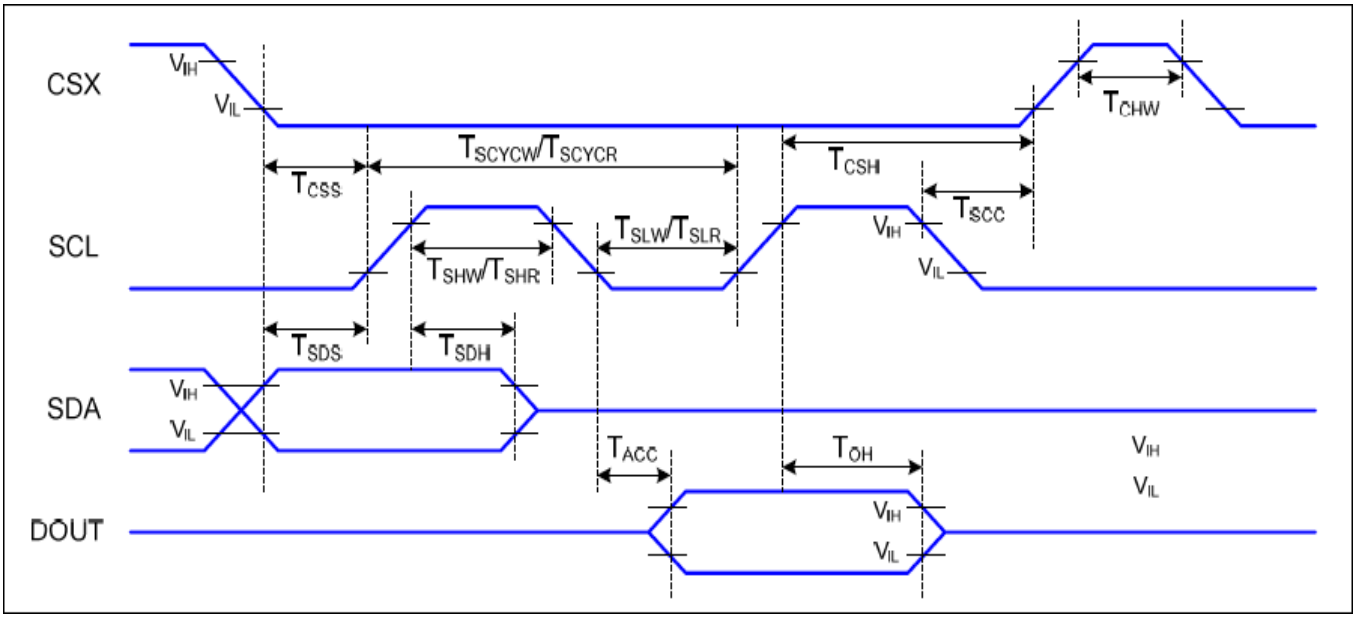


Figure 6.3: 3-Line Serial Interface Timing Diagram

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	20		ns	
	T_{CSH}	Chip select hold time (write)	20		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	100		ns	
	T_{SHW}	SCL “H” pulse width (write)	40		ns	
	T_{SLW}	SCL “L” width (write)	40		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	30		ns	
	T_{SDH}	Data hold time	30			
DOUT	T_{ACC}	Access time	10		ns	For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	10	50		

Table 6.4: 3-Line Serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.4 Display Serial Interface Characteristics (4-line SPI serial)

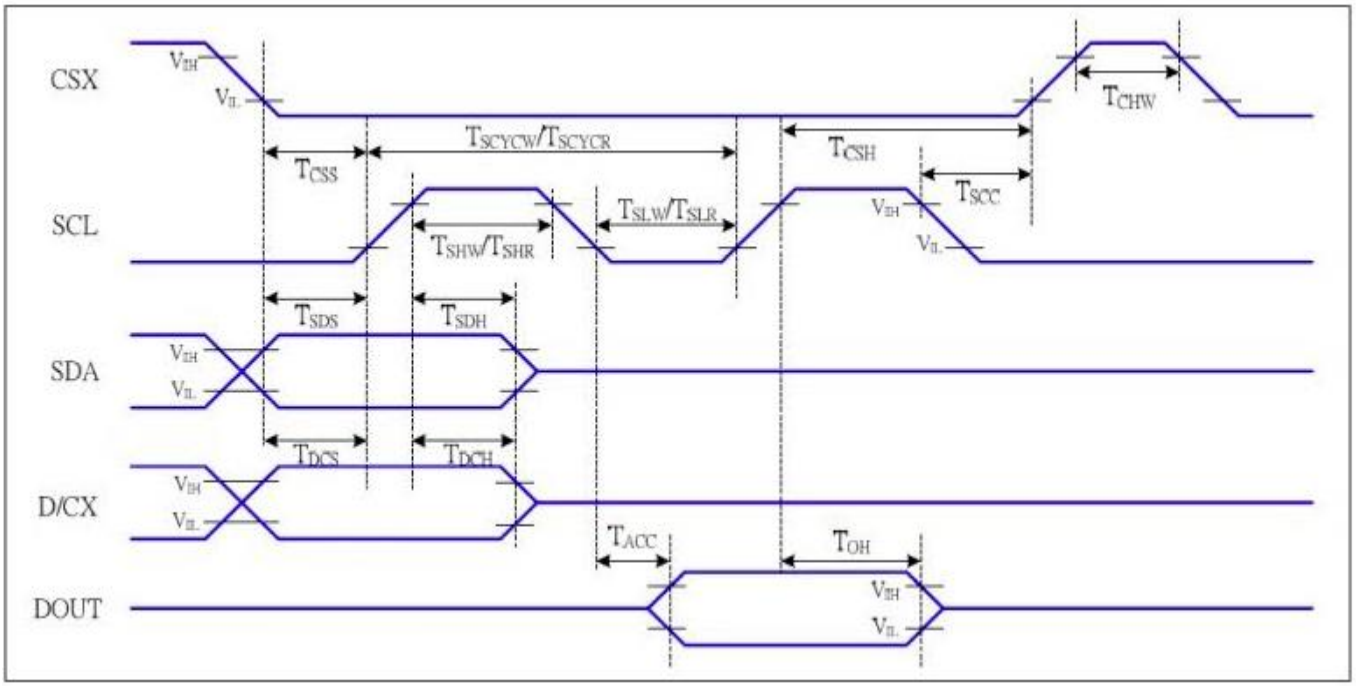


Figure 6.4: 4-Line Serial Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	40		ns	
	T_{CSH}	Chip select hold time (write)	40		ns	
	T_{CSS}	Chip select setup time (read)	40		ns	
	T_{SCC}	Chip select hold time (read)	40		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	100		ns	write command & data ram
	T_{SHW}	SCL “H” pulse width (write)	40		ns	
	T_{SLW}	SCL “L” width (write)	40		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	read command & data ram
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	30		ns	
	T_{SDH}	Data hold time	30		ns	
DOUT	T_{ACC}	Access time	10		ns	For max CL=30pF
	T_{OH}	Output disable time	10	50	ns	For min CL=8pF

Table 6.5: 4-Line Serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.5 Reset Timing

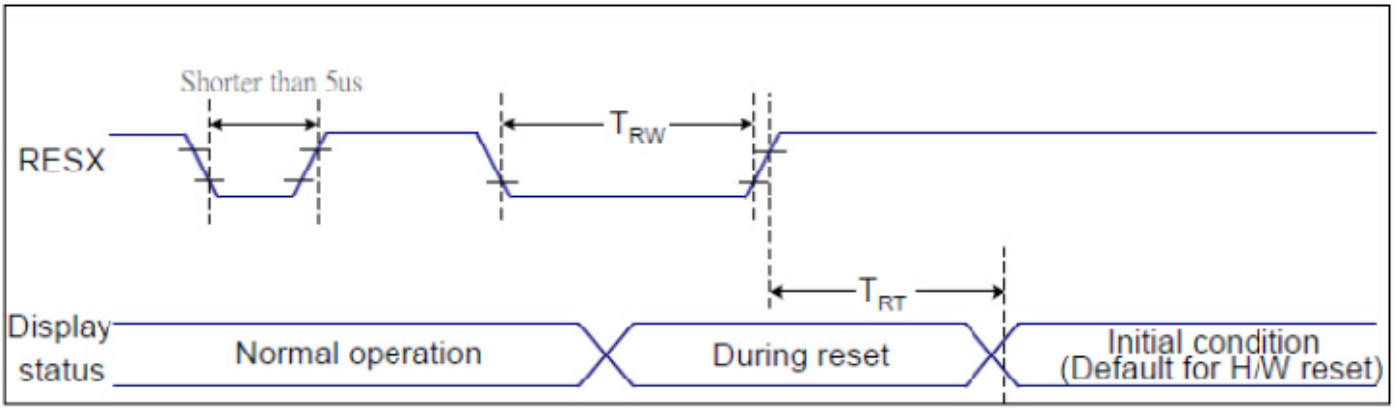


Figure 6.5: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

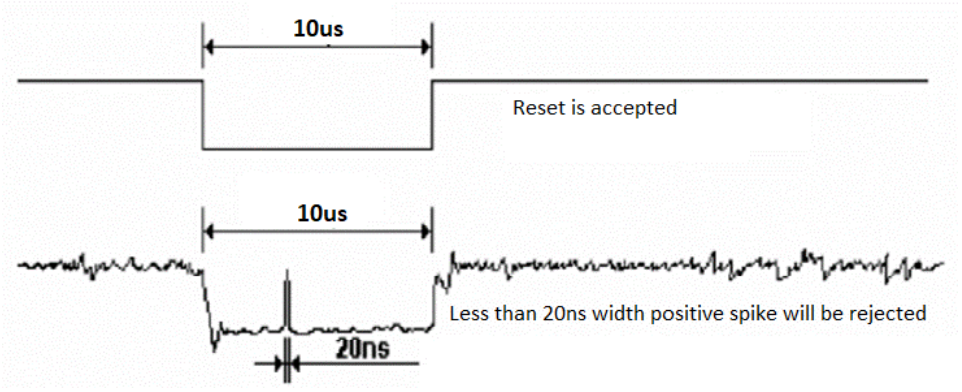
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.