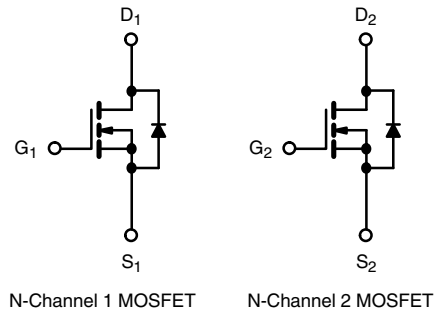
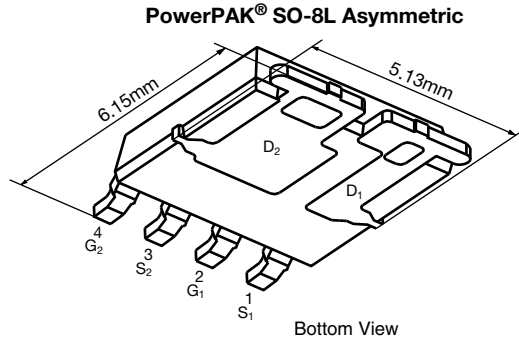
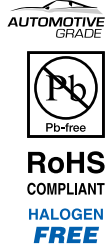


Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFETs

| PRODUCT SUMMARY | | |
|---|-------------|-------------|
| | N-CHANNEL 1 | N-CHANNEL 2 |
| V_{DS} (V) | 40 | 40 |
| $R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V | 0.022 | 0.011 |
| $R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V | 0.026 | 0.013 |
| I_D (A) | 15 | 45 |
| Configuration | Dual N | |

FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



| ORDERING INFORMATION | |
|---------------------------------|--------------------------------|
| Package | PowerPAK SO-8L Dual Asymmetric |
| Lead (Pb)-free and Halogen-free | SQJ942EP-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted) | | | | | |
|---|----------------|----------------|-------------|------|----|
| PARAMETER | SYMBOL | N-CHANNEL 1 | N-CHANNEL 2 | UNIT | |
| Drain-Source Voltage | V_{DS} | 40 | 40 | V | |
| Gate-Source Voltage | V_{GS} | ± 20 | | | |
| Continuous Drain Current ^a | I_D | $T_C = 25$ °C | 15 | 45 | A |
| | | $T_C = 125$ °C | 15 | 32 | |
| Continuous Source Current (Diode Conduction) ^a | I_S | 15 | 44 | mJ | |
| Pulsed Drain Current ^b | I_{DM} | 60 | 180 | | |
| Single Pulse Avalanche Current | I_{AS} | 19 | 27 | | |
| Single Pulse Avalanche Energy | E_{AS} | 18.5 | 36.5 | W | |
| Maximum Power Dissipation ^b | P_D | $T_C = 25$ °C | 17 | | 48 |
| | | $T_C = 125$ °C | 6 | 16 | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 175 | | °C | |
| Soldering Recommendations (Peak Temperature) ^{e, f} | | 260 | | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|----------------------------|------------|-------------|-------------|------|--|
| PARAMETER | SYMBOL | N-CHANNEL 1 | N-CHANNEL 2 | UNIT | |
| Junction-to-Ambient | R_{thJA} | 75 | 70 | °C/W | |
| Junction-to-Case (Drain) | R_{thJC} | 9 | 3.1 | | |

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | | |
|--|--------------|---|---|--------|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 1 | 40 | - | - | V |
| | | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 2 | 40 | - | - | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 1 | 1.3 | 1.8 | 2.3 | V |
| | | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 2 | 1.3 | 1.8 | 2.3 | |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | N-Ch 1 | - | - | ± 100 | nA |
| | | | | N-Ch 2 | - | - | ± 100 | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$ | N-Ch 1 | - | - | 1 | μA |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = -40\text{ V}$ | N-Ch 2 | - | - | 1 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 50 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 50 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 150 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 150 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | N-Ch 1 | 30 | - | - | A |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | N-Ch 2 | 30 | - | - | |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 7.8\text{ A}$ | N-Ch 1 | - | 0.018 | 0.022 | Ω |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 10.1\text{ A}$ | N-Ch 2 | - | 0.009 | 0.011 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 7.8\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 0.032 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 10.1\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 0.017 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 7.8\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 0.038 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 10.1\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 0.020 | |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 7.1\text{ A}$ | N-Ch 1 | - | 0.022 | 0.026 | |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 9.3\text{ A}$ | N-Ch 2 | - | 0.011 | 0.013 | |
| Forward Transconductance ^b | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 7.8\text{ A}$ | | N-Ch 1 | - | 46 | - | S |
| | | $V_{DS} = 15\text{ V}, I_D = 10.1\text{ A}$ | | N-Ch 2 | - | 73 | - | |
| Dynamic^b | | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | N-Ch 1 | - | 647 | 809 | pF |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | N-Ch 2 | - | 1161 | 1451 | |
| Output Capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | N-Ch 1 | - | 105 | 131 | pF |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | N-Ch 2 | - | 178 | 222 | |
| Reverse Transfer Capacitance | C_{rss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | N-Ch 1 | - | 42 | 53 | pF |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | N-Ch 2 | - | 68 | 85 | |
| Total Gate Charge ^c | Q_g | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 16\text{ A}$ | N-Ch 1 | - | 13.1 | 19.7 | nC |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 6\text{ A}$ | N-Ch 2 | - | 22.5 | 33.8 | |
| Gate-Source Charge ^c | Q_{gs} | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 16\text{ A}$ | N-Ch 1 | - | 2.12 | - | nC |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 6\text{ A}$ | N-Ch 2 | - | 3.35 | - | |
| Gate-Drain Charge ^c | Q_{gd} | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 16\text{ A}$ | N-Ch 1 | - | 1.84 | - | nC |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 6\text{ A}$ | N-Ch 2 | - | 3.14 | - | |
| Gate Resistance | R_g | $f = 1\text{ MHz}$ | | N-Ch 1 | 1.5 | 3.02 | 5 | Ω |
| | | | | N-Ch 2 | 2.05 | 4.11 | 7 | |

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|--------------|---|--------|------|------|------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
| Turn-On Delay Time ^c | $t_{d(on)}$ | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 1 | - | 33 | 50 | ns |
| | | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 2 | - | 40 | 60 | |
| Rise Time ^c | t_r | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 1 | - | 25 | 38 | |
| | | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 2 | - | 31 | 46 | |
| Turn-Off Delay Time ^c | $t_{d(off)}$ | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 1 | - | 29 | 43 | |
| | | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 2 | - | 52 | 78 | |
| Fall Time ^c | t_f | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 1 | - | 12 | 18 | |
| | | $V_{DD} = 20\text{ V}$, $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | N-Ch 2 | - | 16 | 24 | |
| Source-Drain Diode Ratings and Characteristics ^b | | | | | | | |
| Pulsed Current ^a | I_{SM} | | N-Ch 1 | - | - | 60 | A |
| | | | N-Ch 2 | - | - | 180 | |
| Forward Voltage | V_{SD} | $I_S = 5.2\text{ A}$ | N-Ch 1 | - | 0.8 | 1.2 | V |
| | | $I_S = 6.8\text{ A}$ | N-Ch 2 | - | 0.8 | 1.2 | |

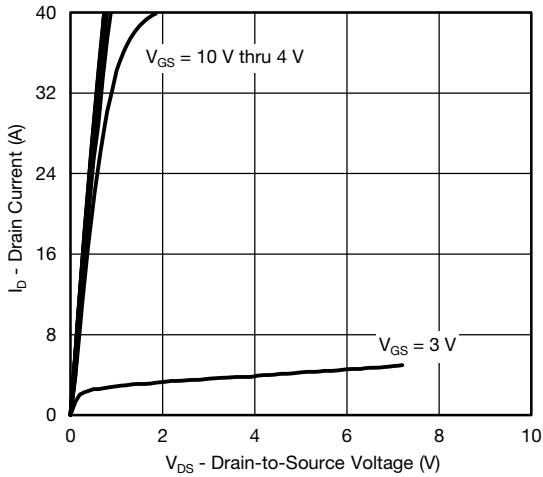
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

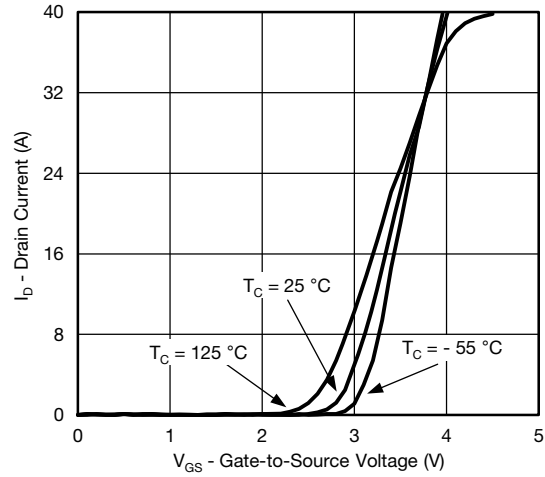
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



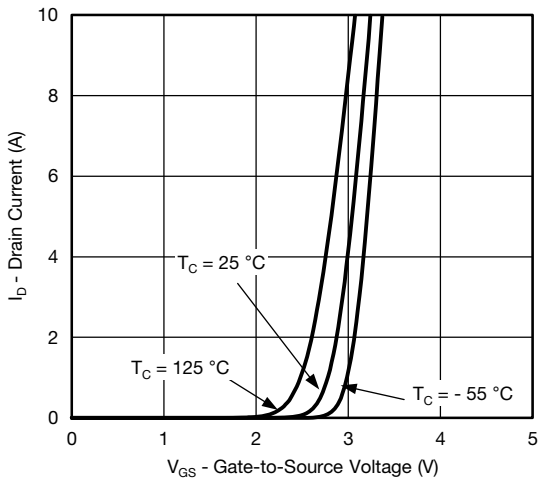
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



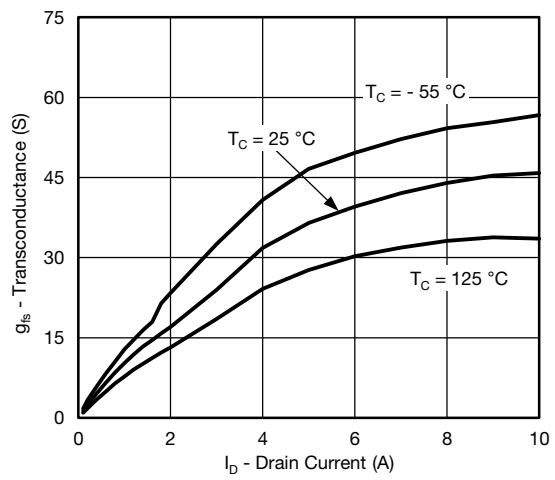
Output Characteristics



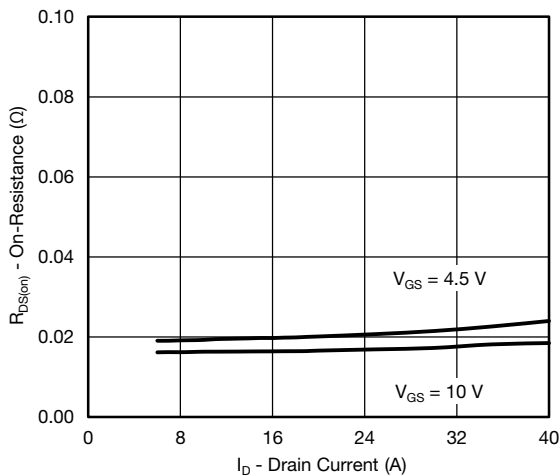
Transfer Characteristics



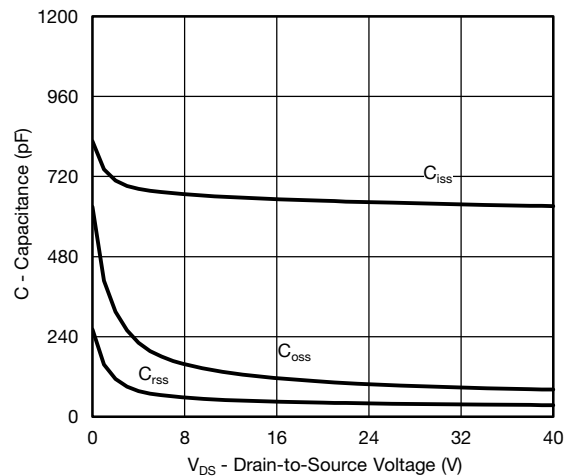
Transfer Characteristics



Transconductance



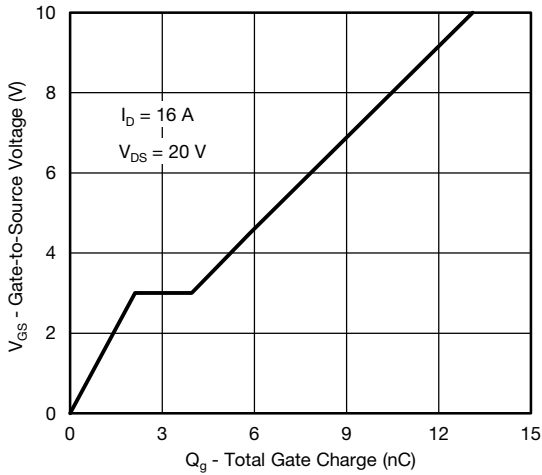
On-Resistance vs. Drain Current



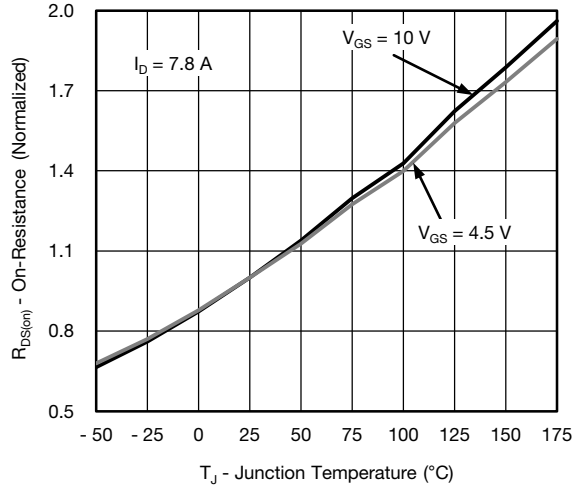
Capacitance



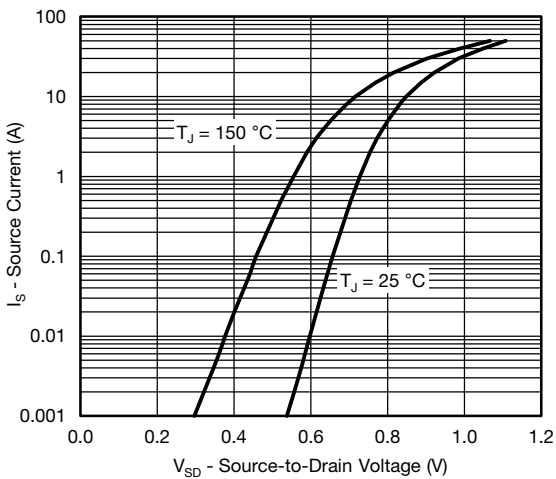
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



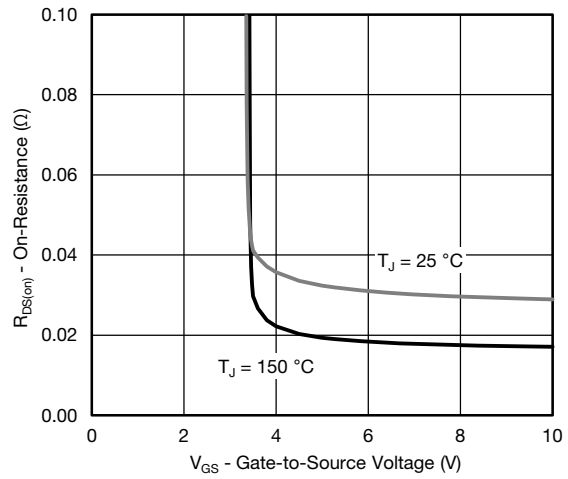
Gate Charge



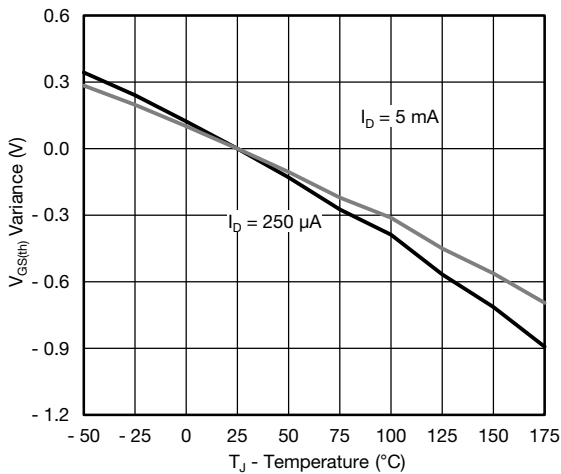
On-Resistance vs. Junction Temperature



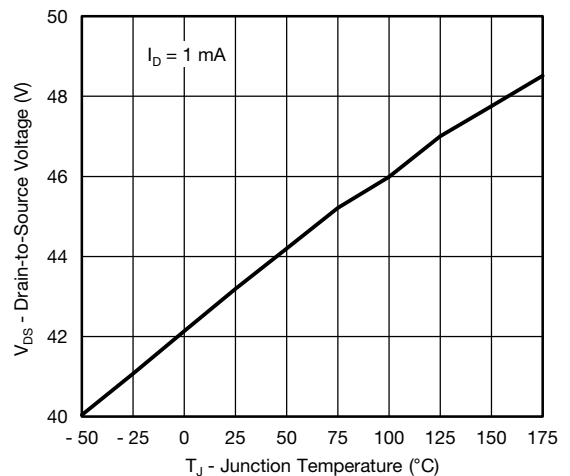
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



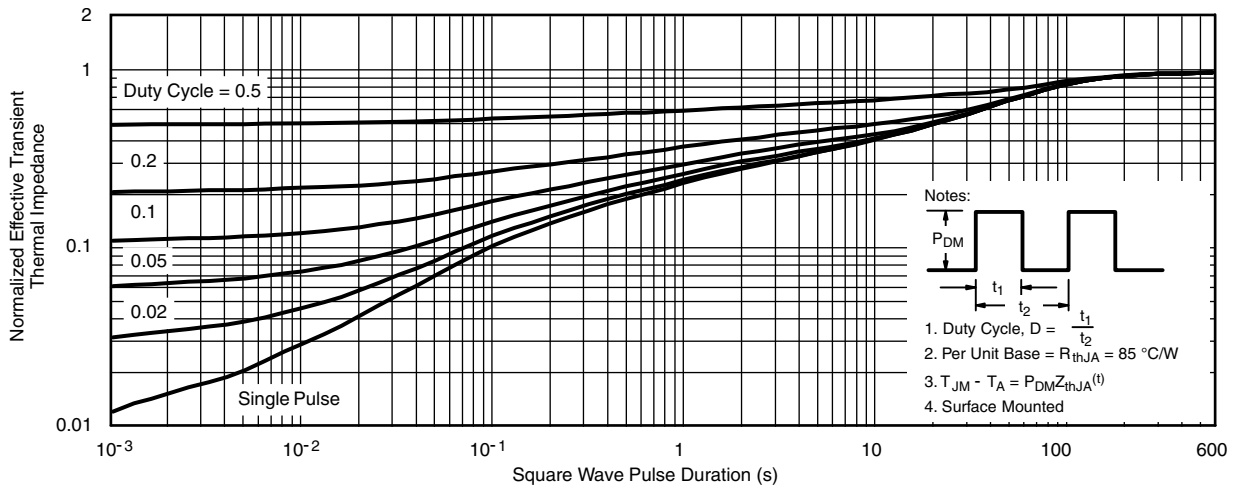
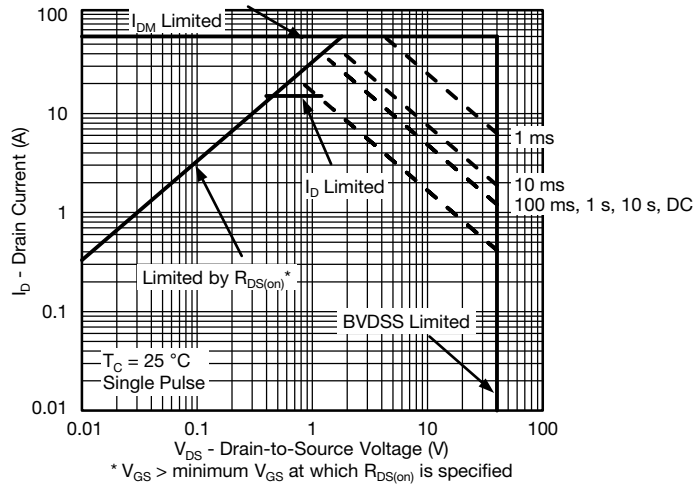
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



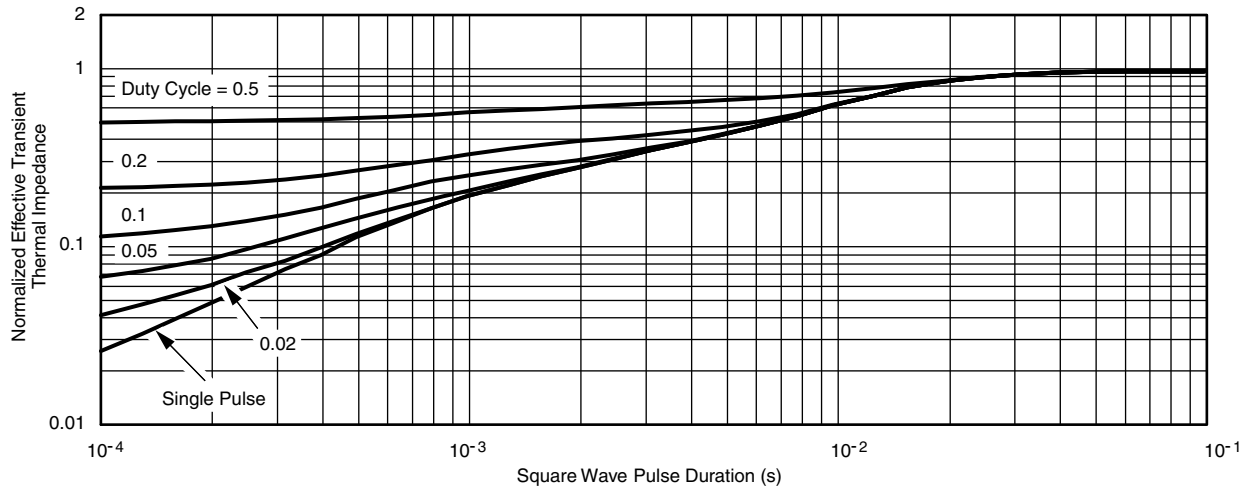
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



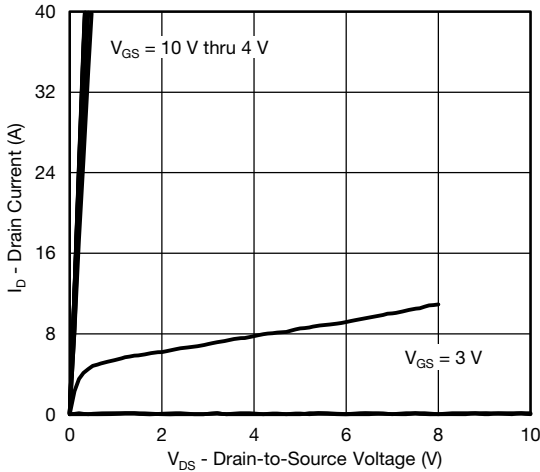
Normalized Thermal Transient Impedance, Junction-to-Case

Note

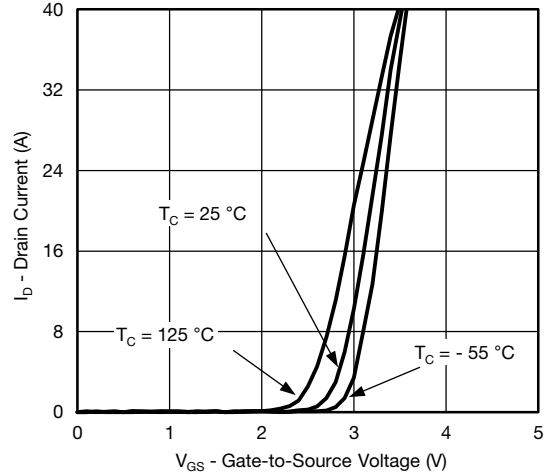
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



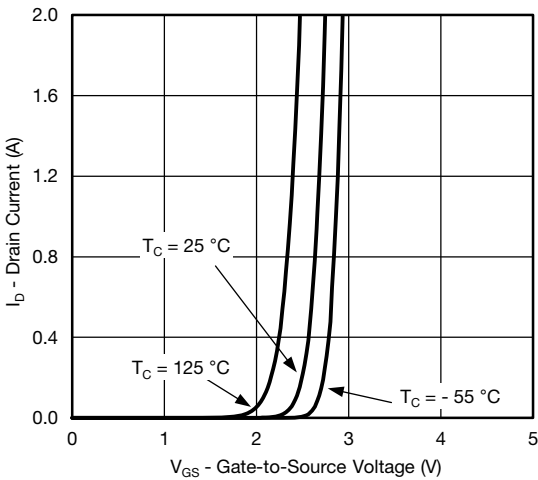
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



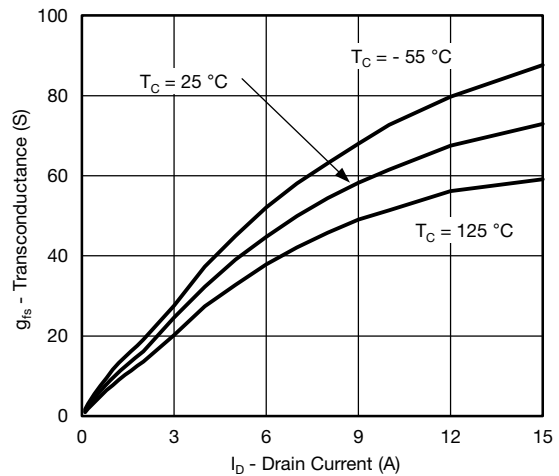
Output Characteristics



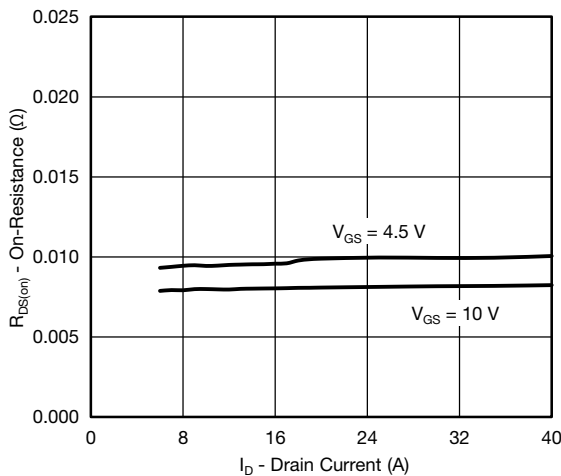
Transfer Characteristics



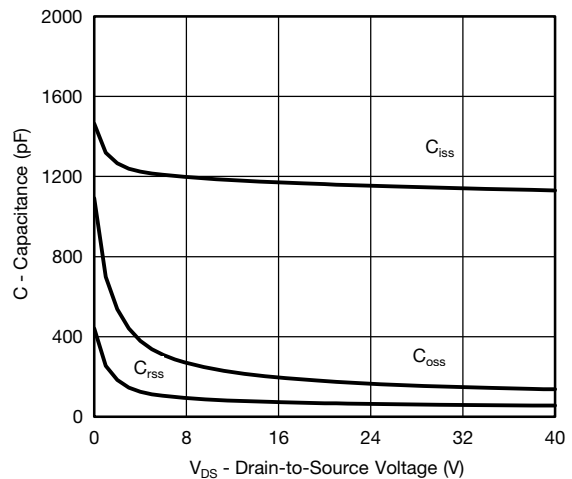
Transfer Characteristics



Transconductance

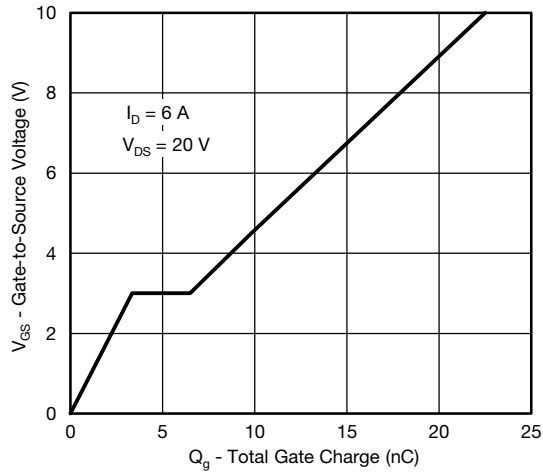


On-Resistance vs. Drain Current

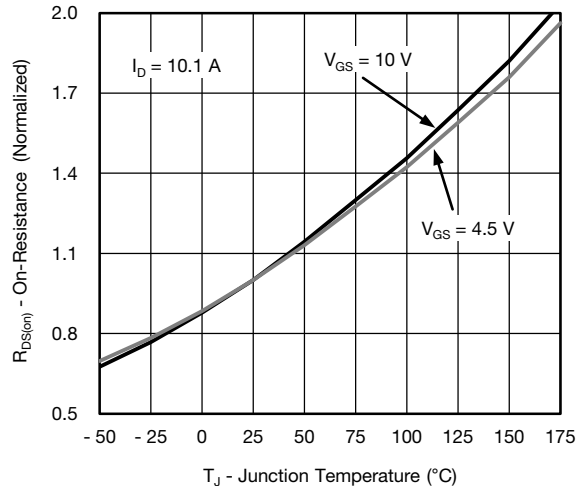


Capacitance

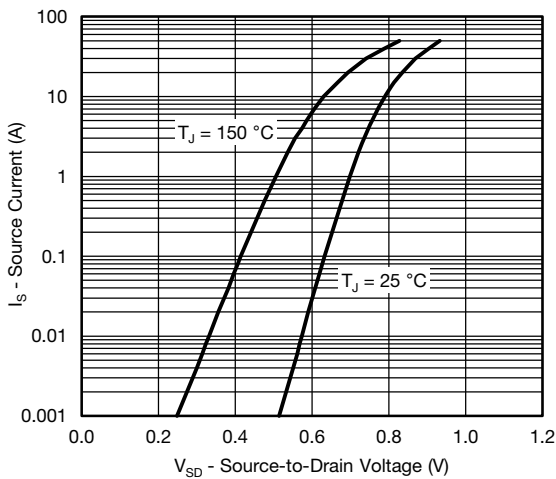
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



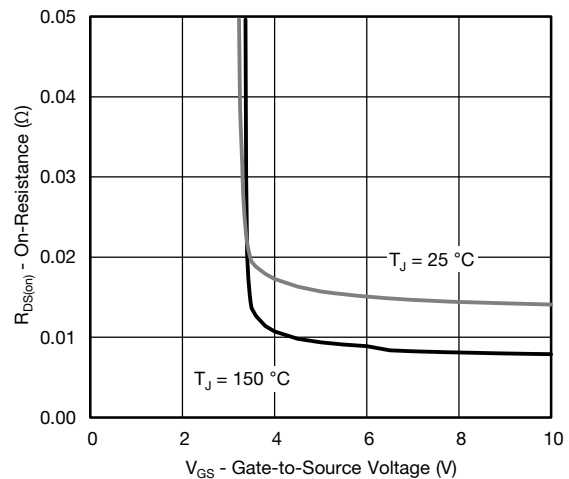
Gate Charge



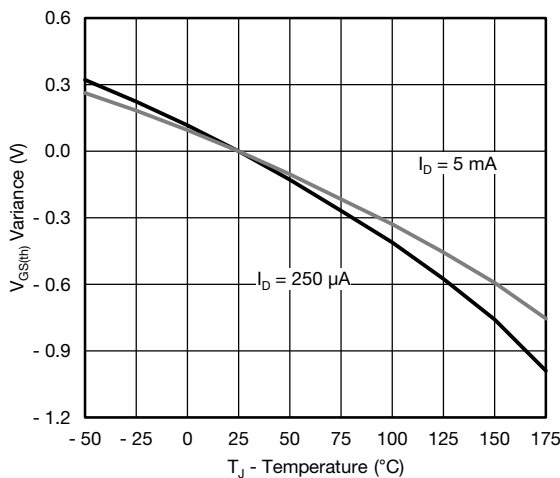
On-Resistance vs. Junction Temperature



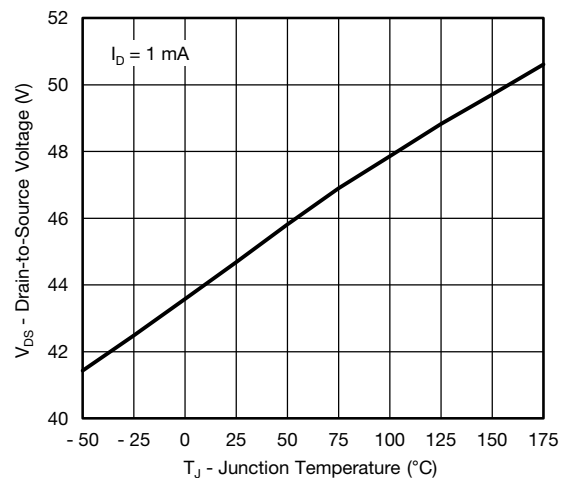
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



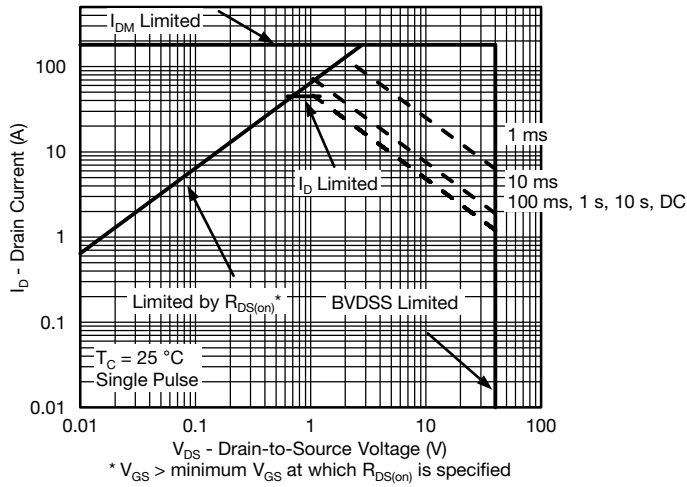
Threshold Voltage



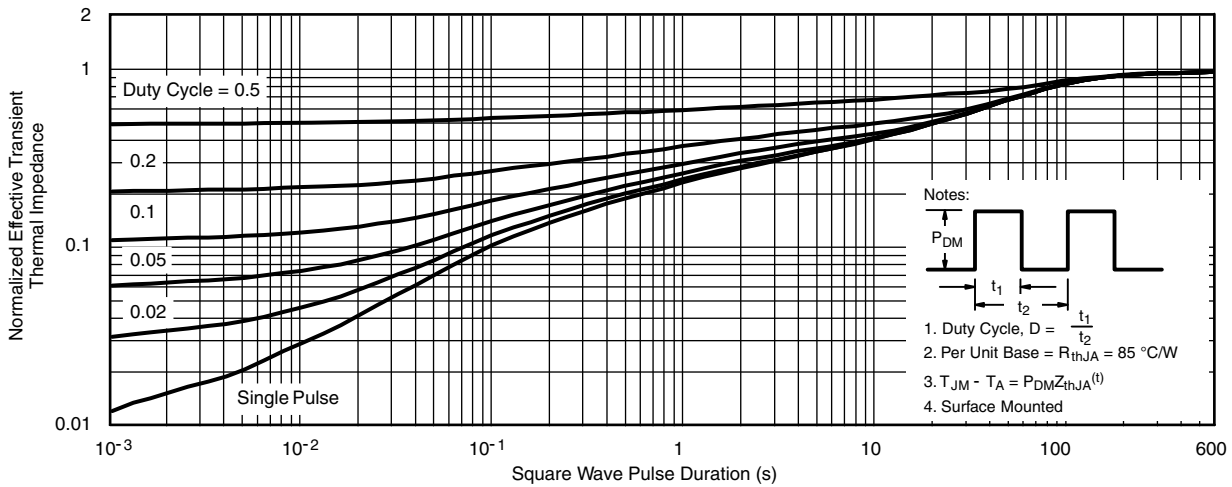
Drain Source Breakdown vs. Junction Temperature



N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



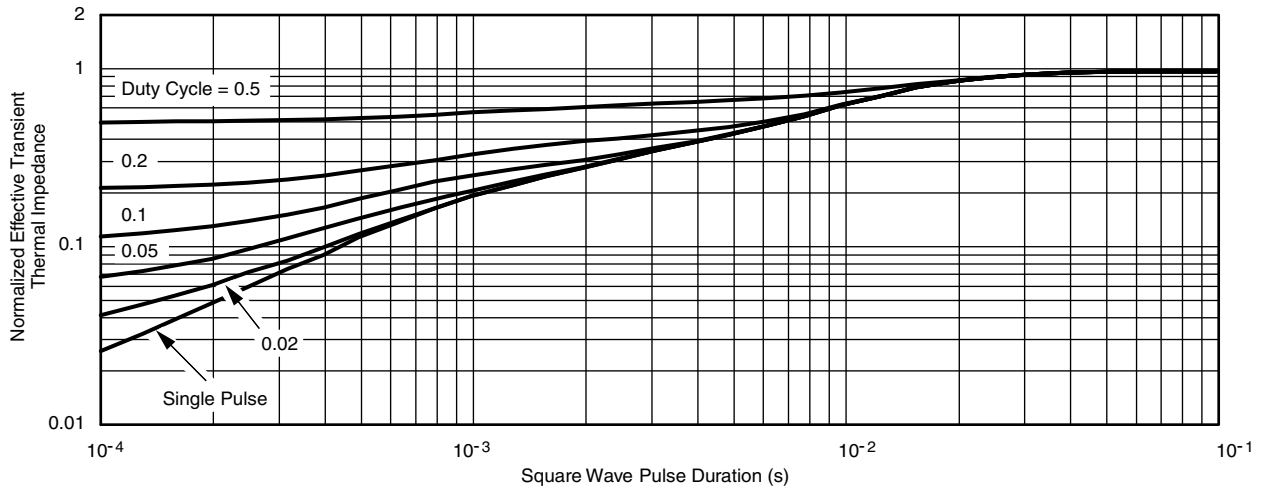
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



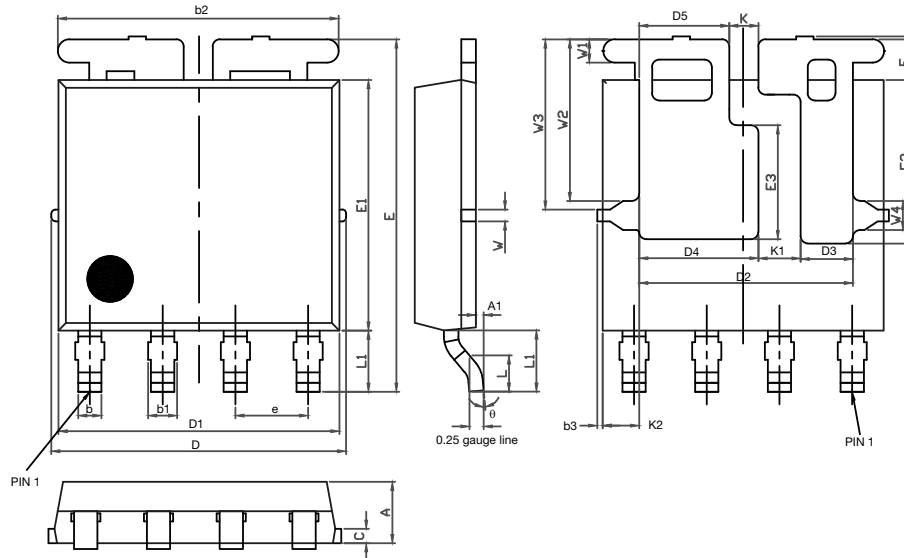
Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62669.

PowerPAK[®] SO-8L Assymmetric Case Outline



| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|------|------|--------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | 1.07 | 1.14 | 0.039 | 0.042 | 0.045 |
| A1 | 0.00 | 0.06 | 0.13 | 0.000 | 0.003 | 0.005 |
| b | 0.33 | 0.41 | 0.48 | 0.013 | 0.016 | 0.019 |
| b1 | 0.44 | 0.51 | 0.58 | 0.017 | 0.020 | 0.023 |
| b2 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| b3 | 0.04 | 0.12 | 0.20 | 0.002 | 0.005 | 0.008 |
| c | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 5.00 | 5.13 | 5.25 | 0.197 | 0.202 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.63 | 3.73 | 3.83 | 0.143 | 0.147 | 0.151 |
| D3 | 0.81 | 0.91 | 1.01 | 0.032 | 0.036 | 0.040 |
| D4 | 1.98 | 2.08 | 2.18 | 0.078 | 0.082 | 0.086 |
| D5 | 1.47 | 1.57 | 1.67 | 0.058 | 0.062 | 0.066 |
| e | 1.20 | 1.27 | 1.34 | 0.047 | 0.050 | 0.053 |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 4.27 | 4.37 | 4.47 | 0.168 | 0.172 | 0.176 |
| E2 | 2.75 | 2.85 | 2.95 | 0.108 | 0.112 | 0.116 |
| E3 | 1.89 | 1.99 | 2.09 | 0.074 | 0.078 | 0.082 |
| F | 0.05 | 0.12 | 0.19 | 0.002 | 0.005 | 0.007 |
| L | 0.62 | 0.72 | 0.82 | 0.024 | 0.028 | 0.032 |
| L1 | 0.92 | 1.07 | 1.22 | 0.036 | 0.042 | 0.048 |
| K | 0.41 | 0.51 | 0.61 | 0.016 | 0.020 | 0.024 |
| K1 | 0.64 | 0.74 | 0.84 | 0.025 | 0.029 | 0.033 |
| K2 | 0.54 | 0.64 | 0.74 | 0.021 | 0.025 | 0.029 |
| W | 0.13 | 0.23 | 0.33 | 0.005 | 0.009 | 0.013 |
| W1 | 0.31 | 0.41 | 0.51 | 0.012 | 0.016 | 0.020 |
| W2 | 2.72 | 2.82 | 2.92 | 0.107 | 0.111 | 0.115 |
| W3 | 2.86 | 2.96 | 3.06 | 0.113 | 0.117 | 0.120 |
| W4 | 0.41 | 0.51 | 0.61 | 0.016 | 0.020 | 0.024 |
| θ | 5° | 10° | 12° | 5° | 10° | 12° |

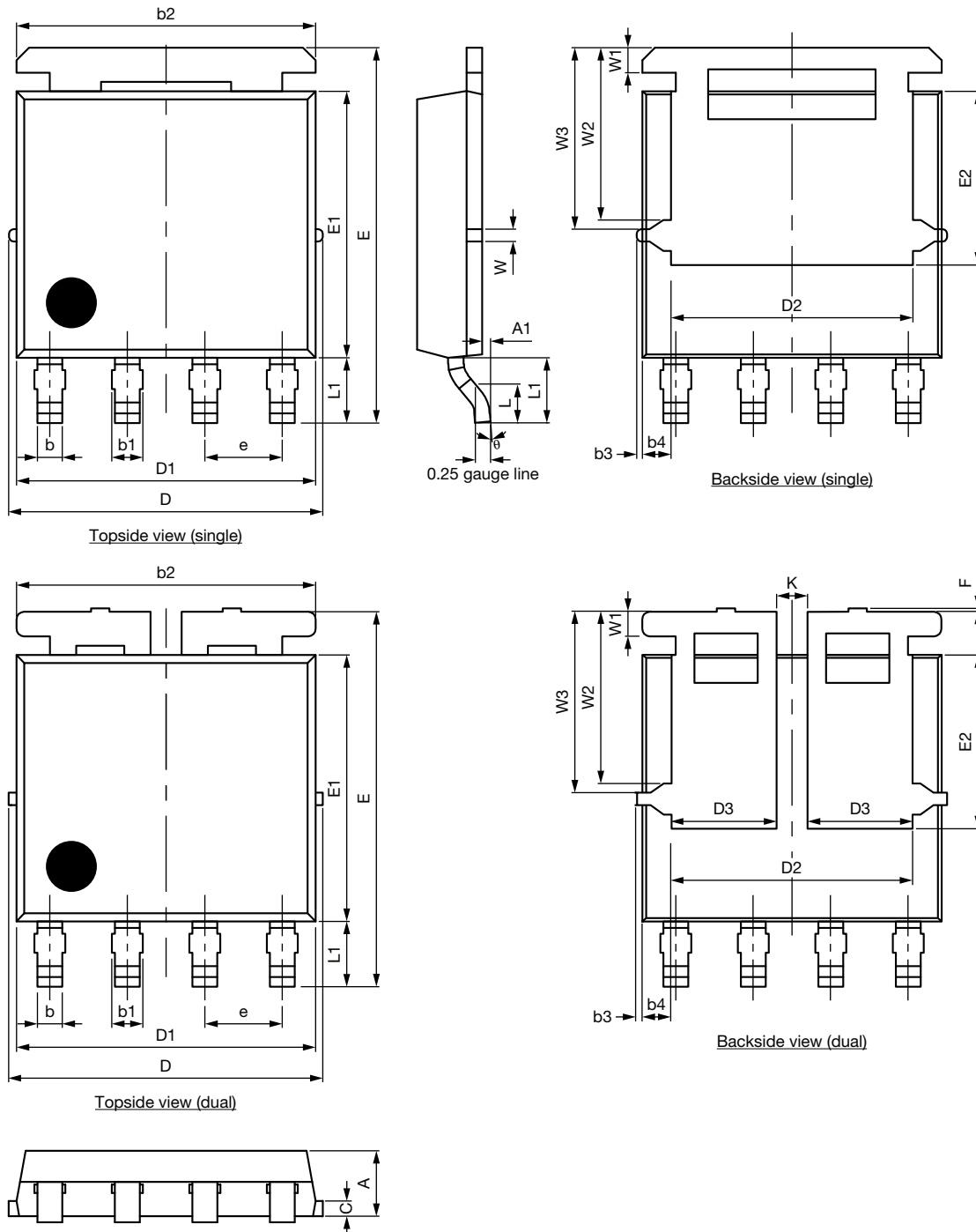
DWG: 6009

Note

- Millimeters will govern



PowerPAK® SO-8L Case Outline 2





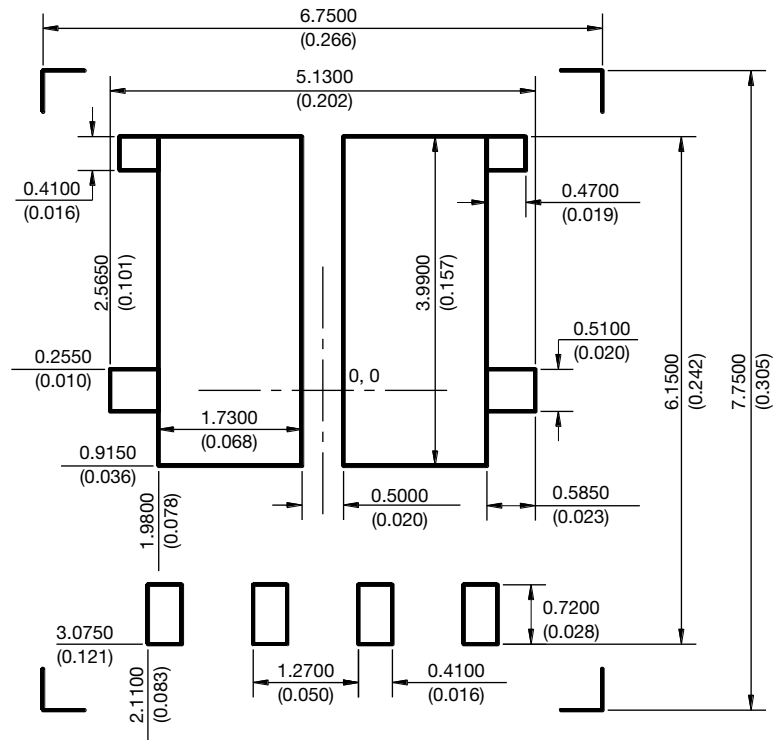
| DIM. | MILLIMETERS | | | INCHES | | |
|-----------------------------------|-------------|------|-------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | 1.07 | 1.14 | 0.039 | 0.042 | 0.045 |
| A1 | 0.00 | - | 0.127 | 0.00 | - | 0.005 |
| b | 0.33 | 0.41 | 0.48 | 0.013 | 0.016 | 0.019 |
| b1 | 0.44 | 0.51 | 0.58 | 0.017 | 0.020 | 0.023 |
| b2 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| b3 | 0.094 | | | 0.004 | | |
| b4 | 0.47 | | | 0.019 | | |
| c | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 5.00 | 5.13 | 5.25 | 0.197 | 0.202 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.86 | 3.96 | 4.06 | 0.152 | 0.156 | 0.160 |
| D3 | 1.63 | 1.73 | 1.83 | 0.064 | 0.068 | 0.072 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 4.27 | 4.37 | 4.47 | 0.168 | 0.172 | 0.176 |
| E2 | 2.75 | 2.85 | 2.95 | 0.108 | 0.112 | 0.116 |
| F | - | - | 0.15 | - | - | 0.006 |
| L | 0.62 | 0.72 | 0.82 | 0.024 | 0.028 | 0.032 |
| L1 | 0.92 | 1.07 | 1.22 | 0.036 | 0.042 | 0.048 |
| K | 0.51 | | | 0.020 | | |
| W | 0.23 | | | 0.009 | | |
| W1 | 0.41 | | | 0.016 | | |
| W2 | 2.82 | | | 0.111 | | |
| W3 | 2.96 | | | 0.117 | | |
| θ | 0° | - | 10° | 0° | - | 10° |
| ECN: C21-1498-Rev. C, 01-Nov-2021 | | | | | | |
| DWG: 6044 | | | | | | |

Note

- Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads
Dimensions in mm (inches)
Keep-out 6.75 (0.266) x 7.75 (0.305)



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