DATASHEET 3A Rated µPOL™ Buck Regulator with Integrated Inductor

Features

- µPOL™ package with output inductor included
- Small size: 3.3mm x 3.3mm x 1.5mm
- Continuous 3A load capability
- Plug and play: no external compensation required
- Input voltage range: 4.5V–5.5V
- Factory trimmed 3.3V ±0.5% initial accuracy
- Supports 3.3V output applications with 5V input
- Enabled input, programmable under-voltage lock-out (UVLO) circuit
- Open-drain power-good indicator
- Built-in protection features
- Operating temperature from -40°C to +125°C
- Lead-free and halogen-free
- Compliant with EU REACH and RoHS

Applications

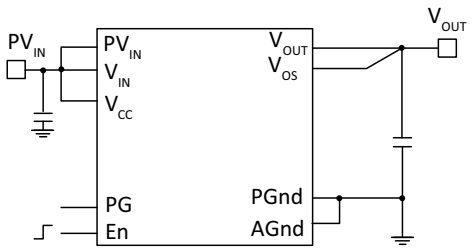
- Storage applications
- Telecom, wireless and 5G applications
- Networking and datacenter applications
- Industrial applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation
- General DC-DC conversion

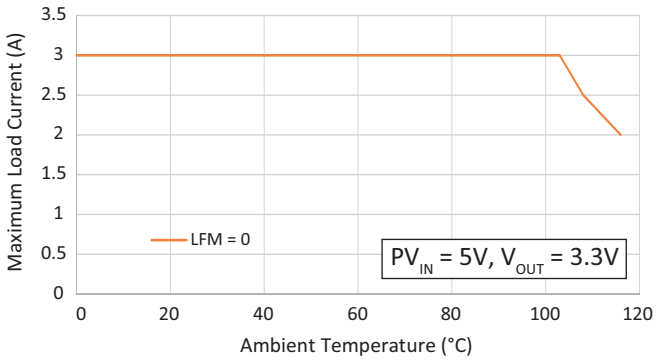
Description

The FS1703 is an easy-to-use, fully integrated and highly efficient micro-point-of-load (µPOL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. Developing and optimizing all of these elements together has yielded the smallest, most efficient and fully featured 3A µPOL™ currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.





Pin configuration

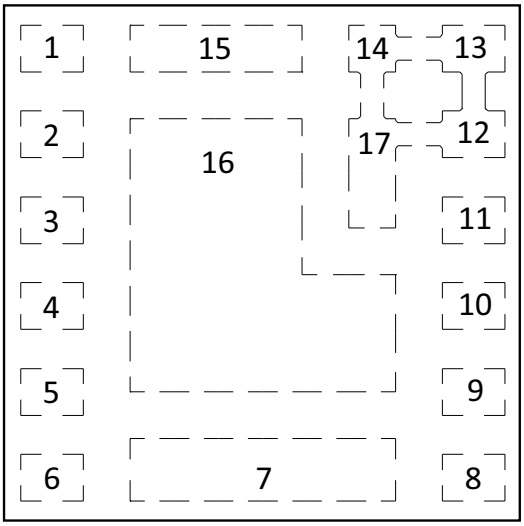


Figure 1 Pin layout (top view)

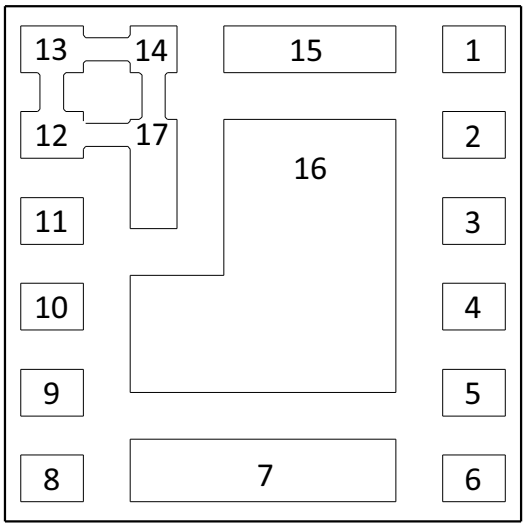


Figure 2 Pin layout (bottom view)

Pin functions

Pin Number	Name	Description
1	NC	**Connect to AGnd.**
2	PG	**Power Good status.** Open drain of an internal MOSFET. Pull up to V_{CC} – pin 10 or an external bias voltage – with a 49.9kΩ resistor.
3	En	**Enable.** Switches the FS1703 on and off. Can be used with two external resistors to set an external UVLO
4	NC	**Connect to AGnd.**
5	V_{OS}	**V_{OUT} sense pin.** Connect to V_{OUT} on the application board using an external resistor divider to set desired output voltage (subject to minimum off time and maximum duty limitations)
6	NC	**Connect to AGnd.**
7	V_{OUT}	**Regulator output voltage.** Place output capacitors between this pin and PGnd (pin 8).
8, 16	PGnd	**Power ground.** Serves as a separate ground for the MOSFETs. Connect to the power ground plane in the application.
9	AGnd	**Signal ground.** Serves as the ground for the internal reference and control circuitry.
10	V_{CC}	**Supply voltage.** May be an input bias for an external V_{CC} voltage. Tie to the V_{IN} pin externally.
11	V_{IN}	**Input voltage.** Tie to PV_{IN} through a 2.7Ω resistor.
12,13,14, 17	PV_{IN}	**Power input voltage.** Input for the MOSFETs.
15	V_{SW}	**Test point for internal V_{SW}.** Connect to an isolated pad on the PCB.

Block diagram

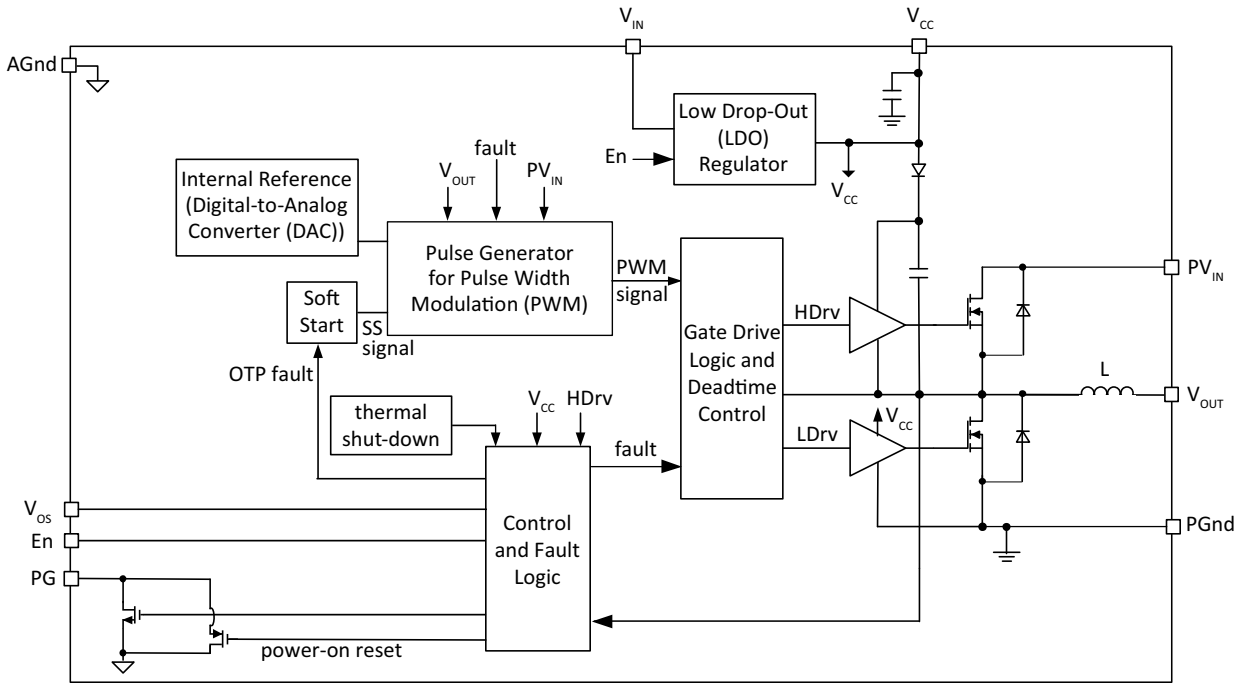


Figure 3 FS1703 µPOL™

Typical applications

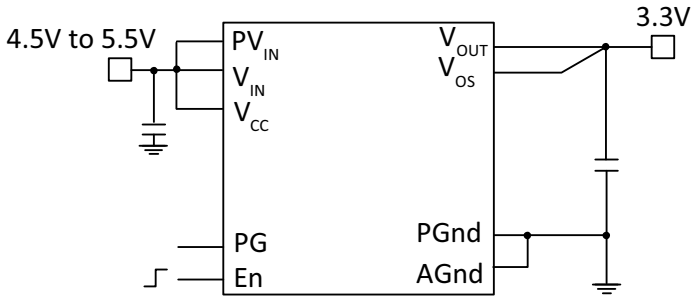


Figure 4 Single supply applications circuit

Absolute maximum ratings

Warning: Stresses beyond those shown may cause permanent damage to the FS1703.

Note: Functional operation of the FS1703 is not implied under these or any other conditions beyond those stated in the FS1703 specification.

Reference	Range
PV_{IN}, V_{IN}, En to PGnd	-0.3V to 18V (Note 1, page 6)
V_{CC} to PGnd	-0.3V to 6V (Note 2, page 6)
V_{OS} to AGnd	-0.3V to V_{CC} (Note 2, page 6)
PG to AGnd	-0.3V to V_{CC} (Note 2, page 6)
PGnd to AGnd	-0.3V to +0.3V
ESD Classification	2kV (HBM JESD22-A114)
Moisture Sensitivity Level	MSL 3 (JEDEC J-STD-020D)

Thermal Information	Range
Junction-to-Ambient Thermal Resistance Θ_{JA}	22.6°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	2.36°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
Note: Θ_{JA} : FS1703 evaluation board and JEDEC specifications JESD 51-2A $\Theta_{J\text{-}c\ (bottom)}$: JEDEC specification JESD 51-8	

Order information

Package details

The FS1703 uses a µPOL™ 3.3 mm x 3.3 mm package delivered in tape-and-reel format, with either 250 or 4000 devices on a reel.

Standard part numbers

	Part numbers	
V_{OUT}	250 devices on a reel	4000 devices on a reel
3.3	FS1703-3300-AS	FS1703-3300-AL

Recommended operating conditions for various output voltages

Output voltage= 3.3V

Definition	Symbol	Min	Max	Units
Input Voltage Range with external V_{CC} (Note 3, Note 5)	PV_{IN}	4.5	5.5	V
Supply Voltage Range (Note 2)	V_{CC}, V_{IN}	4.5	5.5	
Continuous Output Current Range	I_O	0	3	A
Operating Junction Temperature	T_J	-40	125	°C

Electrical characteristics

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 4.5V < PV_{IN} < 5.5V, 4.5V < V_{IN} < 5.5V, 0°C < T < 125°C Typical values are specified at T_A = 25°C						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply Current						
V_{IN} Supply Current (Standby)	$I_{IN\ (STANDBY)}$	Enable low		1		mA
V_{IN} Supply Current (Static)	$I_{IN\ (STATIC)}$	No switching, En = 2V		2		
V_{IN} Supply Current (Dynamic)	$I_{IN\ (DYN)}$	En high, V_{IN} = 5V, V_{OUT} = 3.3V, F_{SW} = 570kHz		6.3	9	
Soft-Start						
Soft-Start Rate	SS_{RATE} (default)	(Note 6)		1		V/ms
Output Voltage						
Accuracy		T_J = 25°C, PV_{IN} = 5V, V_{OUT} = 3.3V (Note 5)		±0.5		%
		-40°C < T_J < 125°C, PV_{IN} = 5V, (Note 5), V_{OUT} = 3.3V	-1.4		+1.4	
On-Time Timer Control						
On Time	T_{ON}	PV_{IN} = 5V, V_{OUT} = 3.3V, F_{SW} = 570kHz		1190		ns
Minimum On-Time	$T_{ON(MIN)}$	(Note 6)		50		
Thermal Shut-Down						
Thermal Shut-Down	TSD (default)			145		°C
Hysteresis				25		
Under-Voltage Lock-Out						
V_{CC} Start Threshold	$V_{CC}\_UVLO_{(START)}$	V_{CC} Rising Trip Level	3.7	4.0	4.2	V
V_{CC} Stop Threshold	$V_{CC}\_UVLO_{(STOP)}$	V_{CC} Falling Trip Level	3.6	3.8	3.95	
Enable Threshold	$En_{(HIGH)}$	Ramping Up	1.1	1.2	1.3	
	$En_{(LOW)}$	Ramping Down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Current Limit						
Current Limit Threshold	I_{OC} (default)	T_J = 25°C	3.6	4	4.3	A

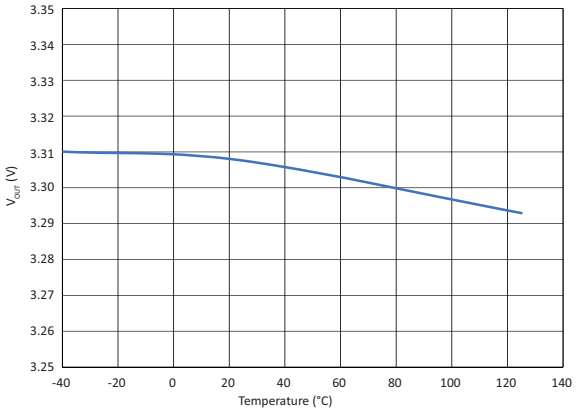
ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: 4.5V < PV_{IN} < 5.5V, 4.5V < V_{IN} < 5.5V, 0°C < T < 125°C Typical values are specified at T_A = 25°C						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Hiccup Blanking Time	$T_{BLK(HICCUP)}$			20		ms
Over-Voltage Protection						
Output Over-Voltage Protection Threshold	V_{OVP} (default)	OVP Detect (Note 6), V_{OUT} = 3.3V	115	120	125	V_{OS}%
Output Over-voltage Protection Delay	T_{OVPDEL}			5		µs
Power Good (PG)						
Power Good Upper Threshold	$V_{PG(UPPER)}$ (default)	V_{OUT} Rising to 3.3V	85	90	95	V_{OS}%
Power Good Hysteresis	$V_{PG(LOWER)}$	V_{OUT} Falling from 3.3V		5		
Power Good Sink Current	I_{PG}	PG = 0.5V, En = 2V		9		mA

Notes

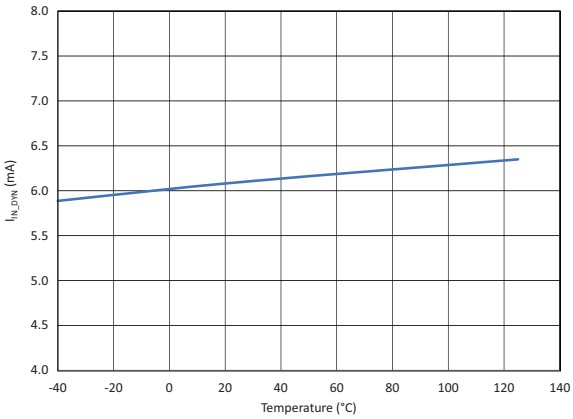
1 PGnd pin and AGnd pin are connected together
2 Must not exceed 6V
3 V_{IN} is connected to V_{CC} to bypass the internal Low Drop-Out (LDO) regulator and also to PV_{IN}
4 Maximum switch node voltage should not exceed 22V
5 Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment
6 Guaranteed by design but not tested in production

Temperature characteristics

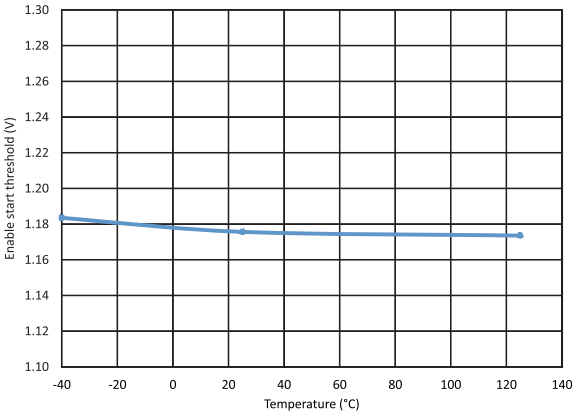
Output Voltage



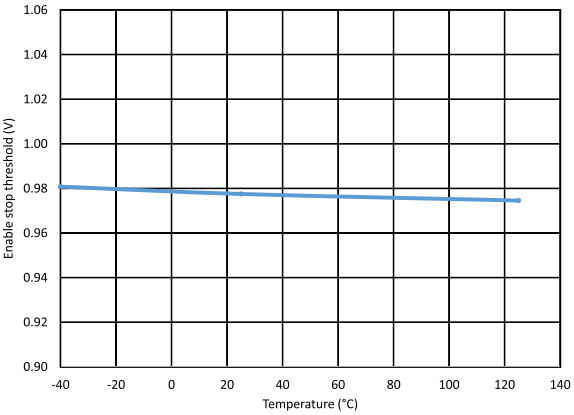
V_{IN} Supply Current (Dynamic)



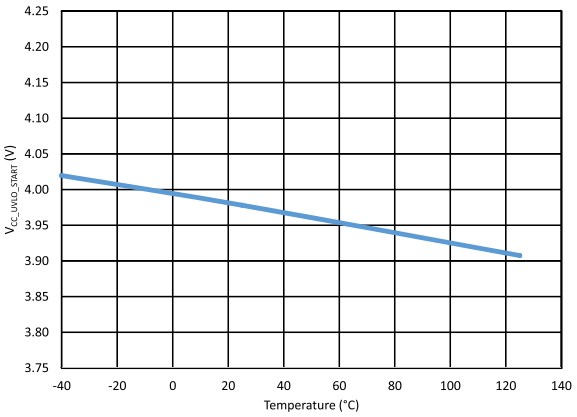
Enable Start Threshold



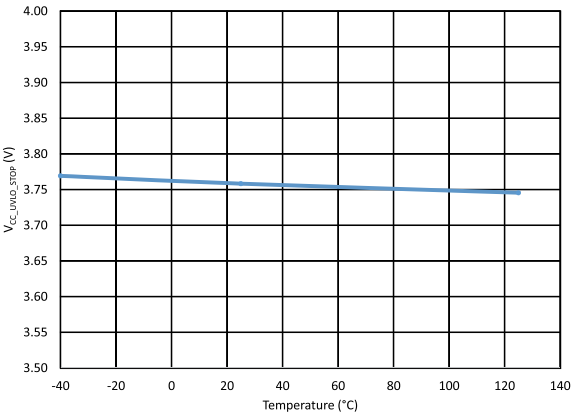
Enable Stop Threshold



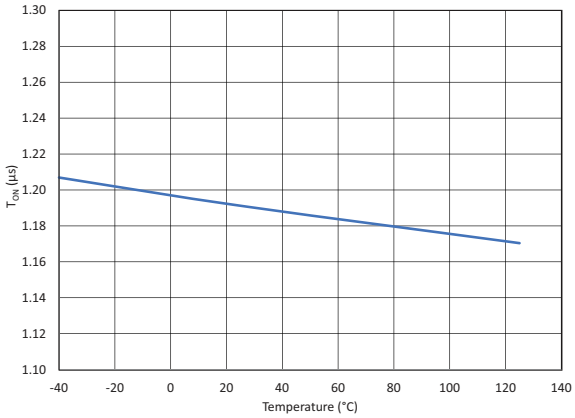
V_{CC} Start Threshold



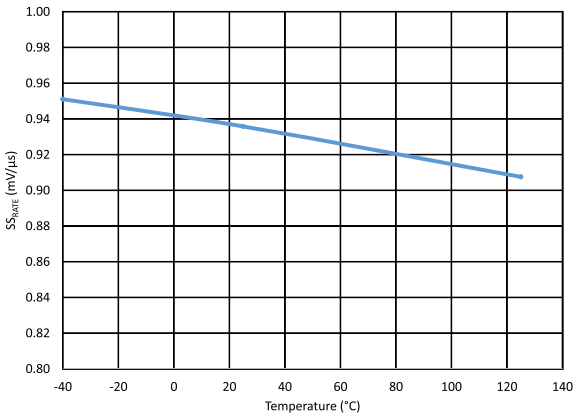
V_{CC} Stop Threshold



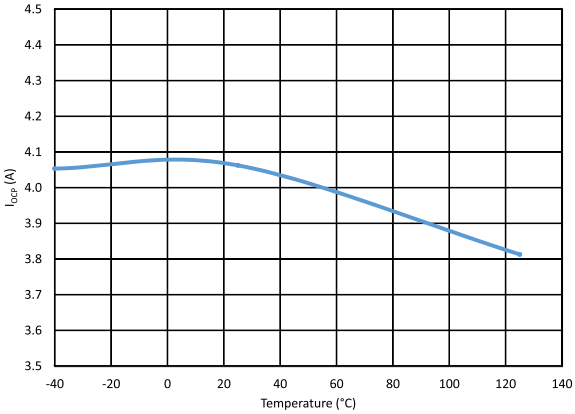
On Time



Soft-Start Rate



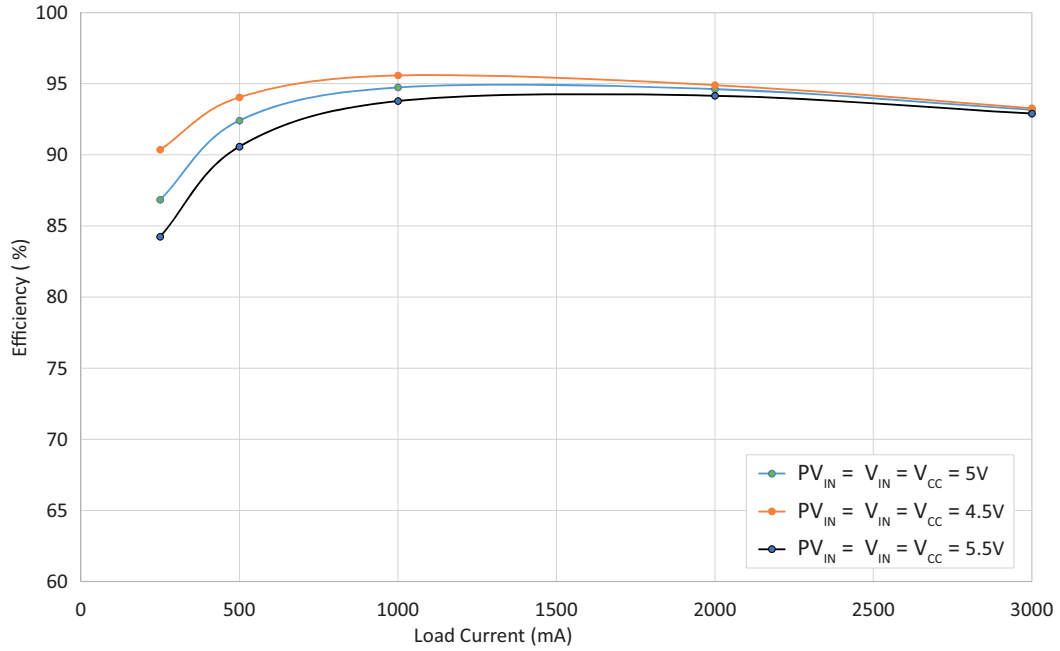
Current Limit Threshold

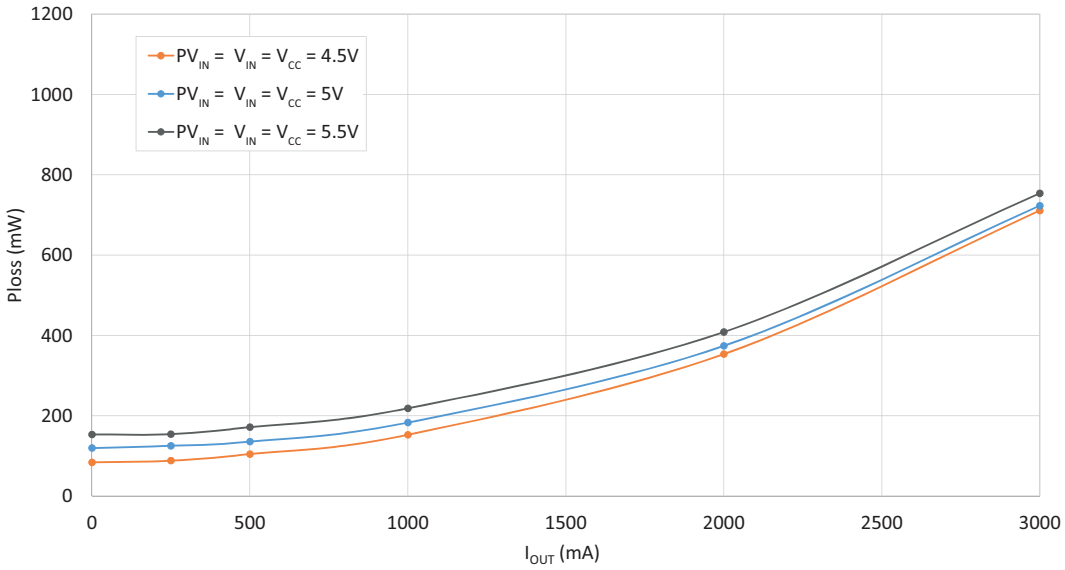


Efficiency characteristics

Typical efficiency and power loss

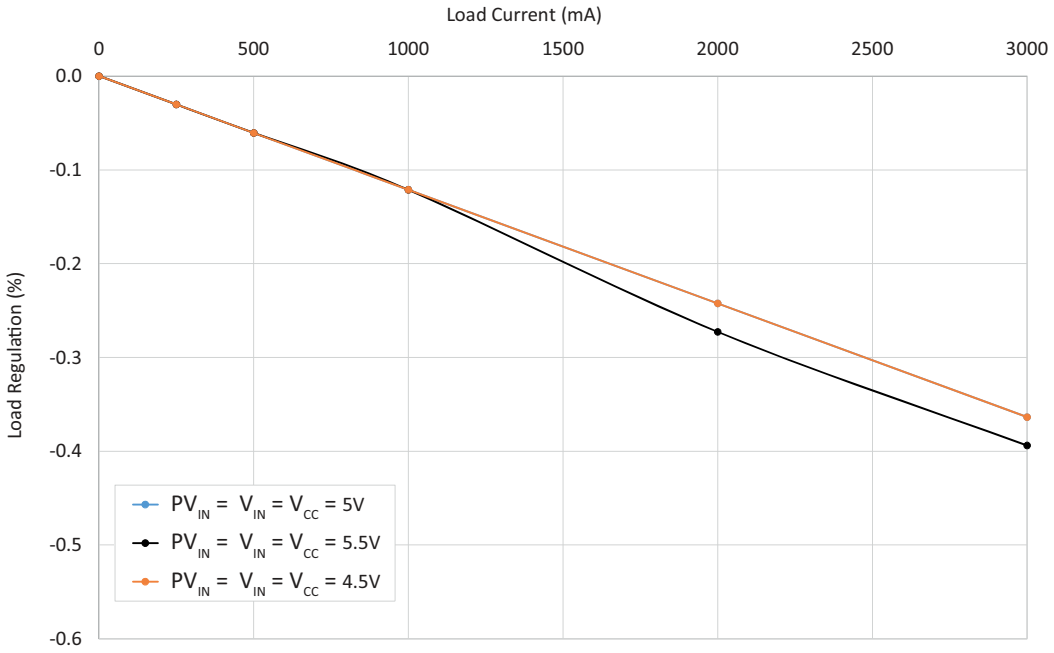
PV_{IN} =4.5V–5.5V, I_O = 0A–3A, room temperature, no air flow, all losses included





Typical load regulation

PV_{IN} = 4.5V–5.5V, I_O = 0A–3A, room temperature, no air flow



Applications information

Overview

The FS1703 is an easy-to-use, fully integrated and highly efficient DC/DC regulator. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues.

Bias voltage

For single-rail operation, the V_{IN} pin of the FS1703 should be connected to the PV_{IN} pin and V_{CC} pin (Figure 5).

Note: **Until initialization is complete, a small leakage current (≈3.4µA) will flow from the device into the output. This may significantly pre-bias the output voltage in applications with long V_{IN}/V_{CC} rise times. To prevent this, a small load capable of sinking 3.4µA should be connected in such applications.**

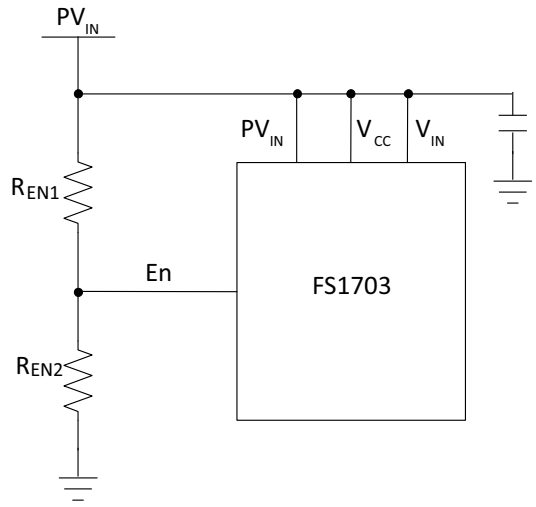


Figure 5 ***Single supply configuration: internal LDO regulator, adjustable PV_{IN}_UVLO***

Soft-start and target output voltage

The FS1703 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When V_{CC} exceeds its start threshold (V_{CC}_UVLO$_{(START)}$), the FS1703 exits reset mode and initialization begins.

Once initialization is complete and the Enable (En) pin has been asserted (Figure 6), the internal reference soft-starts to the target output voltage at 1mV/µs.

During initial start-up, the FS1703 operates with a minimum of high-drive (HDrv) pulses until the output voltage increases (see Switching frequency and minimum values for on-time on page 12). On-time is increased until V_{OUT} reaches the target value.

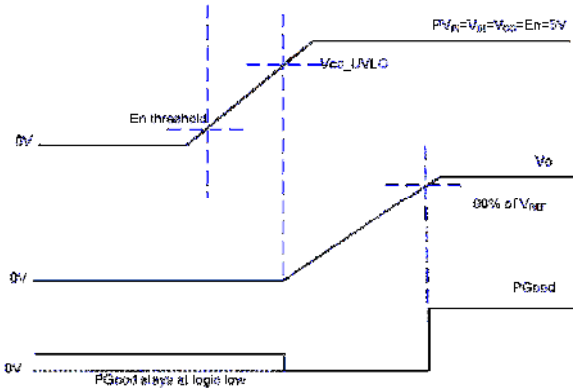


Figure 6 ***Theoretical operational waveforms during soft-start***

Pre-biased start-up

The FS1703 can start up into a pre-charged output smoothly, without causing oscillations and disturbances of the output voltage. When it starts up in this way, the Control and Synchronous MOSFETs are forced off until the internal Soft-Start (SS) signal exceeds the sensed output voltage at the V_{OS} pin. Only then is the first gate signal of the Control MOSFET generated, followed by complementary turn on of the Synchronous MOSFET. The Power Good (PG) function is not active until this point.

Shut-down mechanism

The FS1703 shuts down by de-asserting the En pin. Both drivers switch off and the digital-to-analog converter (DAC) and soft-start are pulled down instantaneously.

Switching frequency and minimum values for on-time

The switching frequency of the FS1703 is set at the factory to 570kHz.

As a result, system designers need not concern themselves with selecting the switching frequency and have one fewer design task to manage.

When input voltage is high relative to target output voltage, the Control MOSFET is switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very small, the FS1703 operates with minimum on-time.

Enable (En) pin

The Enable (En) pin has several functions:

- It is used to switch the FS1703 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal 1MΩ resistor pulls it down to prevent the FS1703 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the PV_{IN} voltage by a set of resistive dividers, R_{EN1} and R_{EN2} (Figure 5). Users can program the UVLO threshold voltage by selecting different ratios. This is a useful feature that stops the FS1703 regulating when PV_{IN} is lower than the desired voltage.
- It can be directly connected to PV_{IN} without external resistive dividers for some space-constrained designs. This is a useful feature for standalone start-up, when no logic signal is available to enable the FS1703.

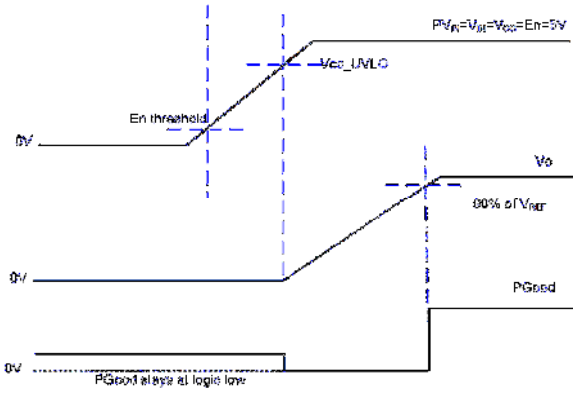


Figure 7 Start-up:
PV_{IN}, V_{IN}, V_{CC} and En pins tied together, PG pin pulled up to an external supply

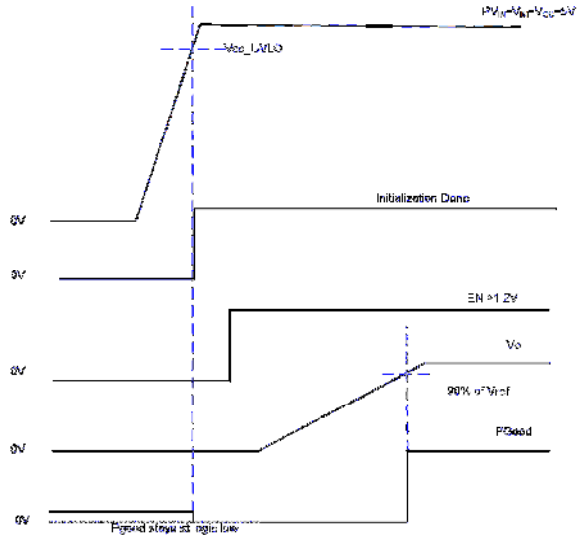


Figure 8 Start-up: En pin asserted after PV_{IN} and V_{IN}, PG pin pulled up to an external supply

For V_{OUT} to start up as defined by the soft-start rate requires correct sequencing:

- PV_{IN} must start up before V_{CC} and/or Enable.
- PV_{IN} must ramp down only after V_{CC} has ramped down below its UVLO threshold and/or Enable has been de-asserted.

Over-current protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the $R_{DS(on)}$ of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

- Provides accurate overcurrent protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is set to 4A.

The threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1703 enters hiccup mode (Figure 9). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1703 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1703 remains in hiccup mode until the over-current fault is remedied.

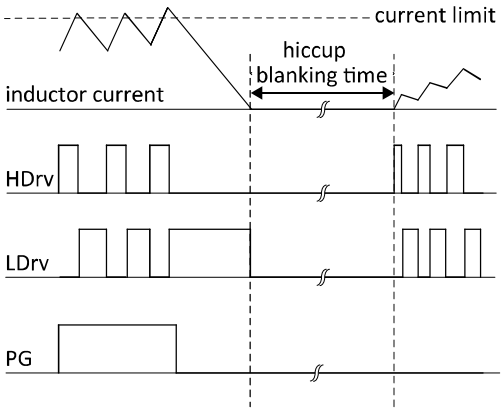


Figure 9 Illustration of OCP in hiccup mode

Over-voltage protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the V_{OS} pin. When V_{OS} exceeds the output OVP threshold for longer than the output OVP delay (typically 5µs), a fault condition is generated.

The OVP threshold is set internally to 120% of V_{OUT}

When an OVP condition is detected, the Control MOSFET is switched off immediately and the PG pin is pulled low. The Synchronous MOSFET is switched on to discharge the output capacitor.

The Control MOSFET remains latched off until reset by cycling either VCC or En. The voltage at the VOS pin falling below the output OVP threshold (with 5% hysteresis) does not switch on the Control

MOSFET but it does switch off the Synchronous MOSFET to prevent build-up of negative current.

Figure 10 shows a timing diagram for over-voltage protection.

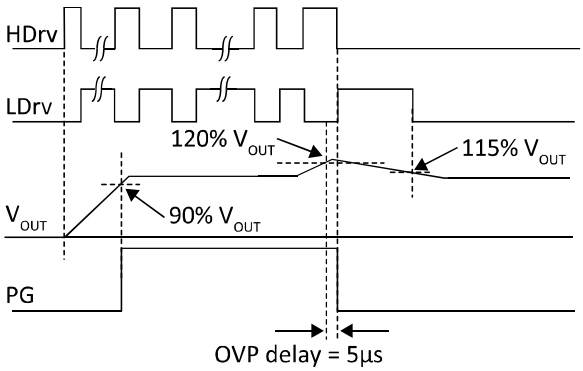


Figure 10 Illustration of latched OVP

Over-temperature protection (OTP)

Temperature sensing is provided inside the FS1703. The OTP threshold is internally set to 145°C.

When the threshold is exceeded, thermal shut-down switches off both MOSFETs and resets the internal soft-start, but the internal LDO regulator is still in operation.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the OTP threshold.

Power Good (PG)

Figure 11 shows PG behavior.

The PG signal is asserted when:

- En and V_{CC} are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- V_{OUT} is within the target range (determined by continuously monitoring whether V_{OS} is above the PG threshold)

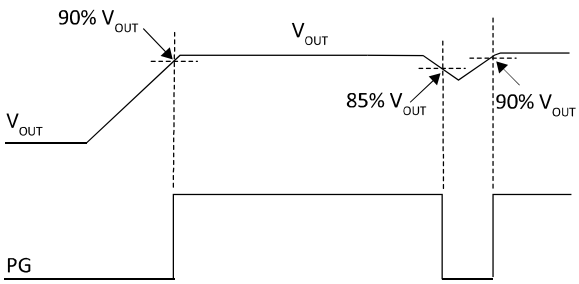


Figure 11 PG signal behavior

As can be seen, when V_{OS} rises above the power good rising threshold (90% of setpoint), the PG signal is pulled high. When V_{OS} drops below the power good falling threshold (85% of setpoint), the PG signal is pulled low.

For pre-biased start-up, the PG signal is not active until the first gate signal of the Control MOSFET is generated.

FS1703 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if V_{CC} is low and the PG pin is pulled up to an external voltage not V_{CC} (Figure 7 and Figure 8).

Design example

Let us now consider a simple design example, using the FS1703 for the following design parameters:

- $PV_{IN} = V_{IN} = 5V$
- $V_{OUT} = 3.3V$
- $F_{SW} = 570kHz$
- $C_{OUT} = 3 \times 22\mu F$
- $C_{IN} = 2 \times 22\mu F$
- Ripple Voltage = ± 1% * V_{OUT}
- $\Delta V_{OUT(MAX)}$ = ±3% * V_{OUT} (for 100% load transient)

Input capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1703
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For a buck converter operating at duty cycle D and output current I_O, the RMS value of the input current is:

$$I_{RMS} = Io\sqrt{D(1-D)}$$

In this application, I_O = 3A and $D = \frac{V_{OUT}}{PV_{IN}} = 0.667$

Therefore, I_{RMS} = 1.4A and we can select two 22µF 16V ceramic capacitors for the input capacitors (C3216X5R1C226M160AB from TDK).

If the FS1703 is not located close to the 12V power supply, a bulk capacitor (68–330µF) may be used in addition to the ceramic capacitors.

For V_{IN}, it is recommended to use a 1µF capacitor very close to the pin. The V_{IN} pin should be connected to PV_{IN} through a 2.7Ω resistor. Together, the 2.7Ω resistor and 1µF capacitor filter noise on PV_{IN}. The V_{IN} pin should be shorted to the V_{CC} pin, bypassing the internal LDO.

Output voltage and output capacitor

The FS1703 is supplied pre-programmed and factory-trimmed in a closed loop to the target voltage specified for the part number. As a result, no external resistor divider is required and resistor tolerances are eliminated from the error budget.

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions.

For the FS1703, the minimum number of output capacitors required to achieve target peak-to-peak V_{OUT} ripple is:

$$N_{MIN} = 5.78 \times \frac{\frac{(1-D)}{8CF_{SW}} + ESR(1-D) + \frac{ESL \times F_{SW} \times (1-D)^2}{D}}{\Delta V_{OUTripple(p-p)}}$$

where:

- N_{MIN} = minimum number of output capacitors
- D = duty cycle
- C = equivalent capacitance of each output capacitor
- F_{SW} = switching frequency
- ESR = equivalent series resistance of each output capacitor
- ESL = equivalent series inductance of each output capacitor
- $\Delta V_{OUTripple(p-p)}$ = target peak-to-peak V_{OUT} ripple

This design uses C2012X5R0J226K125AB from TDK; this is a 22µF MLCC, 0805 case size, rated at 6.3V. At 3.3V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 7µF (C). Equivalent series resistance is 3mΩ (ESR) and equivalent series inductance is 0.44nH (ESL).

Putting these parameters into the equation gives:

N_{MIN} = 1.02

To meet the maximum voltage deviation ΔVo_{max} under a ΔI_o load transient, the minimum required number of output capacitors is:

$$\frac{\mathbf{500 \times 10^{-9} \times \Delta I_o^2}}{\Delta V_{OUTmax} \times V_{OUT} \times C}$$

where:

- ΔI_o = load step
- ΔV_{OUTmax} = target maximum voltage deviation
- V_{OUT} = output voltage
- C = equivalent capacitance of each output capacitor

Again, using C = 7µF, it can be seen that the minimum number of output capacitors required is 1.96.

In our design intended for space-constrained applications, therefore, we use three C2012X5R0J226K125AB capacitors.

It should be noted here that the calculation for the minimum number of output capacitors under a load transient makes some assumptions:

a) No ESR or ESL

b) Converter can saturate its duty cycle instantly

c) No latency

d) Step load (infinite slew rate)

Assumptions (a), (b) and (c) are liberal, whereas (d) is conservative. Therefore, in a real application, additional capacitance may be required to meet transient requirements and should be carefully considered by the system designer.

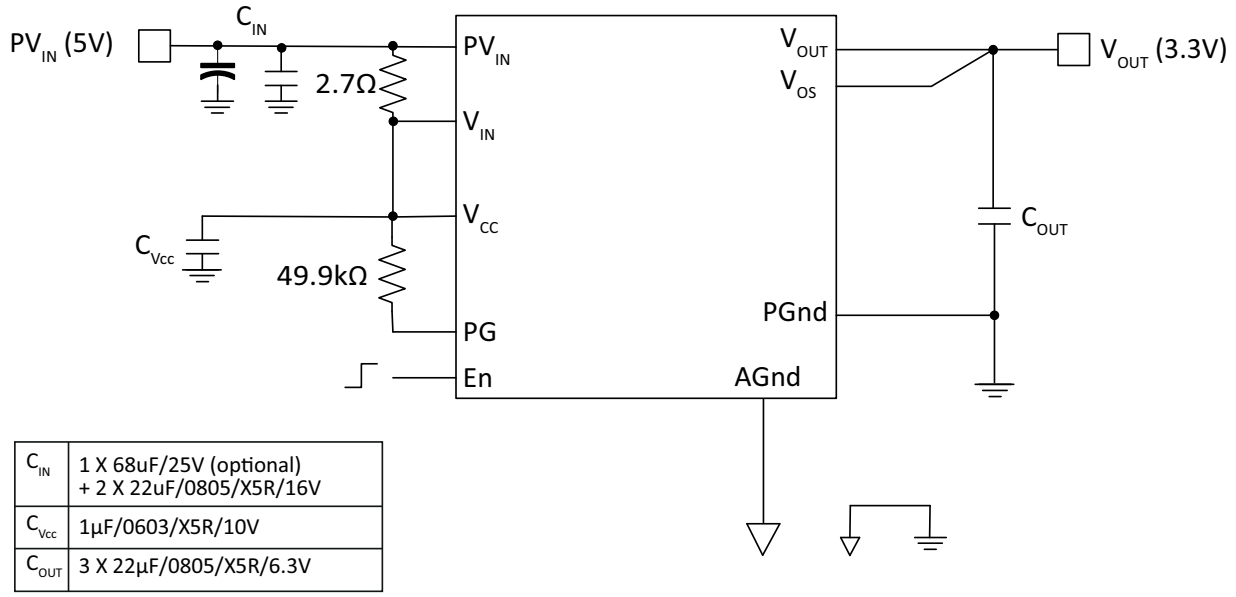
The typical application waveforms in Figure 19 and Figure 20 show the steady state V_{OUT} ripple as well as the voltage deviation in response to a 50% load transient.

It should be noted that even in the absence of a target V_{OUT} ripple or target maximum voltage deviation under load transient, at least one 22µF capacitor is still required in order to ensure stable operation without excessive jitter.

Up to six 22µF capacitors may be used in the design. If more capacitance is required, it is recommended to use a capacitor with relatively high ESR (>3mΩ) such as POSCAP or specialty polymer capacitors.

V_{CC} capacitor selection

FS1703 uses an on-package V_{CC} capacitor to ensure effective high-frequency bypassing. The 1µF capacitor on the V_{IN} pin provides additional bypassing when the LDO is bypassed by shorting the V_{IN} pin to the V_{CC} pin.



C_{IN}	1 X 68uF/25V (optional) + 2 X 22uF/0805/X5R/16V
C_{Vcc}	1µF/0603/X5R/10V
C_{OUT}	3 X 22µF/0805/X5R/6.3V

Figure 12 Application circuit for a single supply, PV_{IN}=5V, V_{OUT}=3.3V, 3A

Typical operating waveforms

PV_{IN}=5V, V_{OUT}=3.3V, I_O=0–3A, room temperature, no airflow

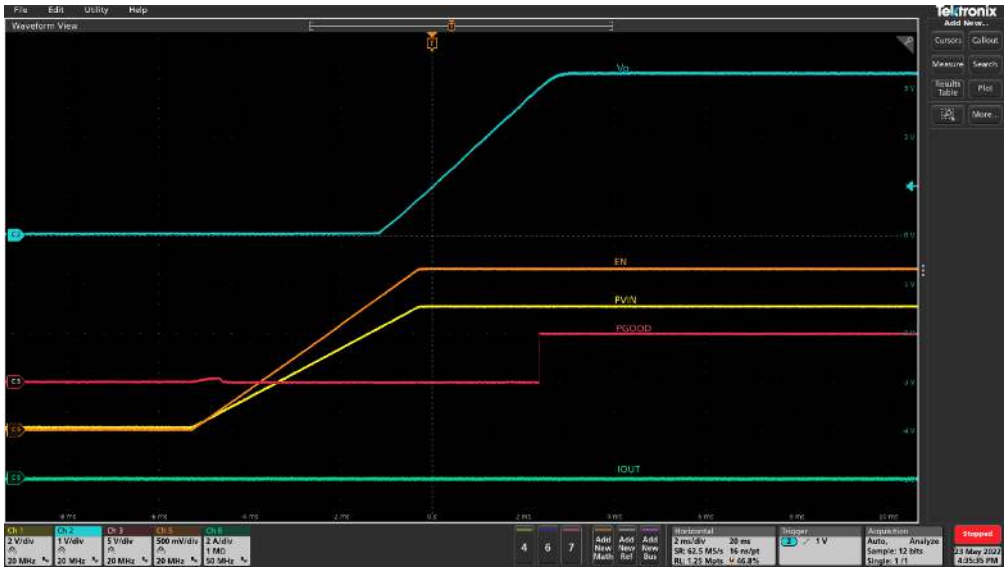


Figure 13 Startup with no load (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch5: Enable, Ch8:I_{OUT})

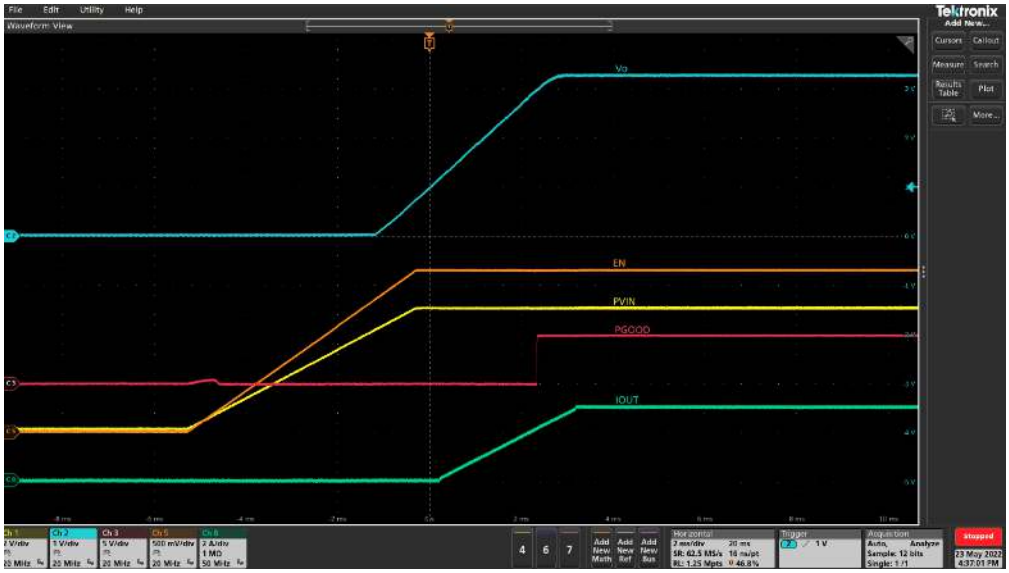


Figure 14 Startup with 3A load (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch5: Enable, Ch8: I_{OUT})

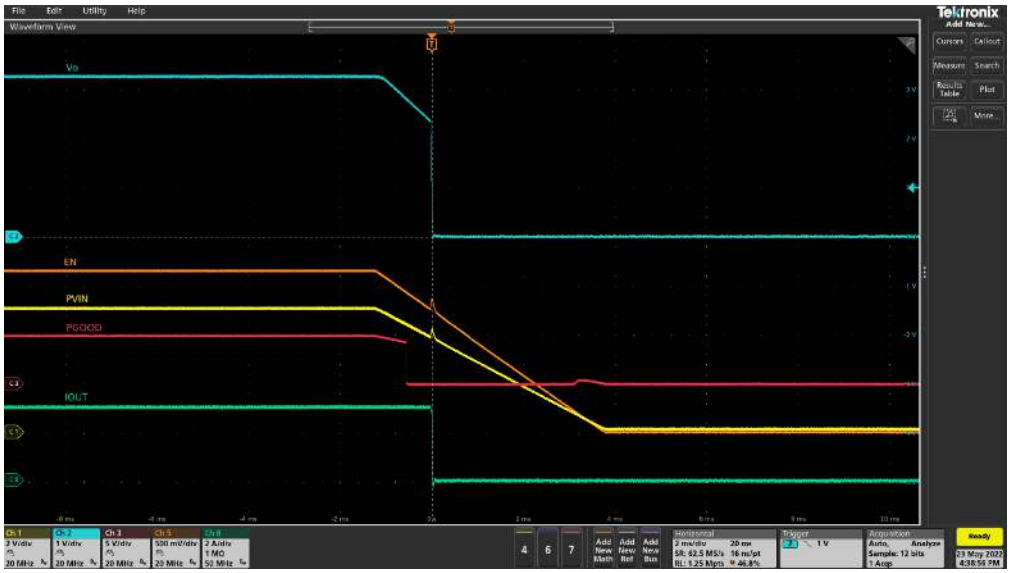


Figure 15 Shutdown with VCC UVLO at 3A load (Ch1: PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch5: Enable, Ch8: I_{OUT})

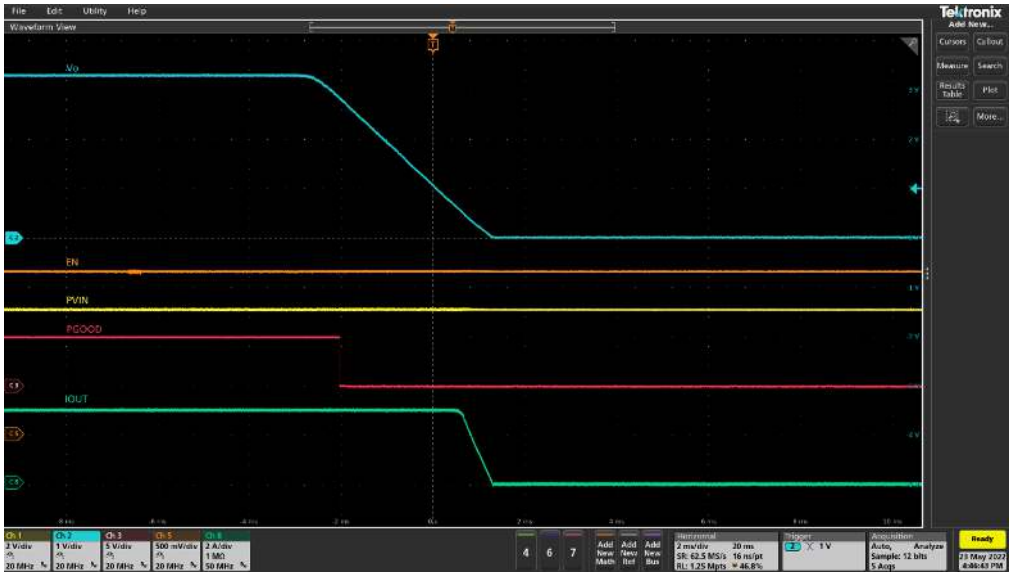


Figure 16 Soft turn off at 3A load (Ch1:PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch5: Enable, Ch8: I_{OUT})

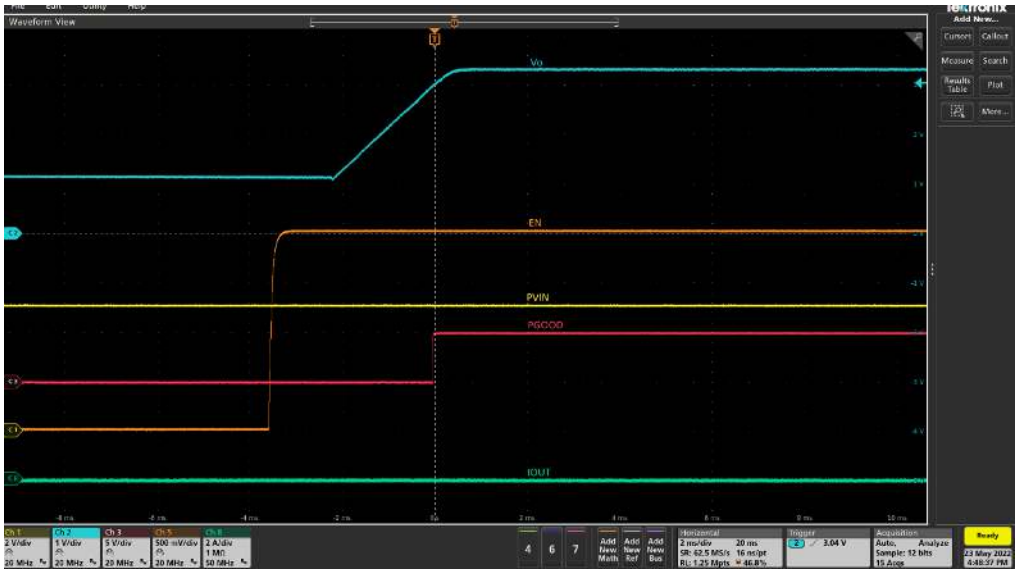


Figure 17 Startup into pre-bias (Ch1: PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch5: Enable, Ch8: I_{OUT})

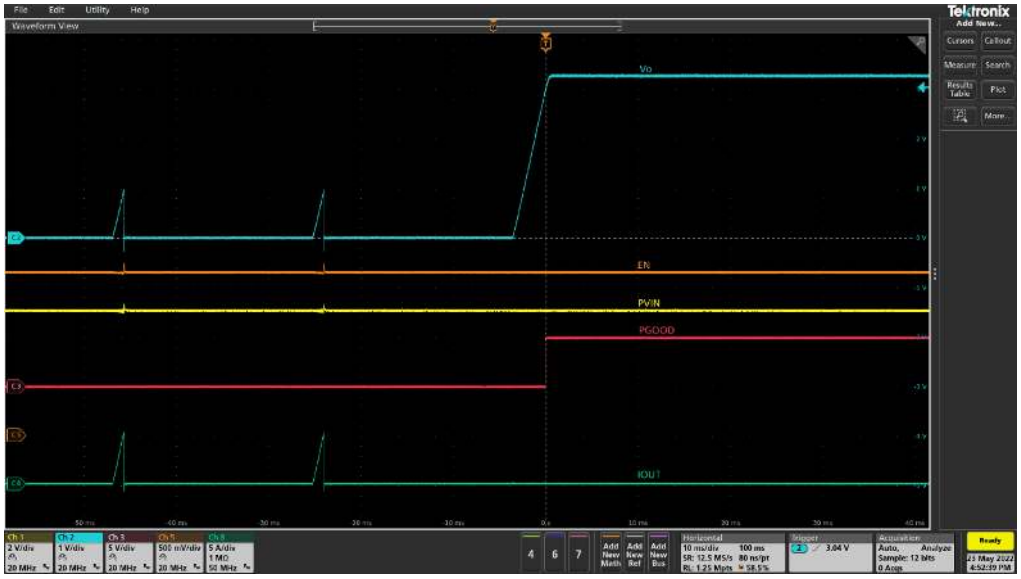


Figure 18 Over-current protection and auto-recover to 3A
(Ch1: PV_{IN}, Ch2: V_{OUT}, Ch3: PG, Ch5: Enable, Ch8: I_{OUT})

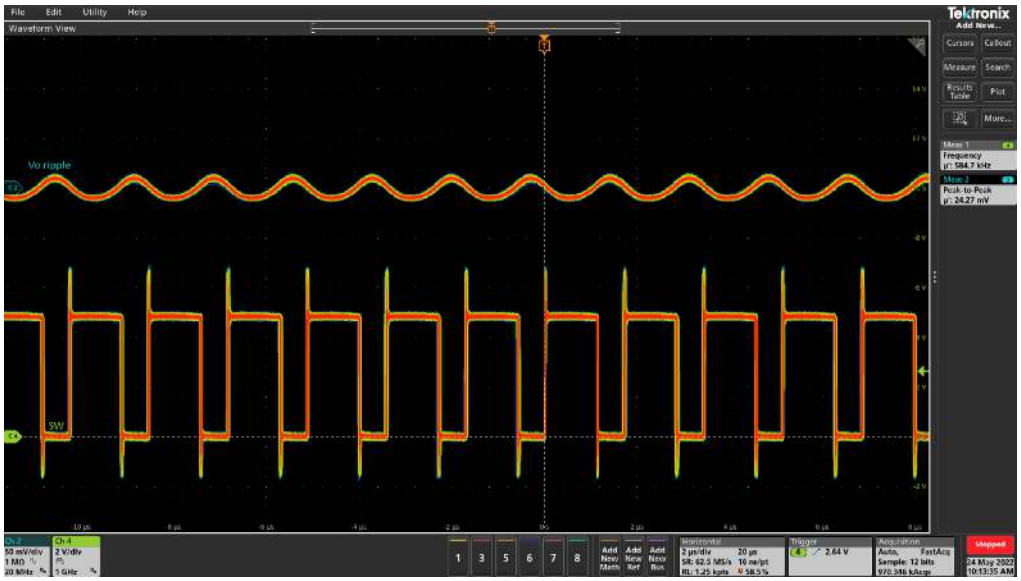


Figure 19 Sw and V_{OUT} ripple at 0A (Ch2: V_{OUT} Ripple, Ch4: Sw)

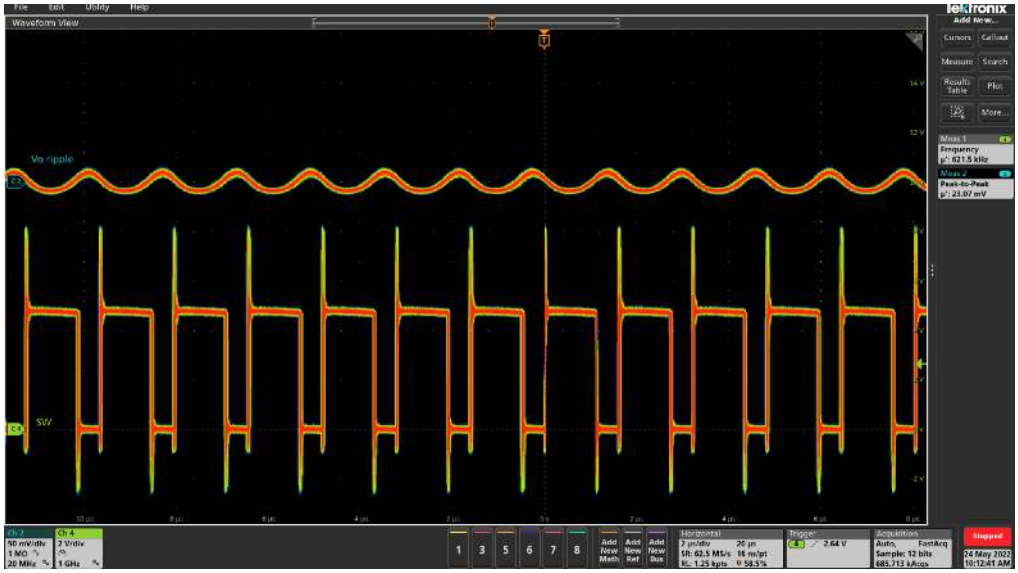


Figure 20 Sw and V_{OUT} ripple at 3A (Ch2: V_{OUT} Ripple, Ch4: Sw)

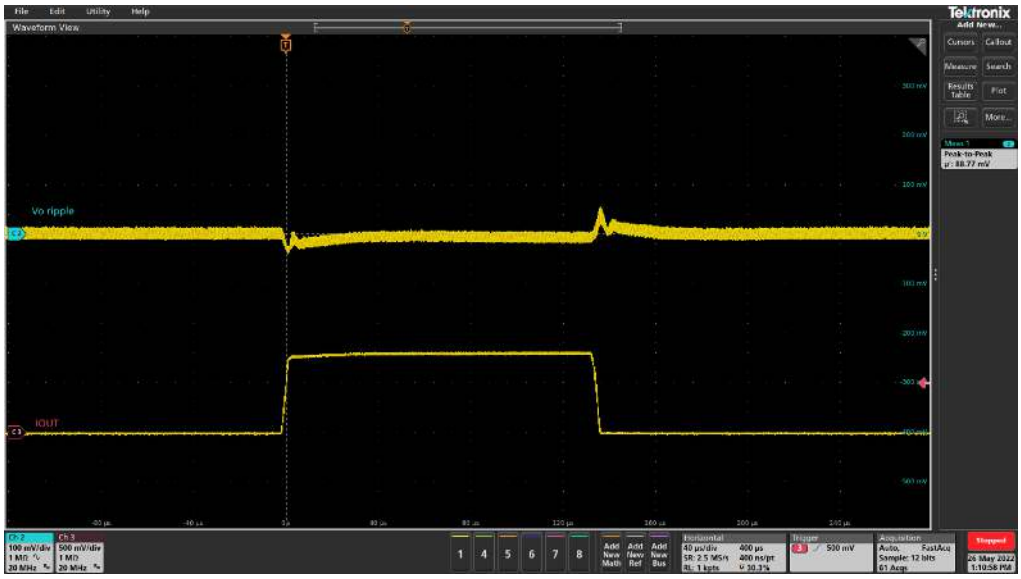


Figure 21 Transient response 0A to 1.5A (Ch2: V_{OUT} rIpple, Ch3: I_{OUT}), peak-peak deviation = 89mV

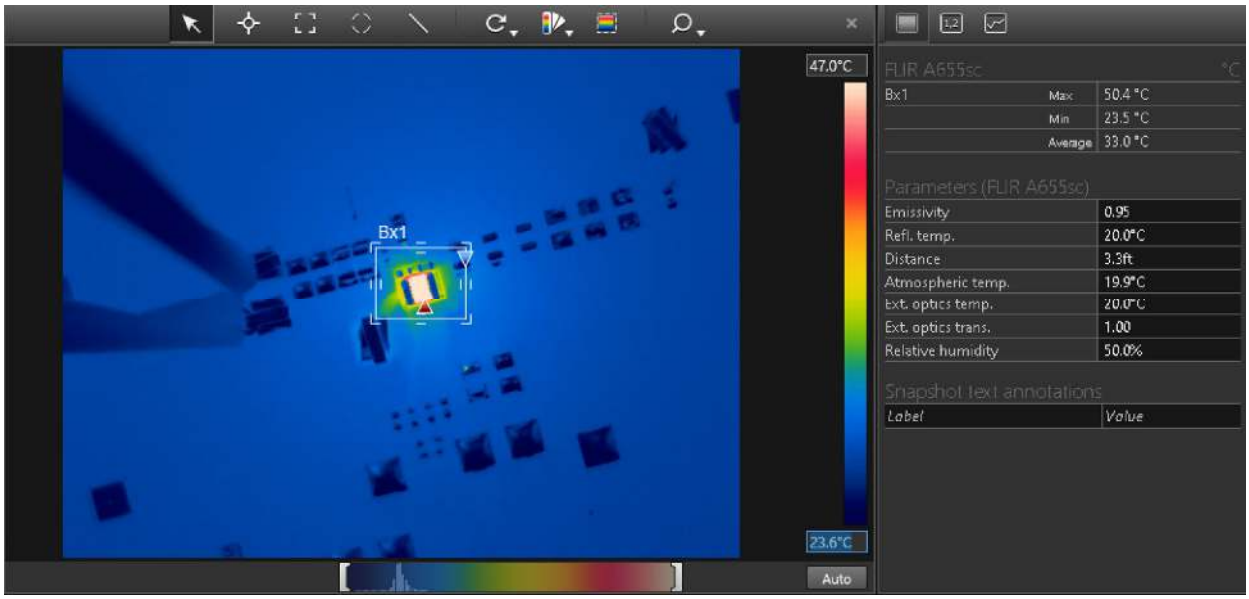


Figure 22 Thermal image (PVIN=5V, I_{OUT} =3A) – maximum temperature rise = 30°C

Layout recommendations

FS1703 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Bypass capacitors, including input/output capacitors and the V_{CC} bypass capacitor (if used), should be placed as close as possible to the FS1703 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- Analog ground and power ground are connected through a single-point connection.
- To aid thermal dissipation, the PGnd pad should be connected to the power ground plane using vias. Copper-filled vias are preferred but plated-through-hole vias are acceptable, provided that they are not filled with resin or covered with solder mask.
- Adequate numbers of vias should be used to make connections between layers, especially for the power traces.
- To minimize power losses and thermal dissipation, wide copper polygons should be used for input and output power connections.

Thermal considerations

The FS1703 has been thermally tested and modelled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1703 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.

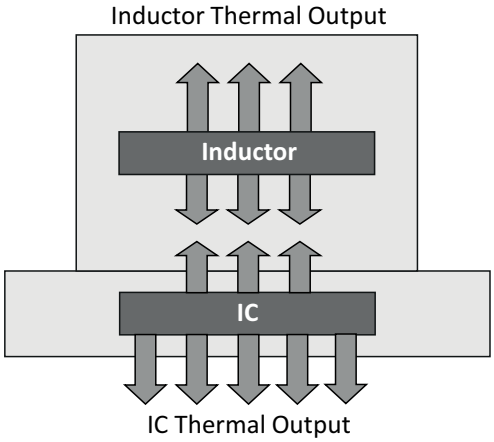


Figure 23 Heat sources in the FS1703

Figure 24 shows the thermal resistances in the FS1703, where:

- Θ_{JA} is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{JCbottom}$ is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- Θ_{JCtop} is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1703 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.

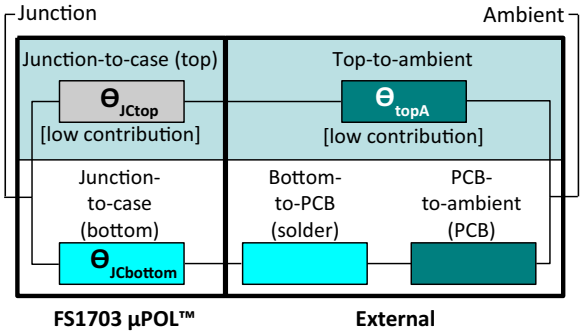


Figure 24 Thermal resistances of the FS1703

The values of the thermal resistances are:

- Θ_{JA} = 22.6°C/W
- $\Theta_{JCbottom}$ = 2.36°C/W

Although these values indicate how the FS1703 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the µPOL™'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

Note: In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

Package description

The FS1703 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate. The finish on the pads is ENiG (Electroless Nickel Immersion Gold).

As a result of these properties, the FS1703 works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Note: Refer to the Design Guidelines for more information about TDK's µPOL™ package series, including importance guidance on checking the compatibility of manufacturing processes such as cleanable flux systems.

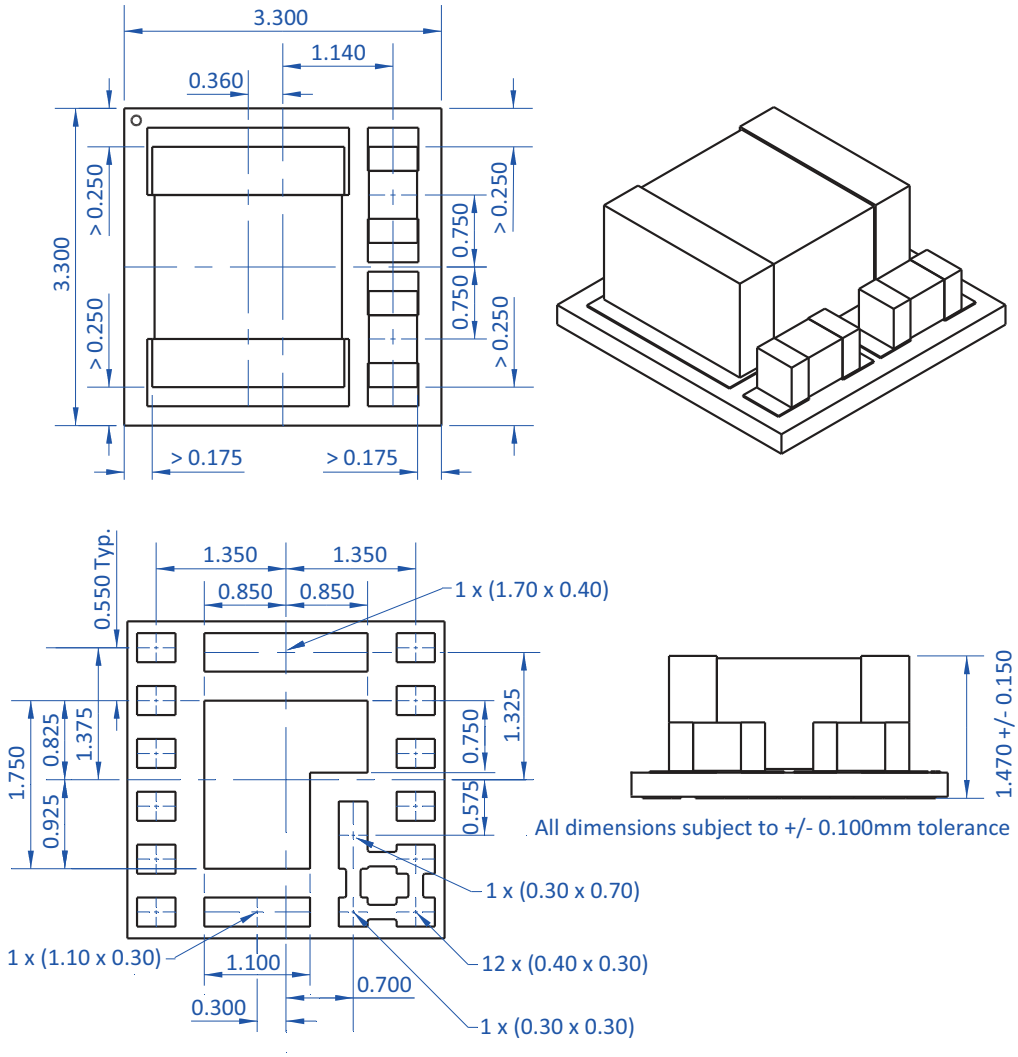
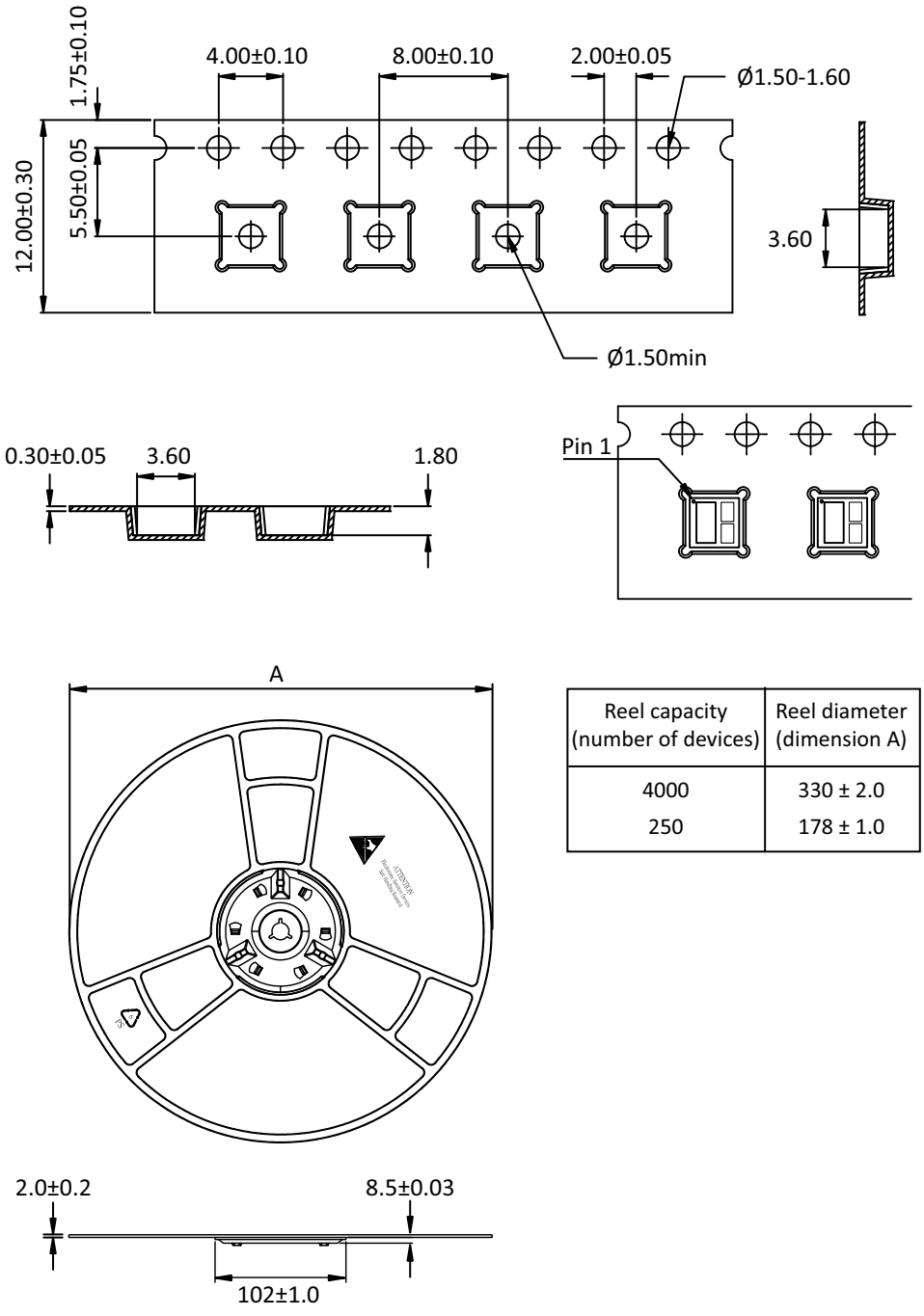


Figure 25 Dimensioned drawings



Reel capacity (number of devices)	Reel diameter (dimension A)
4000	330 ± 2.0
250	178 ± 1.0

Figure 26 Tape and reel pack

REMINDERS FOR USING THESE PRODUCTS

Before using these products, be sure to request the delivery specifications.

SAFETY REMINDERS

Please pay sufficient attention to the warnings for safe designing when using these products.

REMINDER

The products listed on this specification sheet are intended for use in general electric equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal condition and use condition.

The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to sociality, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet.

1. Aerospace/Aviation equipment
2. Transportation equipment (cars, electric trains, ships, etc.)
3. Medical equipment
4. Power-generation control equipment
5. Atomic energy related equipment
6. Seabed equipment
7. Transportation control equipment
8. Public Information-processing equipment
9. Military equipment
10. Electric heating apparatus, burning equipment
11. Disaster prevention/crime prevention equipment
12. Safety equipment
13. Other applications that are not considered general-purpose applications

When using this product in general-purpose application, you are kindly requested to take into consideration securing protection circuit/ equipment or providing backup circuits, etc., to ensure higher safety.