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MAX20446C

Automotive 6-Channel Backlight Driver with Boost/SEPIC Controller and Hybrid Dimming

General Description

The MAX20446C is a 6-channel backlight driver with boost controller for automotive displays. The integrated current outputs can sink up to 130mA LED current each. The device accepts a wide 4.5V to 36V input voltage range and withstands automotive load-dump events.

The internal current-mode switching DC-DC controller supports boost or SEPIC topologies, and operates in the 400kHz to 2.2MHz frequency range. Integrated spread spectrum helps reduce EMI. An adaptive output-voltage-control scheme minimizes power dissipation in the LED current-sink paths.

The device features pulse-width modulation (PWM) dimming and hybrid dimming. In either case, the minimum pulse width is 500ns. Optional phase-shifted dimming of the strings is incorporated for lower EMI.

The MAX20446C is exceptionally easy to configure using a single resistor on the SET pin.

The device is available in a 24-pin TQFN package and operates over the -40 to +125°C temperature range.

Applications

- Infotainment Displays
- Central Information Displays
- Instrument Clusters

Benefits and Features

- Wide Voltage-Range Operation
  - Operates Down to 4V Supply After Startup
  - Survives Load Dump Up to 52V
- High Integration
  - Complete 6-Channel Solution Including Boost Controller
  - All Settings Performed with External Components, No Need for Microcontroller Intervention
- Robust and Low EMI
  - Spread-Spectrum Oscillator
  - Phase Shifting
  - 400kHz to 2.2MHz Switching-Frequency Range
- Versatile Dimming Scheme Allows Hybrid or PWM-Only Dimming
  - Dimming Ratio > 10000:1 Using Hybrid Dimming
  - 10000:1 Dimming Ratio at 200Hz using PWM Dimming
- Complete Fault Protection
  - LED Open/Short Detection and Protection
  - Boost Output Undervoltage and Overvoltage
  - Thermal Shutdown
- Compact (4mm x 4mm) 24-Pin TQFN Package

Ordering Information appears at end of datasheet.

19-100916; Rev 0; 3/21

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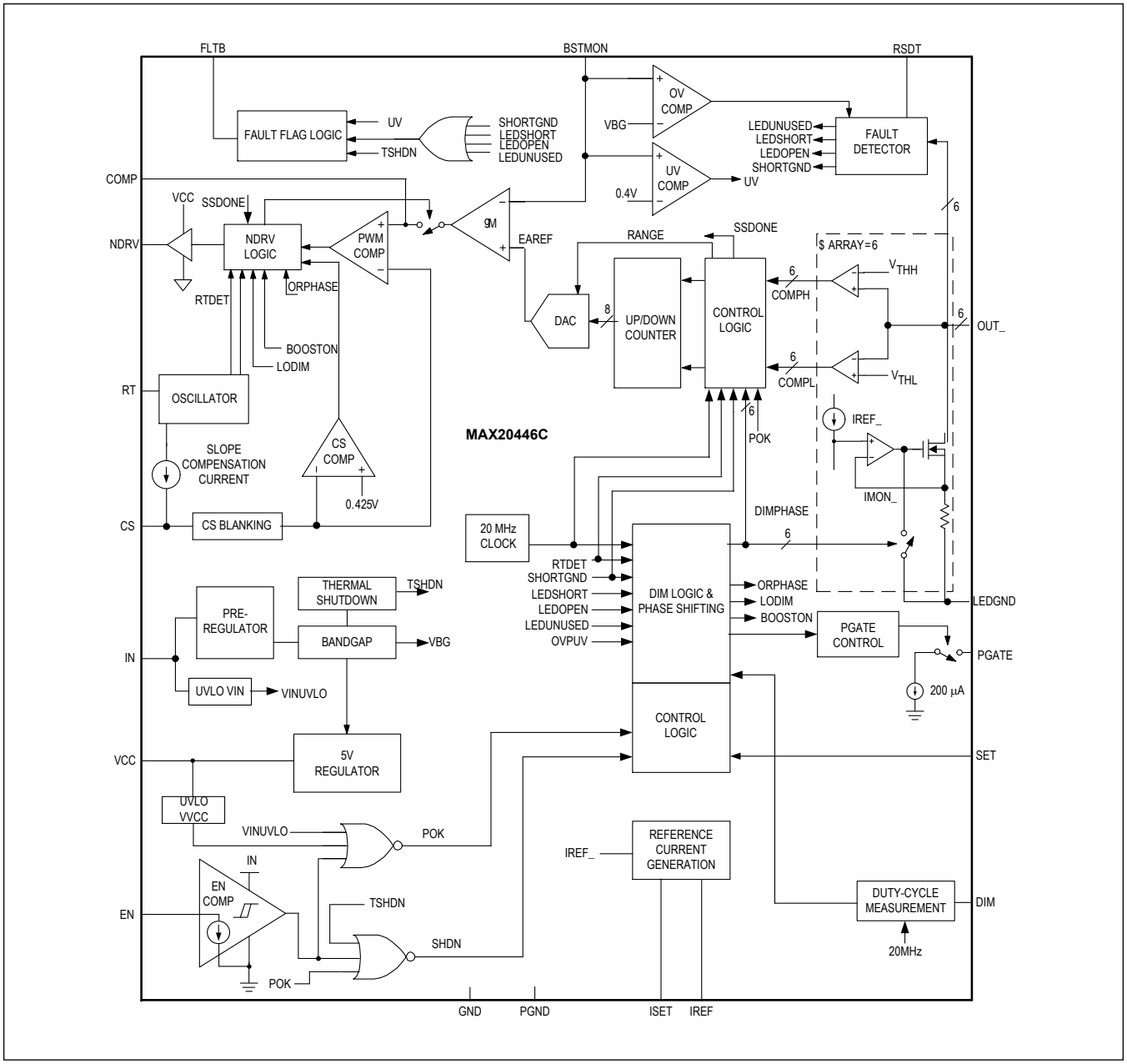
Simplified Block Diagram



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Absolute Maximum Ratings

IN, EN, OUT_, BSTMON, PGATE to GND ..... -0.3V to +52V
PGND, LEDGND to GND ..... -0.3V to +0.3V
V_{CC} to GND.....-0.3V to maximum of (+6, V_{IN} + 0.3)V
FLTB, RSDT, DIM to GND ..... -0.3V to +6V
CS, RT, COMP, NDRV, IREF, ISET, SET to GND-0.3V to V_{CC} + 0.3V
NDRV Peak Current (< 100ns)..... -5A to +5A
NDRV Continuous Current ..... -100mA to +100mA
OUT1-6 Continuous Current ..... -100mA to +150mA
Continuous Power Dissipation Multilayer Board (derate 27.8mW/°C above +70°C) 2.857W
ESDHB ..... -2kV to +2kV
ESDMM.....-200V to +200V
Operating Temperature Range .....-40°C to +125°C
Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T2444+4C
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted., (V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Limits are 100% tested at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT						
Input Operating Range			4.5		36	V
Input Voltage Range After Startup			4.2		36	V
Input Operating Range		IN pin connected to V_{CC}	4.5		5.5	V
Quiescent Supply Current		V_{DIM} = 5V, V_{BSTMON} = 1.3V, OUT1–OUT6 unconnected		10	15	mA
Standby Supply Current		V_{IN} = 12V, V_{EN} = 0V		0.1	1	µA
Undervoltage Lockout, Rising			3.8	4.15	4.45	V

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted., (V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Limits are 100% tested at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout, Falling			3.1	3.7	4	V
Startup Delay		From EN pin high to turn-on of PGATE		1.2	1.8	ms
V_{CC} REGULATOR						
V_{CC} Output Voltage		5.75V < V_{IN} < 36V; I_{VCC} = 1mA to 10mA	4.75	5	5.25	V
Dropout Voltage		V_{IN} = 4.5V, I_{VCC} = 5mA			0.2	V
Short-Circuit Current Limit		V_{CC} shorted to GND		60		mA
V_{CC} Undervoltage-Lockout Threshold, Rising			4.05	4.2	4.35	V
V_{CC} Undervoltage-Lockout Threshold, Falling			3.75	3.9	4.04	V
RT OSCILLATOR						
Switching-Frequency Range	f_{SW}	Frequency dithering disabled	360		2420	kHz
Maximum Duty Cycle		f_{SW} = 400kHz	90	94.5	98.5	%
		f_{SW} = 2200kHz	86	90.5	95	
Oscillator Frequency Accuracy		f_{SW} = 400kHz to 2200kHz, frequency dither disabled	-10		+10	%
Frequency Dither	SS			±6		%
RT Output Voltage	V_{RT}	R_{RT} = 76.8kΩ or R_{RT} = 13.3kΩ	1.2	1.25	1.3	V
Sync Rising Threshold			3			V
Sync Frequency Duty-Cycle Range				50		%
Sync Frequency Range			1.16 x f_{SW}		1.5 x f_{SW}	kHz
MOSFET DRIVER						
NDRV On-Resistance, High Side		NDRV sinking 30mA		1.5	3	Ω
NDRV On-Resistance, Low Side		NDRV sourcing 30mA		0.8	1.6	Ω
NDRV Rise Time		C_{LOAD} = 1nF		8		ns
NDRV Fall Time		C_{LOAD} = 1nF		8		ns
SLOPE COMPENSATION						
Peak Slope-Compensation Current-Ramp Magnitude		Current ramp added to CS	42	50	58	µA

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted., (V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Limits are 100% tested at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE COMPARATOR						
Current-Limit Threshold	V_{CL_MAX}	Includes internal slope-ramp magnitude, V_{CL} = V_{CS} + slope-compensation voltage	390	420	450	mV
ERROR AMPLIFIER						
OUT_ Regulation High Threshold		$V_{OUT_}$ falling	0.95	1.03	1.1	V
OUT_ Regulation Low Threshold		$V_{OUT_}$ rising	0.7	0.78	0.85	V
Transconductance			500	700	880	µS
COMP Sink Current		V_{COMP} = 2V	200	480	800	µA
COMP Source Current		V_{COMP} = 1V	200	480	800	µA
LED CURRENT SINKS						
IREF Voltage	V_{IREF}	R_{IREF} = 49.9kΩ	1.225	1.25	1.275	V
OUT_ Output Current		120mA setting	116	120	124.5	mA
		100mA setting	96	100	104	
		50mA setting	49	50.6	52.2	
Channel-to-Channel Matching		$I_{OUT_}$ = 120mA	-2		+2	%
		$I_{OUT_}$ = 50mA	-2.5		+2.5	
Total OUT_ Leakage Current to IN	$I_{OUTLEAK}$	$V_{OUT_}$ = 48V, V_{DIM} = 0V, all OUT_ pins shorted together		8	12	µA
OUT_ Current Rise Time		10% to 90% $I_{OUT_}$		150		ns
OUT_ Current Fall Time		90% to 10% $I_{OUT_}$		50		ns
DIM Sampling Frequency				20		MHz
LOGIC INPUT AND OUTPUTS						
EN Input Logic-High			2.1			V
EN Input Logic-Low					0.8	V
EN Input Current		V_{EN} = 5V		3	5	µA
DIM Input Logic-High			2.1			V
DIM Input Logic-Low					0.8	V
DIM Input Pullup Current				5		µA
FLTB Output Low Voltage		Sinking 3mA			0.4	V
FLTB Output Leakage Current		V_{FLTB} = 5.5V	-1		+1	µA

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted., (V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 1µF, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Limits are 100% tested at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.))

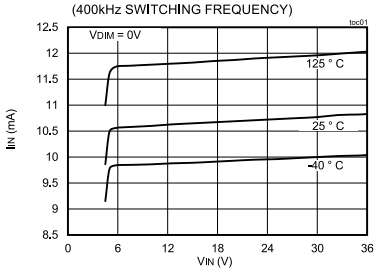
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
BSTMON Overvoltage Trip Threshold		BSTMON rising	1.18	1.23	1.28	V
BSTMON Hysteresis				70		mV
BSTMON Input Bias Current		0V < V_{BSTMON} < 1.3V	-500		500	nA
BSTMON Undervoltage Detection Threshold		BSTMON falling, PGATE latched off	0.4	0.43	0.46	V
Boost Undervoltage Blanking Time		After EN pin high	23.5	26	28.5	ms
BSTMON Undervoltage Detection Delay		BSTMON falling	4	10	18	µs
PGATE Pulldown Current			180	210	245	µA
PGATE Start Delay		Delay between PGATE going low and boost converter starting		2	2.2	ms
PGATE Leakage Current		V_{PGATE} = 12V, V_{EN} = 0V		0.1	1	µA
LED FAULT DETECTION						
LED Short-Detection Disable Threshold	$V_{RSDTOFF}$	RSDT rising	2.3	2.5		V
LED Short-Detection Threshold		V_{RSDT} = 2V	7.6	8	8.4	V
Short-Detection Comparator Delay				9		µs
OUT_ Check LED Source Current			50	60	70	µA
OUT_ Short-to-GND Detection Threshold		Before boost converter startup	250	300	365	mV
OUT_ Unused Detection Threshold			1.15	1.25	1.35	V
OUT_ Open-LED Detection Threshold		During operation	250	300	365	mV
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold				165		°C
Thermal-Shutdown Hysteresis				15		°C

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

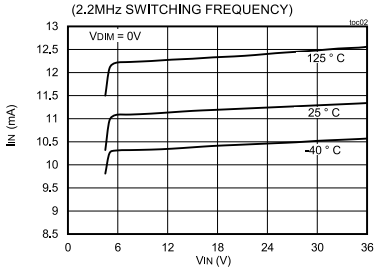
Typical Operating Characteristics

((VIN = VEN = +12V, 6x6 LED load at 100mA, TA = +25°C, unless otherwise noted.))

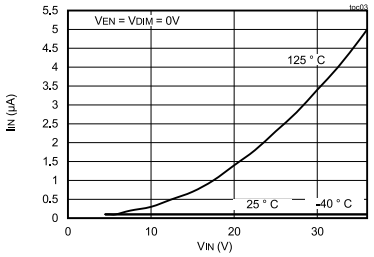
SUPPLY CURRENT vs. SUPPLY VOLTAGE (400kHz SWITCHING FREQUENCY)



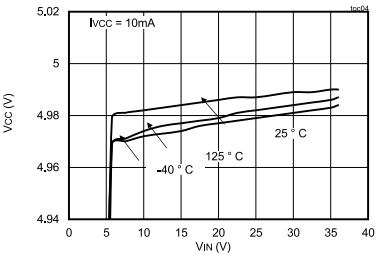
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2.2MHz SWITCHING FREQUENCY)



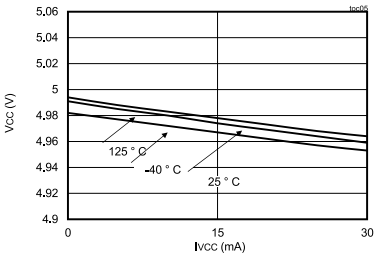
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



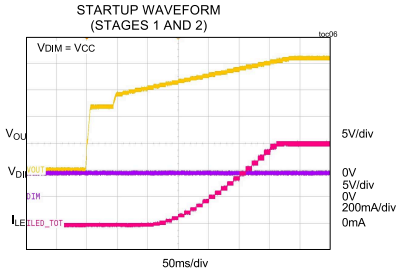
VCC LINE REGULATION



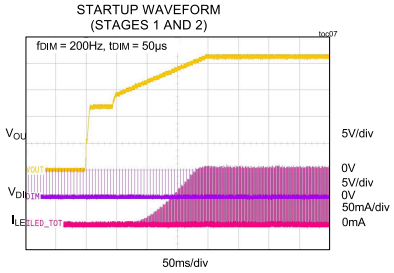
VCC LOAD REGULATION



STARTUP WAVEFORM (STAGES 1 AND 2)

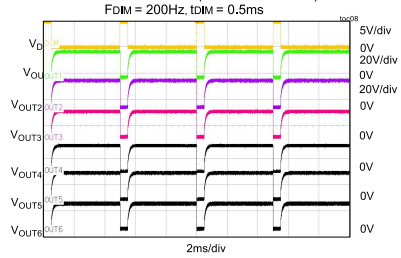


STARTUP WAVEFORM (STAGES 1 AND 2)



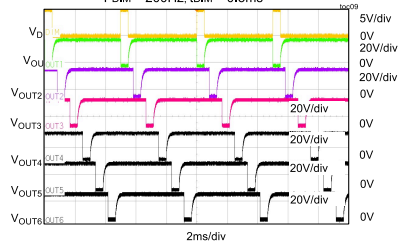
DIMMING WAVEFORM (MAX20446CATGB)

FDIM = 200Hz, tDIM = 0.5ms

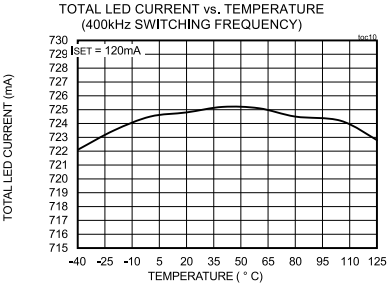


DIMMING WAVEFORM (MAX20446CATGA)

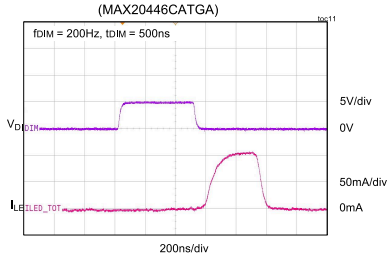
FDIM = 200Hz, tDIM = 0.5ms



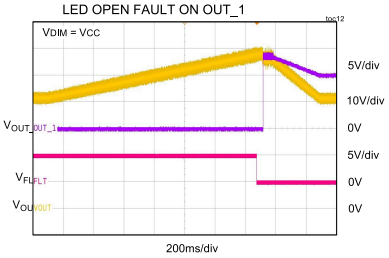
TOTAL LED CURRENT vs. TEMPERATURE (400kHz SWITCHING FREQUENCY)



LED CURRENT WITH DIMMING TON = 500ns (MAX20446CATGA)

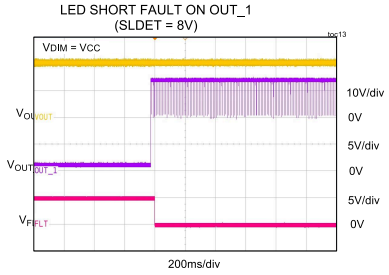


LED OPEN FAULT ON OUT_1



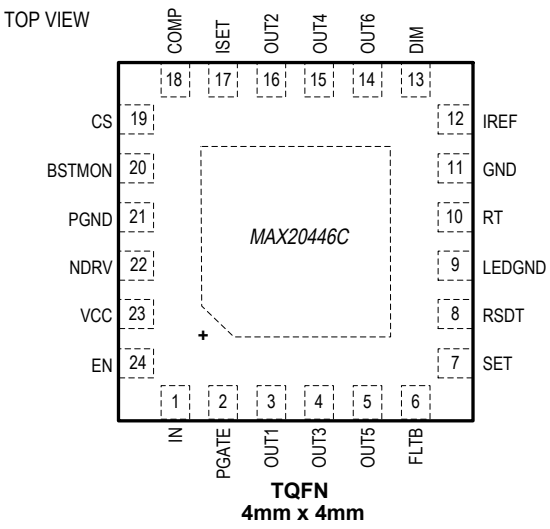
Typical Operating Characteristics (continued)

((VIN = VEN = +12V, 6x6 LED load at 100mA, TA = +25°C, unless otherwise noted.))



Pin Configuration

MAX20446C



Pin Description

PIN	NAME	FUNCTION
1	IN	Bias Supply Input. Connect a 4.5V to 36V supply to IN. Bypass IN to GND with a 2.2µF ceramic capacitor.
2	PGATE	Gate Connection for External Series pMOSFET.
3	OUT1	LED String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT1. OUT1 sinks up to 130mA.
4	OUT3	LED String Cathode Connection 3. OUT3 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT3. OUT3 sinks up to 130mA.

Pin Description (continued)

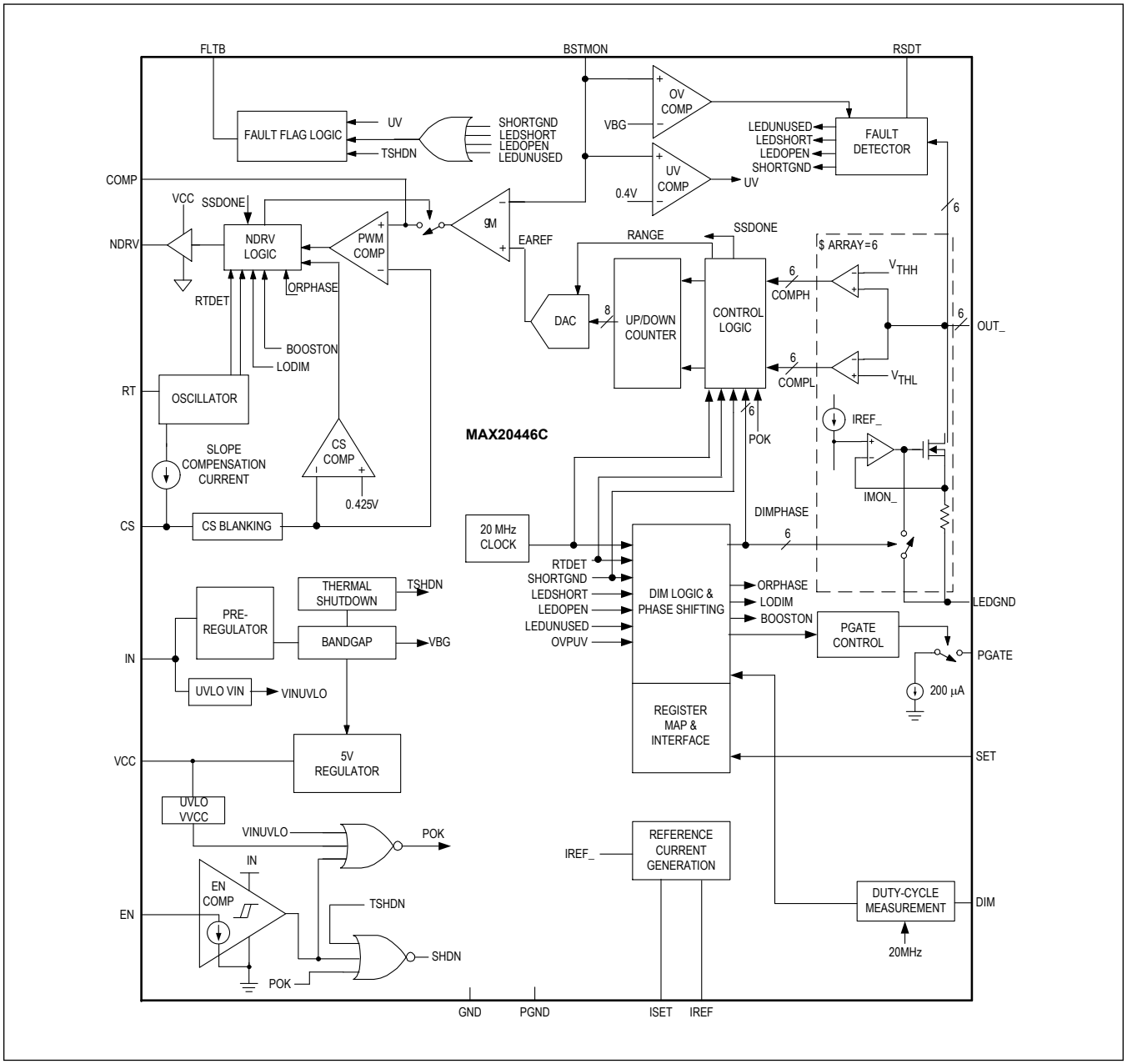
PIN	NAME	FUNCTION
5	OUT5	LED String Cathode Connection 5. OUT5 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT5. OUT5 sinks up to 130mA.
6	FLTB	Open-Drain Fault Output. FLTB asserts low when any diagnostic bit (that is not masked) is asserted. See the *Fault Protection* section for more details. Connect a pullup resistor from FLTB to V_{CC}.
7	SET	Hybrid Dimming and Current Range Setting Input. Connect a resistor from SET to ground to set the hybrid dimming threshold and the LED current range. The state of the SET pin is read once at power-up; settings cannot be changed subsequently unless the device power or EN pin is toggled.
8	RSDT	LED Short-Detection Threshold-Adjust Input. Connect a resistive divider from V_{CC} to RSDT and GND to program the LED short-detection threshold. Do not set the RSDT voltage lower than 1.3V. Connect RSDT directly to VCC to disable LED short detection.
9	LEDGND	LED Ground. LEDGND is the return path connection for the linear current sinks. Connect GND, LEDGND, and PGND at a single point.
10	RT	Oscillator Timing Resistor Connection. Connect a timing resistor (R_{RT}) from RT to GND to program the switching frequency. In addition, connect a 100pF capacitor from RT to GND. To synchronize the switching frequency with an external clock, apply an AC-coupled external clock at RT. When the oscillator is synchronized with the external clock, spread spectrum is disabled.
11	GND	Signal Ground. GND is the current return path connection for the low-noise analog signals. Connect GND, LEDGND, and PGND at a single point.
12	IREF	LED Current Reference Input. Connect a resistor (R_{IREF} = 49.9kΩ) from IREF to GND to set the current reference according to the formula IREF = 1.250/R_{IREF}.
13	DIM	PWM Dimming Input. Apply a PWM signal to DIM for LED dimming control unless I^2C dimming is used. Connect DIM to V_{CC} if dimming control is not used (100% brightness). Connect DIM to GND if dimming is to be controlled through I^2C.
14	OUT6	LED String Cathode Connection 6. OUT6 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT6. OUT6 sinks up to 130mA.
15	OUT4	LED String Cathode Connection 4. OUT4 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT4. OUT4 sinks up to 130mA.
16	OUT2	LED String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 130mA.
17	ISET	LED Current-Adjust Input. Connect a resistor (R_{ISET}) from ISET to GND to set the current through each LED string (ILED). The state of the ISET pin is read once at power-up and the current cannot be changed subsequently.
18	COMP	Switching-Converter Compensation Input. Connect the compensation network from COMP to GND for current-mode control (see the *Feedback Compensation* section for details).
19	CS	Current-Sense Input. CS is the current-sense input for the switching regulator. A sense resistor connected from the source of the external power MOSFET to PGND sets the switching current limit. A resistor connected between the source of the power MOSFET and CS sets the slope-compensation ramp rate (see the *Slope Compensation and Current-Sense Resistor* section).
20	BSTMON	Overvoltage Threshold-Adjust Input. Connect a resistor-divider from the switching converter output to BSTMON and GND. The OVP comparator reference is internally set to 1.23V.
21	PGND	Power Ground. PGND is the switching-current return-path connection. Connect GND, LEDGND, and PGND at a single point.
22	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching-power MOSFET. Typically, a small resistor (1Ω to 22Ω) is inserted between the NDRV output and nMOSFET gate to decrease the slew rate of the gate driver and reduce the switching noise.

Pin Description (continued)

PIN	NAME	FUNCTION
23	VCC	5V Regulator Output. Bypass V_{CC} to GND with a minimum of 1µF ceramic capacitor with 22nF in parallel placed as close as possible to the pin.
24	EN	Enable Input. Connect EN to ground to shut down the device. Connect EN to logic-high or IN for normal operation. EN has an internal clamp at 3.9V. When EN is above this voltage, an input current of (V_{EN} - 3.9V)/1.2MΩ will flow.
-	EP	Exposed Pad. Connect EP to a large-area contiguous copper-ground plane for effective power dissipation. Do not use as the main IC ground connection. EP **must** be connected to GND.

Functional Diagrams

MAX20446C



Detailed Description

The MAX20446C high-efficiency HB LED driver integrates all the necessary features to implement a high-performance backlight driver to power LEDs in medium-to-large-sized displays for automotive, as well as general, applications. The device provides load-dump voltage protection up to 52V in automotive applications and incorporates a DC-DC controller with peak current-mode control to implement a boost or a SEPIC-type switched-mode power supply and a 6-channel LED driver with 45mA to 130mA constant-current sink capability per channel.

Enable

When the EN pin is taken high, the internal regulator is first turned on if the IN pin voltage is above its undervoltage lockout. Then the PGATE output is turned on. Finally, the boost converter and current sinks are enabled. To shut down the device, drive EN low so the current consumption is reduced to 1µA (max).

Undervoltage Lockout

The device features two undervoltage lockouts (UVLOs) that monitor the input voltage at IN and the output of the internal LDO regulator at V_{CC}. The device turns on when EN is taken high if both IN and V_{CC} are higher than their respective UVLO thresholds.

Current-Mode DC-DC Controller

The device has a constant-frequency, current-mode controller designed to drive the LEDs in a boost, SEPIC, or coupled-inductor buck-boost configuration. The device features multiloop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks to minimize power dissipation.

The switching frequency can be programmed over the 400kHz to 2.2MHz range using a resistor connected from RT to GND.

Internal slope compensation is provided to compensate for subharmonic oscillations that occur at above 50% duty cycles in continuous-conduction mode.

The external MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}), connected from the source of the external MOSFET to ground.

The device features leading-edge blanking to suppress the external MOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the MOSFET when the voltage at CS exceeds the error amplifier's output voltage, which is also the voltage on the COMP pin. This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the device has two other feedback loops for control. The converter output voltage is sensed through the BSTMON input, which goes to the inverting input of the error amplifier. The other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of 0.78V and a high threshold of 1.03V. The outputs of these comparators control an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit DAC that sets the reference to the error amplifier. When dimming is set to 100%, the counter is updated at intervals of 10ms.

8-Bit Digital-to-Analog Converter

The error amplifier's reference input is controlled with an 8-bit digital-to-analog converter (DAC). The DAC output ramps up slowly during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited to 0.6V to 1.25V. Because the DAC output is limited to no less than 0.6V during normal operation, the overvoltage threshold for the output should be set to a value less than twice the minimum LED forward voltage. The DAC LSB determines the minimum step-in output voltage according to Equation 1.

Equation 1:

$$V_{STEP_MIN} = V_{DAC_LSB} \times A_{OVP}$$

where:

V_{STEP_MIN} = Minimum output-voltage step

V_{DAC_LSB} = DAC least significant bit size (2.5mV)

A_{OVP} = BSTMON resistor-divider gain

Dimming

Dimming is performed by applying a PWM signal to the DIM pin. The signal on the DIM pin is sampled with a 20MHz internal clock.

Hybrid Dimming

In hybrid dimming mode, the external LEDs are dimmed by first reducing their current as the dimming duty-cycle decreases from 100% (see Figure 1). At the crossover level set by the resistor on SET, dimming transitions to PWM dimming where the LED current is chopped. The device measures the duty-cycle on the DIM pin and translates it into a combined LED current value and PWM setting.

Hybrid Dimming Operation

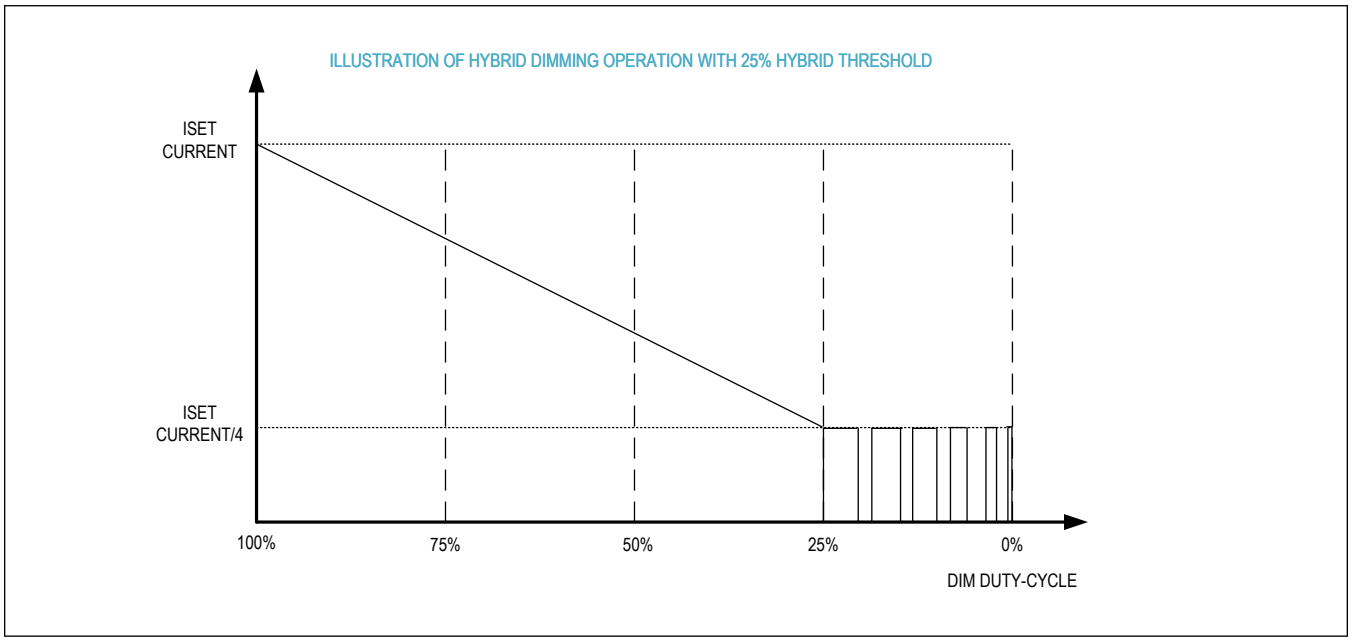


Figure 1. Hybrid Dimming Operation

Low-Dimming Mode

The device operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. If the dimming on-time is lower than 50µs (typ), the device enters low-dimming mode. In this state, the converter switches continuously and the LED short detection is disabled. When the DIM input is greater than 51µs (typ), the device goes back into normal operation, enabling the short-LED detection and switching the power MOSFET only when the effective dimming signal is high. OUT_ current monitoring does not operate in low-dim mode although the BSTMON voltage can still be measured.

Phase-Shift Dimming

The MAX20446CATGA has phase-shifting enabled. The device automatically sets the phase shift between strings to 60, 72, 90, 120, or 180 degrees, depending on the number of strings enabled.

If phase shifting between the strings is not needed, select the MAX20446CATGB.

Disabling Individual Strings

To disable an unused LED string, connect the unused OUT_ to ground through a 12kΩ resistor. During startup, the device sources 60µA (typ) current through the OUT_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT_ voltage should measure between 350mV and 1.15V during this check. The maximum threshold for the OUT_ short-to-ground check is 350mV and the minimum unused string-detection threshold is 1.15V.

Note: When disabling unused strings, start by disabling the highest numbered current sinks first (e.g., if two strings need to be disabled, disable OUT6 and OUT5. Do not disable any two strings at random).

Startup Sequence

When the EN pin is taken high (assuming the IN voltage is above its undervoltage-lockout value), the internal regulator is turned on and the device checks the OUT_ channels. If any of the OUT_ pins are detected as shorted to GND, the boost converter does not start (to avoid possible damage) and the FLTB pin goes low. The device also detects and disconnects any unused current-sink channels that are connected to GND through a 12kΩ resistor. The total duration of this phase of the startup is 2ms (max). After this phase, the startup sequence occurs in three stages (see the Stage 1, Stage 2, and Stage 3 sections).

Stage 1

After the initial checks described above, the controller begins the soft-start of the boost. First the driver of the external pMOSFET is turned on. A constant current of 200µA (typ) then flows into the PGATE pin of the device. This current flows into the external gate-source resistor and pulls down the gate of the external pMOSFET and turns it on. An external gate-source capacitor can be used to control the turn-on time of the external pMOSFET.

After the external pMOSFET is turned on and a 2ms timeout expires, Stage 2 of the startup begins (see the Stage 2 section).

Stage 2

After the Stage 1 timeout, the converter starts switching and the output begins to ramp. The DAC reference to the error amplifier is stepped up one bit at a time until it reaches 1.2V. This stage duration is fixed at approximately 25ms (typ). The BSTMON pin is then monitored, and if the voltage at the BSTMON pin is less than 930mV (typ), FLTB is asserted low, the power converter is turned off, the external pMOSFET is turned off, and they all remain off until the EN pin or device power is toggled (see the Stage 3 section).

Stage 3

The third stage begins once Stage 2 is complete and the DIM input goes high. During Stage 3, the output of the converter is adjusted until the minimum OUT_ voltage falls within 0.68V (typ) and 0.93V (typ) comparator limits. The output adjustment is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input pin. If the DIM input is at 100% duty cycle (DIM = high), the DAC output is updated once every 10ms.

The total soft-start time can be calculated using Equation 2.

Equation 2:

$$t_{SS} = 26ms + \frac{(V_{LED} + 0.91) - (0.6 \times A_{OVP})}{f_{DIM} \times 0.01 \times A_{OVP}}$$

where:

SS = Total soft-start time,

26ms = Fixed Stage 1 + Stage 2 duration,

V_{LED} = Total forward voltage of the LED strings,

0.91V = Midpoint of the window comparator,

f_{DIM} = Dimming frequency (use 100Hz for f_{DIM} when input duty cycle is 100%),

0.01V = 4 times the 2.5mV LSB of the DAC, and

A_{OVP} = Gain of the BSTMON resistor-divider or 1 + R6/R7.

After the soft-start period, a fault is detected whenever the BSTMON pin falls below 430mV (typ). When this occurs, the power converter is latched off and PGATE goes high. Cycling the EN pin or the supply is required to start up again once the fault condition has been removed.

Boost Startup

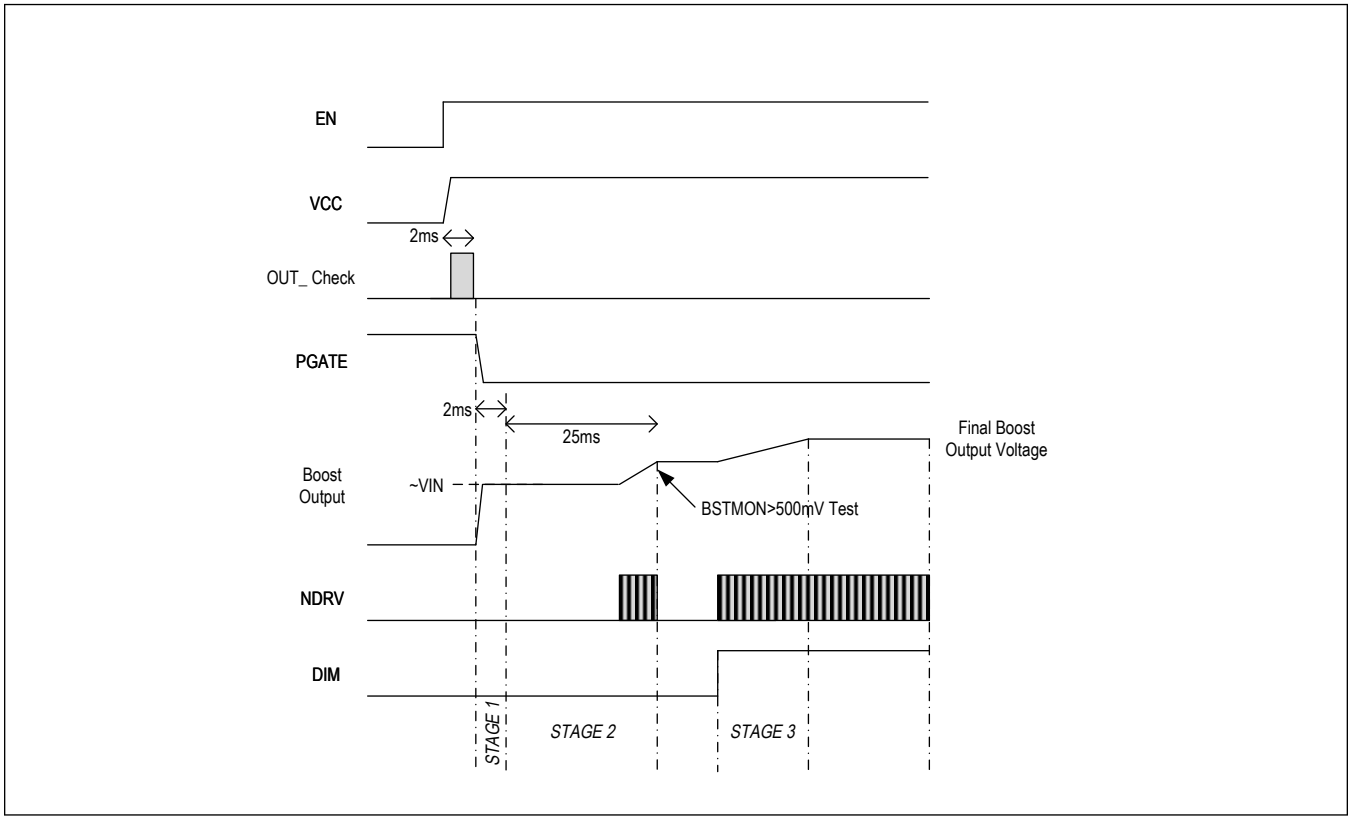


Figure 2. Boost Startup

Oscillator Frequency/External Synchronization

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a timing resistor (R_{RT}) connected from the RT pin to GND. Use Equation 3 to calculate the value of R_{RT} for the desired switching frequency (f_{SW}).

Equation 3:

$$R_{RT} = \frac{29260 + (2200 - f_{SW}) \times 0.81}{f_{SW}}$$

where f_{SW} is in kHz and R_{RT} is in kΩ.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the RT input. The value of the capacitor used for AC-coupling is C_{SYNC} = 10pF and the duty cycle of the external clock should be 50%.

Spread-Spectrum Switching

The device includes spread spectrum, which reduces peak electromagnetic interference (EMI) at the boost converter switching frequency and its harmonics.

The spread spectrum uses a pseudo-random dithering technique where the switching frequency is varied in the range of 94% of the programmed switching frequency, to 106% of the programmed switching frequency, set through the external resistor from RT to GND. The total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the energy peak.

Spread spectrum is disabled if external synchronization is used.

5V LDO Regulator (V_{CC})

The internal LDO regulator converts the input voltage at IN to a 5V output voltage at V_{CC}. The LDO regulator supplies up to 50mA current to provide power to internal control circuitry and the gate driver. Bypass V_{CC} to GND, with a minimum of 1µF (+22nF in parallel) ceramic capacitor, as close as possible to the device.

LED Current Control

The full-scale sink current for the outputs OUT1–OUT6 is set using the resistors on the ISET and SET pins. When PWM dimming is used, the current in the OUT_ channels switches between zero and the full-scale sink current at the set duty cycle.

When hybrid dimming is used, the sink current in OUT1–OUT6 is reduced linearly from the full-scale value until the hybrid dimming threshold is reached; dimming at lower levels is then accomplished using PWM (see Figure 1).

Fault Protection

Fault protection in the device includes cycle-by-cycle current limiting using the PWM controller, DC-DC converter output undervoltage protection, output overvoltage protection, open-LED detection, short-LED detection and protection, and overtemperature shutdown. An open-drain fault flag output (FLTB) goes low when an open-LED string is detected, a short-LED string is detected, during an output undervoltage, or during thermal shutdown. FLTB is cleared when the fault condition is removed during thermal shutdown and in the case of shorted LEDs. FLTB is latched low for an open LED and can be reset by cycling power or toggling the EN pin. The thermal-shutdown threshold is +165°C and has +15°C hysteresis.

Open-LED Management and Overvoltage Protection

On power-up, the device performs a soft-start of the boost converter. After soft-start, the device detects open-LED and disconnects any strings with an open LED from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency.

During normal operation, the DC-DC converter output-regulation loop uses the minimum OUT_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, the BSTMON input, and GND. The overvoltage-protection threshold at the DC-DC converter output is determined using the Equation 4.

Equation 4:

$$V_{OUT_BSTMON} = 1.23 \times \left(1 + \frac{R6}{R7}\right)$$

where 1.23 (typ) is the overvoltage threshold on BSTMON (see *Functional Diagrams*). Select V_{OUT_BSTMON} according to Equation 5.

Equation 5:

$$1.1 \times \left(V_{LED_MAX} + 1.1\right) < V_{OUT_BSTMON} < 2 \times \left(V_{LED_MIN} + 0.7\right)$$

where:

V_{LED_MAX} = Maximum expected LED string voltage, and

V_{LED_MIN} = Minimum expected LED string voltage.

Select R6 and R7 such that the voltage at OUT_ does not exceed the *Absolute Maximum Ratings*. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the internal MOSFET is switched off.

The overvoltage threshold should be set to less than twice the minimum LED voltage to ensure proper operation; the BSTMON minimum regulation point is 600mV (typ). Connect a 12kΩ resistor between OUT_ and LEDGND for each unused channel to avoid overvoltage triggering at startup. When an open-LED overvoltage condition occurs, FLTB is latched low. Any current-sink output with $V_{OUT_}$ < 300mV (typ) is disconnected from the minimum voltage detector.

Short-LED Detection

The device checks for shorted LEDs as the current in any channel is turned on. A shorted LED is detected at OUT_ if the condition in Equation 6 is met.

Equation 6:

$$V_{OUT_} = 4 \times V_{RSDT}$$

where:

V_{RSDT} is the DC voltage on the RSDT pin.

If a short is detected on any of the strings, the affected LED strings are disconnected for the remainder of the DIM cycle and the FLTB output flag asserts until the device detects that the shorts are removed. Disable short-LED detection by connecting RSDT to V_{CC}. Short-LED detection is disabled in low-dimming mode. When the DIM input is connected continuously high, the OUT_ pins are periodically scanned to detect shorted LEDs. The scan frequency is 100Hz.

Thermal Shutdown

The device includes thermal protection that operates at a temperature of 165°C. When the thermal-shutdown temperature is reached, the device is immediately disabled and begins to cool. When the junction temperature falls by 15°C, the device is re-enabled with the same settings as before (the boost converter performs a soft-start). When a thermal shutdown occurs, the FLTB pin goes low.

Device Configuration

Set the peak LED current using the ISET and SET pins as shown below. To select a current of 130mA, use an ISET resistor of 84.5kΩ with a resistor on the IREF pin of value 45.3kΩ.

Table 1. LED Current Setting

R_{ISET}	CURRENT RANGE	CURRENT SETTING
3480	Low	45mA
7150	Low	50mA
12k	Low	55mA
18.7k	Low	60mA
27.4k	Low	65mA
39k	Low	70mA
59k	Low	75mA
84.5k	Low	80mA
3480	High	85mA
7150	High	90mA
12k	High	95mA
18.7k	High	100mA
27.4k	High	105mA

Table 1. LED Current Setting (continued)

R_{ISET}	CURRENT RANGE	CURRENT SETTING
39k	High	110mA
59k	High	115mA
84.5k	High	120mA

The following dimming modes are available:

1. External PWM dimming.
2. External Hybrid dimming with a PWM signal applied to the DIM pin. In this mode the device automatically determines whether the LED current is to be dimmed by reducing the LED current or by chopping the LED current (depending on the hybrid dimming threshold).

Hybrid dimming can be used in stand-alone mode by connecting a resistor from SET to GND. The resistor selects either the low-current or high-current range and the current value where analog dimming transitions to PWM dimming:

Table 2. Hybrid-Dimming Current-Range Settings

CURRENT RANGE SETTING	R_{SET} (Ω)	HYBRID DIMMING THRESHOLD
Low	3480	Hybrid dimming disabled
Low	8200	50% of peak LED current
Low	14k	25% of peak LED current
Low	21.5k	12.5% of peak LED current
Low	27.4k	6.25% of peak LED current
High	36.5k	50% of peak LED current
High	47k	25% of peak LED current
High	59k	12.5% of peak LED current
High	75k	6.25% of peak LED current
High	SET shorted to V_{CC}	Hybrid dimming disabled

The state of the ISET, and SET pins is read at start-up and stored in the device. The resulting settings cannot be changed subsequently unless the device is powered down and back up again.

Applications Information

DC-DC Converter

Three different converter topologies are possible with the DC-DC converter in the MAX20446C, which has the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always greater than the input supply-voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply-voltage range, use a buck-boost converter topology. The possible buck-boost topologies are SEPIC, or a coupled-inductor buck-boost topology. The latter is basically a flyback converter with 1:1 turns ratio. 1:1-coupled inductors are available with tight coupling suitable for this application.

The boost-converter topology provides the highest efficiency among the aforementioned topologies. The coupled-inductor topology has the advantage of not using a coupling capacitor, but does require tightly coupled windings to avoid additional snubber components. The SEPIC configuration requires two inductors (or a coupled inductor) and a coupling capacitor. Furthermore, the feedback-loop compensation for SEPIC becomes complex if the coupling capacitor is not large enough.

Power-Circuit Design

First, select a converter topology based on the factors listed in the *DC-DC Converter* section. Determine the required input supply voltage range, the maximum voltage needed to drive the LED strings, including the minimum 0.85V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}), as shown in Equation 7.

Equation 7:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where I_{STRING} is the current per string and N_{STRING} is the number of strings used.

Next, calculate the maximum duty cycle (D_{MAX}) using Equations 8 and 9.

For boost configuration (Equation 8):

$$D_{MAX} = \frac{\left(V_{LED} + V_{D1} - V_{IN_MIN}\right)}{\left(V_{LED} + V_{D1} - V_{DS} - 0.3\right)}$$

For SEPIC and coupled-inductor buck-boost configurations (Equation 9):

$$D_{MAX} = \frac{V_{LED} + V_{D1}}{\left(V_{IN_MIN} - V_{DS} - 0.3 + V_{LED} + V_{D1}\right)}$$

where:

- V_{D1} = Forward drop of the rectifier diode in volts (approximately 0.6V),
- V_{IN_MIN} = Minimum input supply voltage, and
- V_{DS} = Drain-to-source voltage of the external MOSFET when it is on.

Select the switching frequency (f_{SW}) depending on the space, noise, and efficiency constraints.

Boost and Coupled-Inductor Configurations

In all three converter configurations, the average inductor current varies with the line voltage; the maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔI_L). The recommended maximum peak-to-peak ripple is 60% of the average inductor current, but lower and higher values for ripple are also acceptable.
Use the following equations (Equations 10, 11, and 12) to calculate the maximum average inductor current (I_{LAVG}) and peak inductor current (I_{LP}) in amperes.

Equation 10:

$$I_{LAVG} = \frac{I_{LED}}{\left(1 - D_{MAX}\right)}$$

Allowing the peak-to-peak inductor ripple ΔI_L to be ±30% of the average inductor current:

Equation 11:

$$\Delta I_L = I_{LAVG} \times 0.3 \times 2$$

and:

$$I_{LP} = I_{LAVG} + \frac{\Delta I_L}{2}$$

Calculate the minimum inductance value (L_{MIN}), in henries (H), with the inductor current ripple set to the maximum value:

Equation 12:

$$L_{MIN} = \frac{\left(V_{IN_MIN} - V_{DS} - 0.3\right) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and current rating greater than I_{LP}. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration. For the coupled-inductor, the saturation limit of the inductor with only one winding conducting should be 10% higher than I_{LP}.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts. One of the inductors (L2) takes LED current as the average current and the other (L1) takes input current as the average current.

Use the following equations (Equations 13–16) to calculate the average inductor currents (I_{L1AVG}, I_{L2AVG}) and peak inductor currents (I_{L1P}, I_{L2P}) in amperes.

Equation 13:

$$I_{L1AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses.

Equation 14:

$$I_{L2AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔI_L is ±30% of the average inductor current

Equation 15:

$$\Delta I_{L1} = I_{L1AVG} \times 0.3 \times 2$$

and:

$$I_{L1P} = I_{L1AVG} + \frac{\Delta I_{L1}}{2}$$

and:

$$\Delta I_{L2} = I_{L2AVG} \times 0.3 \times 0.2$$

and:

$$I_{L2P} = I_{L2AVG} + \frac{\Delta I_{L2}}{2}$$

Calculate the minimum inductance values ($L1_{MIN}$ and $L2_{MIN}$) in henries with the inductor current ripple set to the

maximum value shown in Equation 16.

Equation 16:

$$L1_{MIN} = \frac{\left(V_{IN_MIN} - V_{DS} - 0.3\right) \times D_{MAX}}{f_{SW} \times \Delta I_{L1}}$$

$$L2_{MIN} = \frac{\left(V_{IN_MIN} - V_{DS} - 0.3\right) \times D_{MAX}}{f_{SW} \times \Delta I_{L2}}$$

Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$, and current rating greater than I_{L1P} and I_{L2P}, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

To simplify further calculations, consider L1 and L2 as a single inductor with L1 and L2 connected in parallel. The combined inductance value and current is calculated as shown in Equation 17.

Equation 17:

$$L = \frac{L1 \times L2}{L1 + L2}$$

and:

$$I_{LAVG} = I_{L1AVG} + I_{L2AVG}$$

where I_{LAVG} represents the total average current through both the inductors in the SEPIC configuration. Use these values in the calculations in the following sections.

Select coupling-capacitor C_S so that the peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series-resonant circuit comprising L1, C_S, and L2 do not affect the normal operation of the converter. Use Equation18 to calculate the minimum value of C_S:

Equation 18:

$$C_S = \frac{I_{LED} \times D_{MAX}}{V_{IN_MIN} \times 0.02 \times f_{SW}}$$

where:

- C_S = Minimum value of the coupling capacitor in farads, and
- 0.02 = 2% ripple factor.

Slope Compensation and Current-Sense Resistor

The device generates a current ramp for slope compensation. This ramp current is in sync with the switching frequency and starts from zero at the beginning of every clock cycle, rising linearly to reach 50µA at the end of the clock cycle. The slope-compensating resistor (R_{SC}) is connected between the CS input and the source of the external switching MOSFET. This adds a programmable ramp voltage to the CS input voltage to provide slope compensation.

Use one of the the following equations (Equation 19 or 20) to calculate the value of R_{SC}.

For boost configuration (Equation 19):

$$R_{SC} = \frac{(V_{LED} - 2 \times V_{IN_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

For SEPIC and coupled-inductor configurations (Equation 20):

$$R_{SC} = \frac{(V_{LED} - V_{IN_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where:

- V_{LED} and V_{IN_MIN} are in volts,
- R_{SC} and R_{CS} are in ohms,

- L_{MIN} is in henries, and
- f_{SW} is in hertz.

The value of the switch current-sense resistor (R_{CS}) can be calculated using the boost configuration shown in Equation 21.

Equation 21:

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.39 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times \left(V_{LED} - 2 \times V_{IN_MIN}\right) \times 3}$$

For SEPIC and coupled-inductor configurations, use Equation 22.

Equation 22:

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.39 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times \left(V_{LED} - V_{IN_MIN}\right) \times 3}$$

where 0.39 is the minimum value of the peak current-sense threshold. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.39 is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

For all three converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across constant-current sink outputs because the LED-string voltages are stable due to the constant current. For the MAX20446C, limit peak-to-peak output-voltage ripple to 200mV to get stable output current.

Use the following equation to calculate the minimum capacitor value:

$$C_{OUT(MIN)} = \frac{I_{LED} \times DMAX}{0.2 \times f_{SW}}$$

The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitors on the output are usually minimized. In this case, an additional electrolytic or aluminum organic polymer capacitor provides most of the bulk capacitance.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than I_{LED}.

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of 0.6V and 0.85V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the steady-state condition in the form of capacitor voltages, mainly the output-filter-capacitor voltage and the compensation-capacitor voltage.

The switching converter small-signal-transfer function has a right-half plane (RHP) zero in the boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90-degree phase lag, which is difficult to compensate.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated for boost configuration as shown in Equation 23.

Equation 23:

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2 \times \pi \times L \times I_{LED}}$$

For the SEPIC and coupled-inductor configurations, see Equation 24.

Equation 24:

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2 \times \pi \times L \times I_{LED} \times D_{MAX}}$$

The standard way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}) that is calculated for the boost configuration, as shown in Equation 25.

Equation 25:

$$f_{P1} = \frac{I_{LED}}{\pi \times V_{LED} \times C_{OUT}}$$

For SEPIC and coupled-inductor use Equation 26.

Equation 26:

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{\pi \times V_{LED} \times C_{OUT}}$$

Compensation components, R_{COMP} and C_{COMP}, perform two functions. C_{COMP} introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain. R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at f_{P1} to provide a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP}, needed to fix the total loop gain at f_{P1} so that the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency, is calculated as shown in Equation 27.

Equation 27 (for boost configuration):

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times \left(1 - D_{MAX}\right)}$$

Equation 28 (for SEPIC and coupled-inductor buck-boost configurations):

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP} \times D_{MAX}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times \left(1 - D_{MAX}\right)}$$

where:

- R_{COMP} = Compensation resistor in ohms,
- A_{OVP} = BSTMON resistor-divider gain (a value << 1),
- R_{CS} = Current-sense resistor in ohms, and
- GM_{COMP} = Transconductance of the error amplifier (700µS).

The value of C_{COMP} is calculated as shown in Equation 29.

Equation 29:

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{Z1} \times R_{COMP}}$$

where f_{Z1} is the compensation zero placed at 1/5 the crossover frequency, which is, in turn, set at 1/5 the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency could fall below the 0dB crossover frequency. An additional pole may be required to cancel out this pole placed at the same frequency. This can be added by connecting

a capacitor from the COMP pin directly to GND with a value shown in Equation 30.

Equation 30:

$$GM_{COMP} \times R_{ESR} \times C_{OUT}$$

where R_{ESR} is the capacitor ESR value and C_{OUT} is the output-capacitor value.

External Disconnect-MOSFET Selection

An external pMOSFET can be used to disconnect the boost output from the battery in the event of an output overload or short condition. This protection is not necessary In the case of the SEPIC or buck-boost, so there is no need for the pMOSFET. Connect the PGATE pin to ground in the case of the SEPIC and buck-boost. If it is necessary to have an output short protection for the boost even at power-up, then the current through the pMOSFET (see the *Typical Application Circuits*) has to be sensed. Once the current-sense voltage exceeds a certain threshold, it should limit the input current to the programmed threshold. This threshold should be set at a sufficiently high level so it never trips at startup or under normal operating conditions. Check the safe operating area (SOA) of the pMOSFET so the current-limit trip threshold and voltage on the MOSFET do not exceed the limits of the SOA curve of the pMOSFET at the highest operating temperature.

V_{OUT} to OUT_ Bleed Resistors

The OUT_ pins have a leakage specification of 12µA (max) in cases where all OUT_ pins are shorted to 48V (see $I_{OUTLEAK}$ in *Electrical Characteristics*). This leakage current is dependent on the OUT_ voltage and is higher at higher voltages. Therefore, in cases where large numbers of LEDs are connected in series, a 100kΩ (or larger) bleed resistor can be placed in parallel with the LED string to prevent the OUT_ leakage current from very dimly illuminating the LEDs, even when the DIM signal is low (see resistors R8–R11 in *Typical Application Circuits*).

Thermal Considerations

The on-chip power dissipation of the MAX20446C comprises two main factors:

- Current-sink power loss: $1.1V \times I_{LED}$
- Device operating current power loss: $V_{IN} \times 15mA$.

Calculate the total power dissipation by adding the two values calculated above. The junction temperature at the maximum ambient temperature can then be calculated using Equation 31.

Equation 31:

$$T_J = T_A + P_{TOT} \times \theta_{JA}$$

where T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the package (36°C/W on a four-layer board). Ensure that the junction temperature does not exceed 150°C.

The general formula for total power dissipation is shown in Equation 32.

Equation 32:

$$P_{TOT} = V_{OUT(MAX)} \times I_{LED} + V_{IN} \times I_Q$$

As an example, consider an application with an operating voltage of 14V and a total output current of 600mA. The total power dissipation is shown in Equation 33.

Equation 33:

$$P_{TOT} = 1.1 \times 0.6 + 14 \times 0.015 = 0.87W$$

The maximum junction temperature at an ambient temperature of 85°C is shown in Equation 34.

Equation 34:

$$T_J = 85 + 0.87 \times 36 = 116\ ^\circ C$$

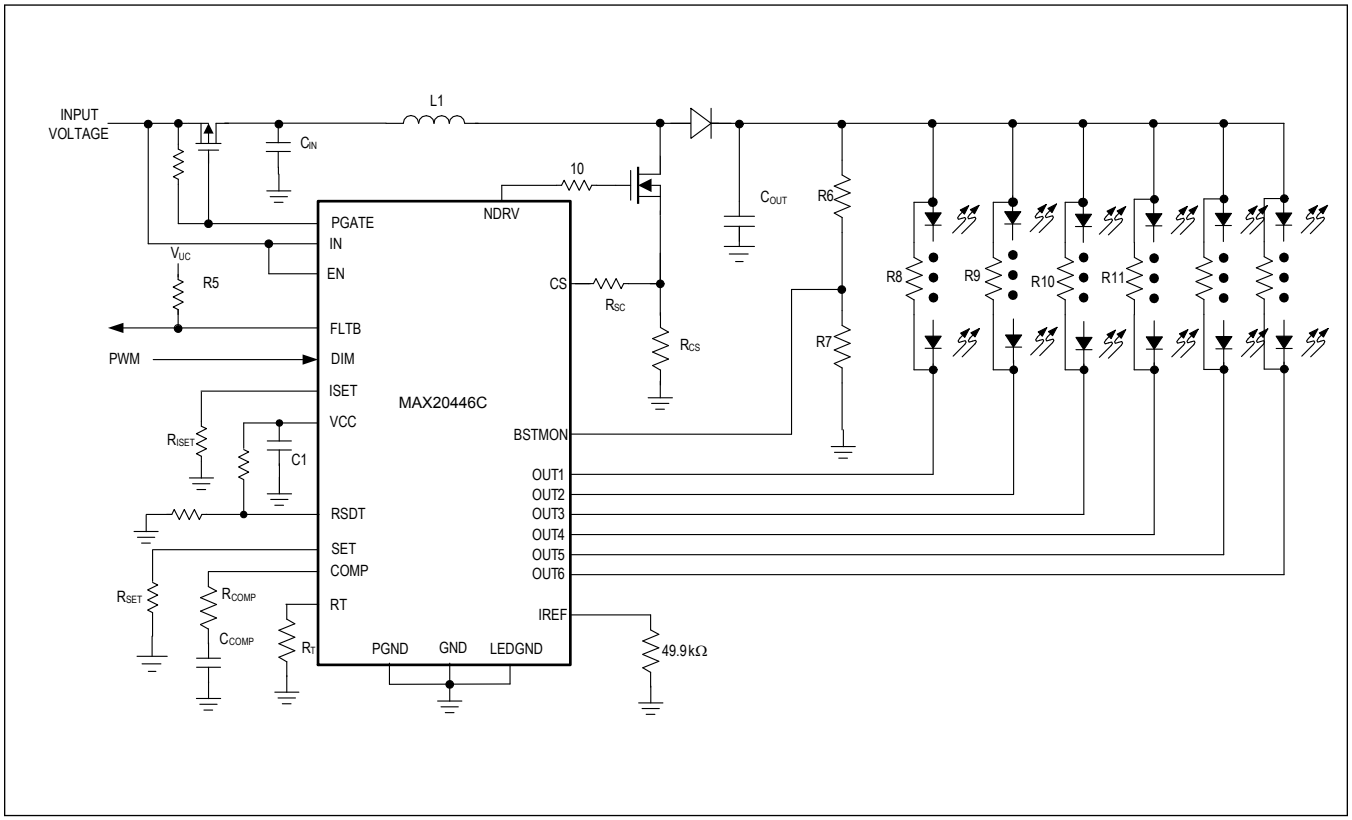
PCB Layout Considerations

LED driver circuits based on the MAX20446C use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure correct operation. The switching-converter portion of the circuit has nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit. Follow the guidelines below to reduce noise as much as possible:

- Connect the bypass capacitor on V_{CC} as close as possible to the device and connect the capacitor ground to the analog ground plane using vias close to the capacitor terminal. Connect the GND of the device to the analog ground plane using a via close to GND. Lay the analog ground plane on the inner layer, preferably next to the top layer. Use the analog ground plane to cover the entire area under critical signal components for the power converter.
- Have a power-ground plane for the switching-converter power circuit under the power components (i.e., input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power-ground plane closest to PGND. Connect all other ground connections to the power ground plane using vias close to the terminals.
- There are two loops in the power circuit that carry high-frequency switching currents. One loop is when the MOSFET is on (from the input filter capacitor positive terminal, through the inductor, the internal MOSFET and the current-sense resistor, to the input capacitor negative terminal). The other loop is when the MOSFET is off (from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power ground plane for the switching currents on the top layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.
- Connect the power-ground plane for the constant-current LED driver portion of the circuit to LEDGND as close as possible to the device. Connect GND to PGND at the same point.
- Add a small bypass capacitor (22pF to 47pF) to the BSTMON input. Place the capacitor as close as possible to the pin to suppress high-frequency noise.
- Boost output voltage for the LED strings should be taken directly from the output capacitors and not from the boost diode anode.
- Input and output capacitors need good grounding with wide traces and multiple vias to the ground plane.
- Refer to the MAX20446C evaluation kit (EV kit) data sheet for an example layout.

Typical Application Circuits

MAX20446C Applications Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PHASE SHIFTING
MAX20446CATGA/V+T	-40 to +125°C	24 TQFN	On
MAX20446CATGB/V+T*	-40 to +125°C	24 TQFN	Off

/V denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	03/21	Initial release	—

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