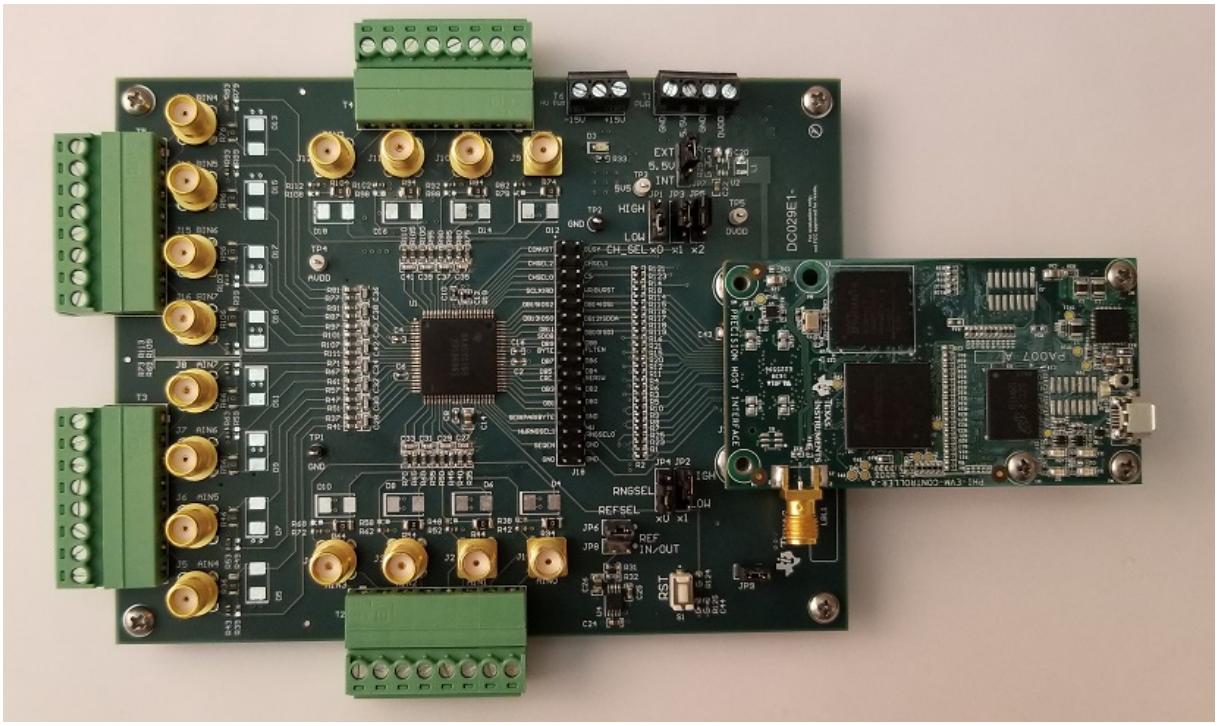
ADS8686SEVM-PDK Evaluation Module



This user's guide describes the characteristics, operation, and use of the ADS8686S evaluation module (EVM) performance demonstration kit (PDK). The ADS8686S is a 16-channel, integrated front-end data acquisition (DAQ) system based on a dual, simultaneous-sampling, 16-bit successive approximation (SAR) analog-to-digital converter (ADC). Each input channel on the device supports true bipolar input ranges of ±10 V, ±5 V, or ±2.5 V with single-supply operation. The device includes an analog front-end offering a 1-MΩ, constant resistive input impedance. The ADS8686SEVM supports all the mentioned features and provides provisions for an external reference, user-selectable oversampling ratio, and features 16 input channels. The EVM-PDK eases the evaluation of the ADS8686S device and any devices derived from the ADS8686X family with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials using the ADS8686S device as an example throughout the document. Throughout this document, the terms *EVM-PDK* and *ADS8686SEVM* are synonymous with the *ADS8686SEVM-PDK*.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS8686S	SBAS905
REF5025	SBOS410
TPS7A4700	SBVS204
OPA192	SBOS620
INA149	SBOS579

Contents

List of Figures

List of Tables

Trademarks

1 Overview

The ADS8686SEVM-PDK is a platform for evaluating the performance of the ADS8686X family. The EVM-PDK comes with the ADS8686S SAR ADC, a 16-channel, 16-bit, ±10-V, ±5-V, or ±2.5-V input range, simultaneous-sampling ADC device. The evaluation kit includes the ADS8686SEVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The ADS8686SEVM board includes the ADS8686S SAR ADC and all peripheral analog circuits and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8686SEVM
- Supplies power to the digital circuitry on the ADS8686SEVM board

Along with the ADS8686SEVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS8686SEVM-PDK Features

The ADS8686SEVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8686X family of SAR ADC devices
- USB digital power to enable digital communication
- The PHI controller that provides a convenient communication interface to the ADS8686S ADC over a USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for Windows 7®,Windows 8®, and Windows 10® 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS8686SEVM Features

The ADS8686SEVM includes the following features:

- Onboard SMB and terminal block connectors and RC input filters
- Jumper-selectable onboard precision 2.5-V voltage reference or the ADS8686X family devices internal reference
- Jumper-selectable ±10-V, ±5-V, or ±2.5-V range
- Jumper-selectable channel sequence selection
- Onboard, ultralow noise, low-dropout (LDO) regulator for excellent 5.0-V, single-supply regulation of the ADC and onboard voltage reference

2 EVM Analog Interface

The ADS8686SEVM is designed for easy interfacing to analog sources. The four Phoenix Contact™ 8-terminal headers paired with a respective screw connection tension sleeve, T2 thru T5, provides convenient and interchangeable access points to all input channels (AIN_0A to AIN_7A and AIN_0B to AIN_7B) of the device. In addition, the 16 SMB connectors footprints, J-1 to J-16, provide high-quality connections to channels AIN_0A to AIN_7A and AIN_0B to AIN_7B. Figure 1 shows the ADS8686SEVM analog input connections and input RC filters for channels AIN_0A to AIN_7A. Table 1 lists the analog interface connections for header JP1 and Table 2 lists the analog interface connections for the SMB connectors.

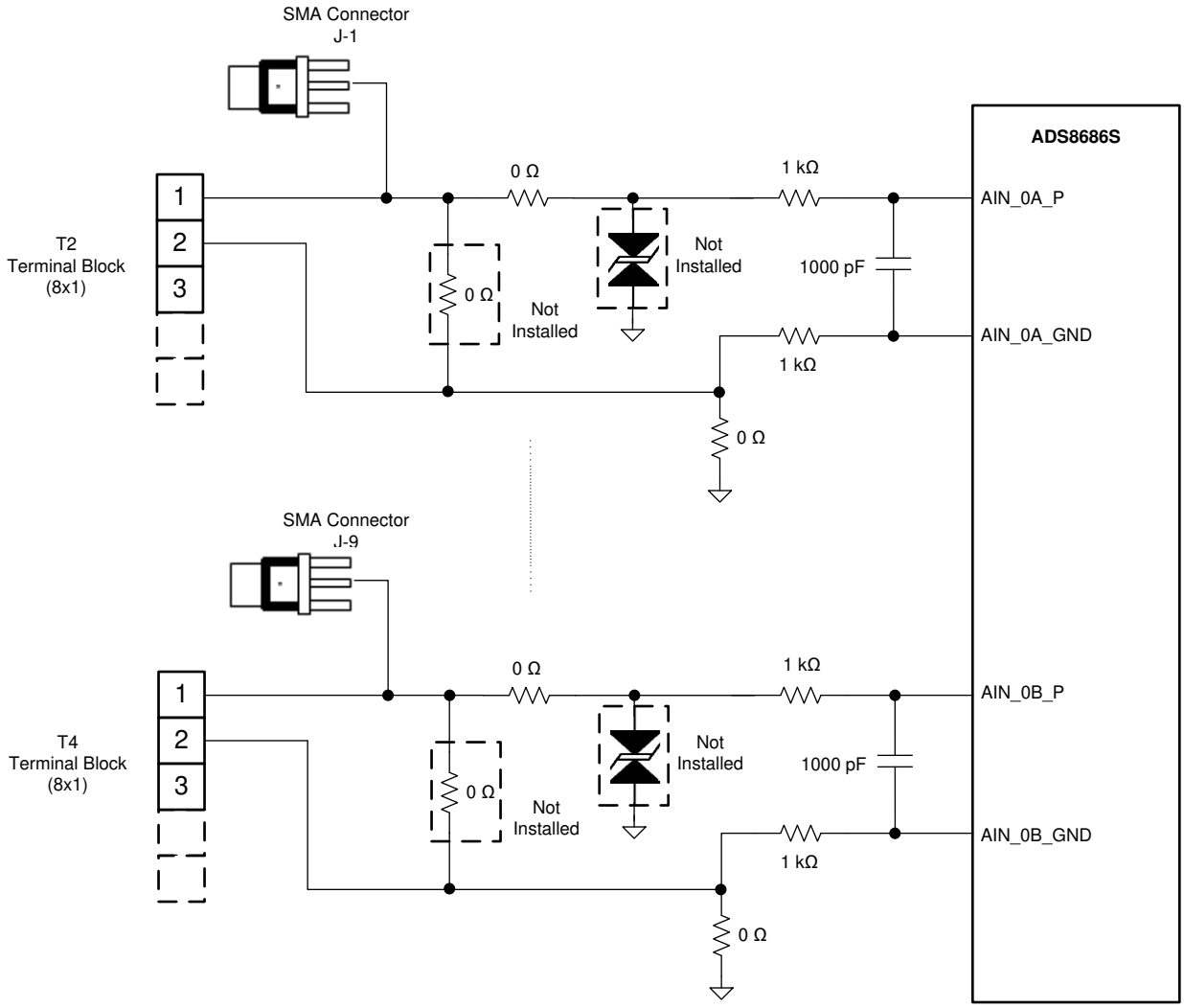


Figure 1. ADS8686SEVM Analog Input Connections for Channels

Table 1. Terminal Block Analog Interface Connections

Terminal # - Pin Number	Signal	Description
T2/3 - 1	AIN_0/7A_P	Positive analog input for channel AIN0A OR positive analog input for channel AIN7A
T2/3 - 2	AIN_0/7A_GND	Negative analog input for channel AIN0A OR negative analog input for channel AIN7A
T2/3 - 3	AIN_1/6A_P	Positive analog input for channel AIN1A OR positive analog input for channel AIN6A
T2/3 - 4	AIN_1/6A_GND	Negative analog input for channel AIN1A OR negative analog input for channel AIN6A
T2/3 - 5	AIN_2/5A_P	Positive analog input for channel AIN2A OR positive analog input for channel AIN5A
T2/3 - 6	AIN_2/5A_GND	Negative analog input for channel AIN2A OR negative analog input for channel AIN5A
T2/3 -7	AIN_3/4A_P	Positive analog input for channel AIN3A OR positive analog input for channel AIN4A
T2/3 -8	AIN_3/4A_GND	Negative analog input for channel AIN3A OR negative analog input for channel AIN4A
T4/5 - 1	AIN_0/7B_P	Positive analog input for channel AIN0B OR positive analog input for channel AIN7B
T4/5 - 2	AIN_0/7B_GND	Negative analog input for channel AIN0B OR negative analog input for channel AIN7B
T4/5 - 3	AIN_1/6B_P	Positive analog input for channel AIN1B OR positive analog input for channel AIN6B
T4/5 - 4	AIN_1/6B_GND	Negative analog input for channel AIN1B OR negative analog input for channel AIN6B
T4/5 - 5	AIN_2/5B_P	Positive analog input for channel AIN2B OR positive analog input for channel AIN5B
T4/5 - 6	AIN_2/5B_GND	Negative analog input for channel AIN2B OR negative analog input for channel AIN5B
T4/5 -7	AIN_3/4B_P	Positive analog input for channel AIN3B OR positive analog input for channel AIN4B
T4/5 -8	AIN_3/4B_GND	Negative analog input for channel AIN3B OR negative analog input for channel AIN4B

Table 2. SMA Analog Interface ADC-A Connections

SMA Connector	Signal	Description
J-1	AIN_0A	Analog input for channel AIN_0A
J-2	AIN_1A	Analog input for channel AIN_1A
J-3	AIN_2A	Analog input for channel AIN_2A
J-4	AIN_3A	Analog input for channel AIN_3A
J-5	AIN_4A	Analog input for channel AIN_4A
J-6	AIN_5A	Analog input for channel AIN_5A
J-7	AIN_6A	Analog input for channel AIN_6A
J-8	AIN_7A	Analog input for channel AIN_7A

Table 3. SMA Analog Interface ADC-B Connections

SMA Connector	Signal	Description
J-9	AIN_0B	Analog input for channel AIN_0B
J-10	AIN_1B	Analog input for channel AIN_1B
J-11	AIN_2B	Analog input for channel AIN_2B
J-12	AIN_3B	Analog input for channel AIN_3B
J-13	AIN_4B	Analog input for channel AIN_4B
J-14	AIN_5B	Analog input for channel AIN_5B
J-15	AIN_6B	Analog input for channel AIN_6B
J-16	AIN_7B	Analog input for channel AIN_7B

2.1 ADS8686S Internal Reference and EVM Onboard Reference

The ADS8686S device incorporates an internal 2.5-V reference. Alternatively, the user can select the onboard 2.5-V reference, REF5025 (U4). The reference voltage source is determined by setting REFSEL (pin 35) of the ADS8686S device. By default, the evaluation module is set up with the ADS8686S internal reference source, with a shunt jumper installed on JP6 (REFSEL). If the onboard REF5025 2.5-V reference is desired, the shunt jumper must be removed from JP6 and placed on JP8 (REFIN/OUT). For more information, see Section 5.1. The output of the REF5025 is filtered through a passive RC filter and connected to the REFINOUT pin (pin 33) of the ADS8686S using jumper JP8 (REFIN/OUT). Figure 2 shows a schematic for the reference circuit.

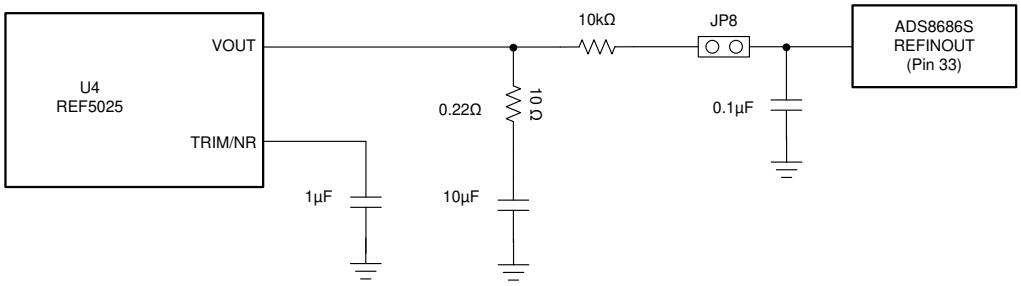


Figure 2. REF5025 2.5-V External Reference Source

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8686S ADC (over a single or dual SDO serial interface or parallel interface) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS8686SEVM-PDK platform. The EEPROM is initially programmed to communicate with the ADS8686S, but can be reprogrammed for any of the supported devices in the ADS8686X device family through their respective GUI software. See Section 5.2 for more information and instructions. After the hardware is initialized, the EEPROM is no longer used.

3.1 ADS8686S Digital Interface

The ADS8686SEVM-PDK supports parallel, parallel byte, and serial digital interface as detailed in the ADS8686S data sheet. The PHI controller is configured to operate at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC. The digital interface configuration can be easily selected by navigating within the ADS8686SEVM GUI to *Device Configuration* tab. For more information, see Section 6.1.

Socket strip connector J17 provides the digital I/O connections between the ADS8686SEVM board and the PHI controller. Table 4 summarizes the pin outs for connector J17.

Table 4. Digital I/O Connections for Connector J17

Pin Number	Signal	Description
J17.6, J17.8, J17.10	DB15/OS2, DB14/OS1, DB13/OS0	Parallel data output connections OR oversampling mode control pins
J17.12, J17.14,	DB12/SDOA, DB11/SDOB	Parallel data output connections OR serial data output connections
J17.16,	DB10/SDI	Parallel data output connections OR serial data input connections
J17.18	DB9/BYTESEL	Parallel data output connections OR enable parallel byte interface
J17.20	DB8/FLTEN	Parallel data output connections
J17.22,J17.24	DB7, DB6	Parallel data output connections
J17.26	DB5/CRCEN	Parallel data output connections OR enable CRC word
J17.28	DB4/SER1W	Parallel data output connections OR serial data output wire select

Table 4. Digital I/O Connections for Connector J17 (continued)

Pin Number	Signal	Description
J17.30	DB3	Parallel data output connections
J17.32, J17.34	CSn	$\overline{CS}$ select, active low
J17.36	SCLK/RD	Clock input pin in serial interface mode OR active-low ready input pin in parallel and parallel byte interface
J17.38, J17.40, J17.42	DB2, DB1, DB0	Parallel data output connections
J17.44	CONVST	Active high logic input to control start of conversion
J17.46, J17.48	HW_RNGSEL1,0	Pins used to select input range of device (±10 V, ±5 V, or ±2.5 V)
J17.50	DVDD	3.3-V digital supply from the PHI controller board
J17.56, J17.58	I^2C Bus	I^2C bus; used only to read the EEPROM (U5) in the EVM board
J17.3, J17.60	GND	Ground connections
J1721	WR/BURST	Write register configuration in parallel and parallel byte modes OR enable burst mode
J17.23	BUSY	Active high digital output indicating ongoing conversion
J17.31	SEQEN	Active high digital input enabling channel sequencer
J17.33	RESET	Active low logic input to reset the device
J17.39	SER/BYTE/PAR	Logic input pin to select between serial, parallel byte, or parallel interface mode
J17.41, J17.43, J17.45	CHSEL0,1,2	Logic input pin to select channel for hardware mode sequencer
J17.59	ID_POWER	Power supply used only to power the EEPROM (U3) in the EVM board

4 Power Supplies

4.1 Device Power Supplies

The ADS8686S ADC analog supply (AVDD) is provided by a low-noise linear regulator (TPS7A4700). The regulator uses a 5.5-V external supply provided through terminal block T1 (PWR) connected in position 3 (5.5V), and position 4 (GND). This (TBD this what?) is connected to JP7 set to position EXT (pins 2 and 3). The switching regulator (U2) is not populated, and the EVM does not support setting JP7 in position INT (pins 1 and 2). The 3.3-V supply to the digital supply of the ADS8686S is provided directly by an LDO on the PHI controller. The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper filled areas where possible between bypass capacitors and their loads to minimize inductance along the load current path.

CAUTION

When using the ADS8686SEVM in conjunction with the PHI controller, install a shunt between JP7 pins 2-3 as shown in Figure 4 The PHI controller supplies the DVDD power supply. Do not use the JP7 internal setting or the device can be damaged.

CAUTION

When using the ADS8686SEVM as a stand-alone board, install a shunt between JP7 (pins 2 and 3) and connect the analog supply (AVDD) on the terminal block T1 (position 3 or 4). For the digital supply (DVDD), remove R28 and supply DVDD on the terminal block T1 (position 1 or 2). Make sure that the AVDD voltage is in the range between 5.5 V to 6 V, and that DVDD is in the range of 2.3 V < DVDD < AVDD for proper device operation. Do not exceed the absolute maximum ratings for the ADS8686S device, or damage may occur.

4.2 High-Voltage Power Supplies

As shown in Figure 3, the ADS8686SEVM is equipped with two input driving amplifiers for two ADS8686S analog inputs. The device input AIN_0B can be driven by U6, the OPA192 (a precision rail-to-rail operational amplifier) in a buffer configuration. Input AIN_B1 can be driven by a difference amplifier, U7 (INA149). Each of these amplifiers require positive and negative power rails over the expected maximum and minimum input levels, and the recommended supply is ±15 V. Connect an external power supply to terminal block T6 (HV PWR) to provide the high-voltage power supplies. See the respective device data sheet for more information.

By default, each of the amplifiers are bypassed. To include the OPA192 in the input driving circuit to channel AIN_0B, remove the 0-Ω resister, R127, and populate R129 and R128 with 0-Ω resisters. The input can be connected through either terminal block T4 (position 3 or4) or by the BNC connector J10. To include the INA149 in the input driving circuit to channel AIN_1B, remove the 0-Ω resistors, R130 and R133, and populate R134, R135, and R131. Inputs can be connected through either terminal block T4 (position 5 or 6) or by the BNC connector J11. To use a different value other than ground for input AIN_1BGND, use terminal block T4, position 6.

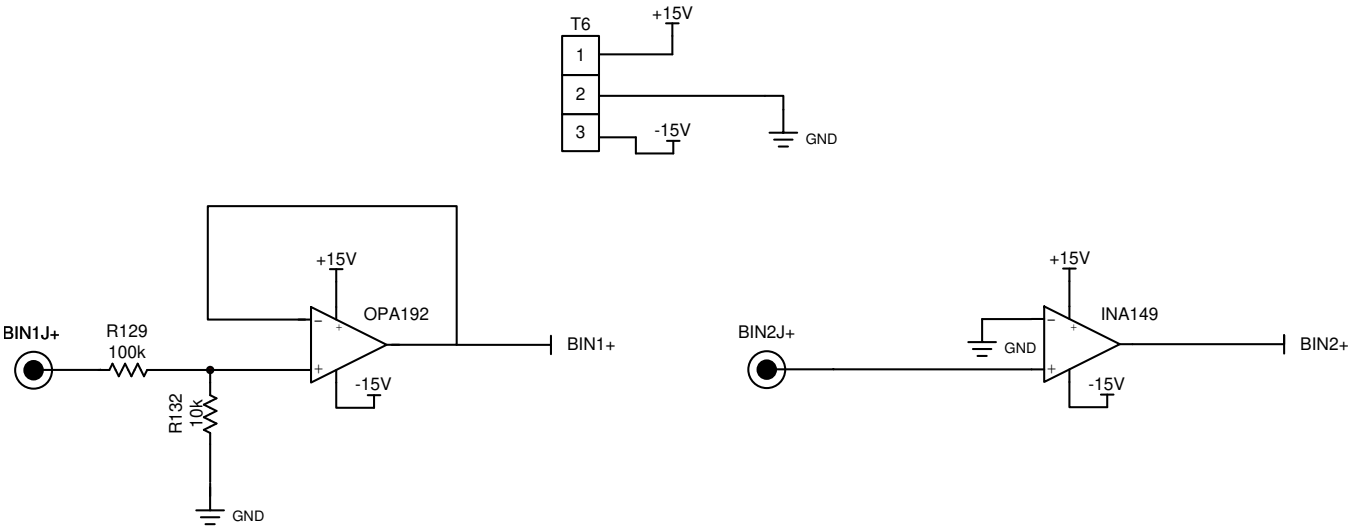


Figure 3. High-Voltage Power Supply for Amplifiers

NOTE: The high-voltage power supplies connected to terminal block T6 only provide power to U6 and U7, the input driving amplifiers. The high-voltage power supplies are not connected to any other device on the board.

CAUTION

Terminal T6 (HV PWR) on the ADS8686SEVM is intended for high-voltage supplies and does not have a protection scheme or regulation circuitry onboard. When connecting an external power supply to T6 use a clean and precise supply, otherwise damage can occur to the driving amplifiers U6 and U7.

5 Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS8686SEVM-PDK.

5.1 Default Jumper Settings

Install a shunt at JP6 to select the internal reference. Install a shunt between JP7 (pins 2 and 3) as shown in Figure 4 to connect the onboard regulated AVDD 5.0-V supply. Figure 4 details the default jumper settings. Table 5 explains the configuration for these jumpers. When the EVM is paired with the PHI board, the jumper selections on JP1 thru JP5 have no effect in either hardware or software mode. The GUI provides user-selectable options to control these settings and overrides the jumper selection. When the EVM is used standalone, the jumper settings take effect in the device settings.

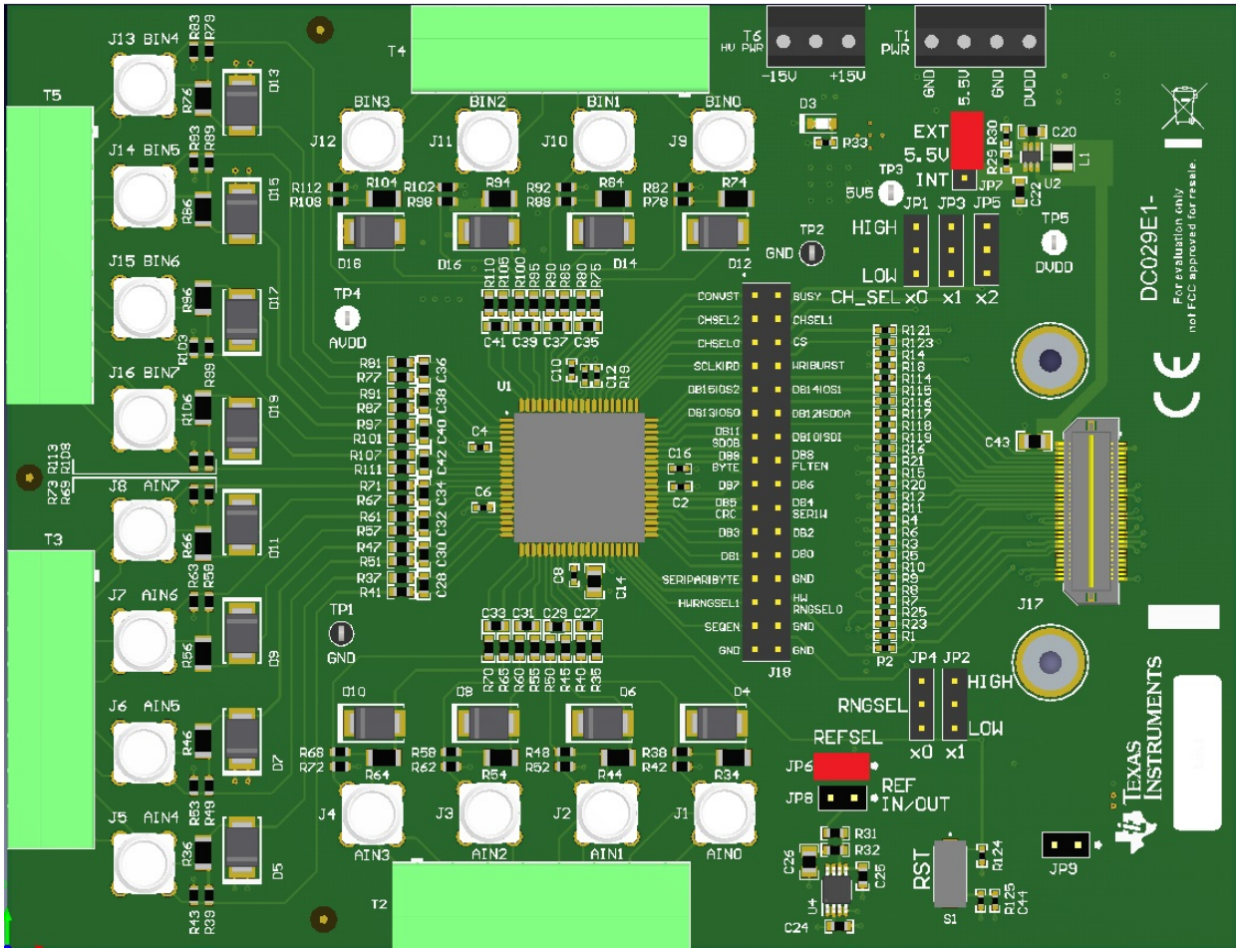


Figure 4. ADS8686SEVM Default Jumper Settings

Table 5. Default Jumper Configuration

Jumper	Function	Default Position	Description
JP1, JP3, JP5	CHSEL0, CHSEL1, CHSEL2	Open	1-2 logic high, 2-3 logic low. Programs the channel sequencer.
JP2, JP4	HW_RNGSEL0, HW_RNGSEL1	Open	1-2 logic high, 2-3 logic low. Selects the analog input range.
JP6	REFSEL	Closed	Open selects the external reference; closed selects the internal reference
JP7	AVDD Ext	Closed between pins 2 and 3	2-3 external source regulated with the onboard LDO to the AVDD 5.0-V supply

Table 5. Default Jumper Configuration (continued)

Jumper	Function	Default Position	Description
JP8	REFIN/OUT	Open	Open when using the internal reference; closed connects the external onboard reference

5.2 EVM Graphical User Interface (GUI) Software Installation

NOTE: Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

The following steps list the directions to install the software using the ADS8686S as an example. Download and install the ADS8686SEVM software GUI from he ADS8686SEVM-PDK product folder. Administrator privileges are required on the PC to install the EVM software.

Accept the license agreements and follow the on-screen instructions to complete the installation, as shown in Figure 5, after downloading and starting the GUI installer.

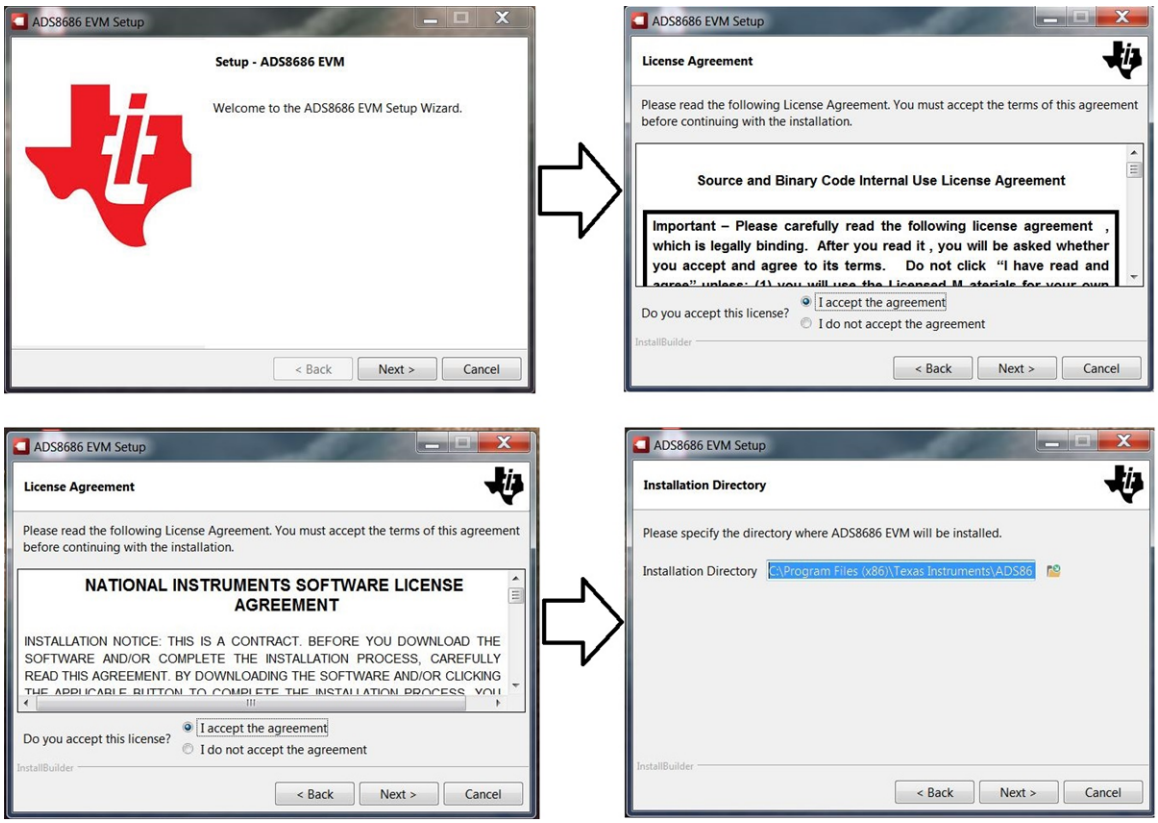


Figure 5. Software Installation Prompts

A prompt with a *Device Driver Installation* appears on the screen, as shown in Figure 6, as part of the ADS8686S EVM GUI installation. Click *Next* to proceed.

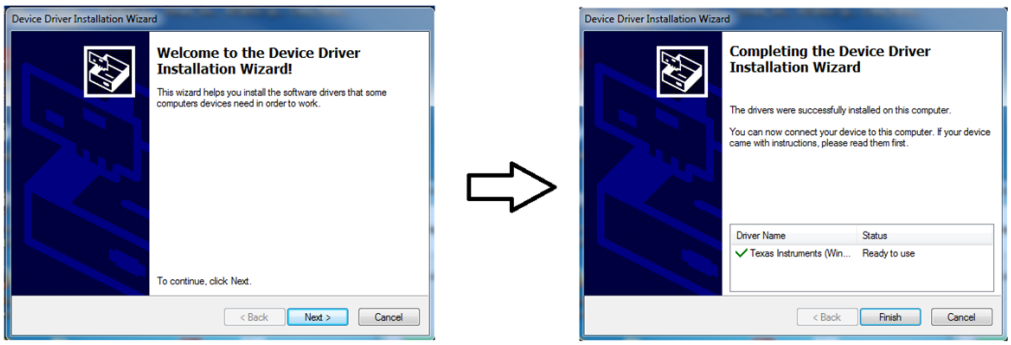


Figure 6. ADS8686S Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

TheADS8686SEVM-PDK requires the LabVIEW™ Run-Time Engine. A prompt appears for the installation of this software, as shown in Figure 7, if not already installed.

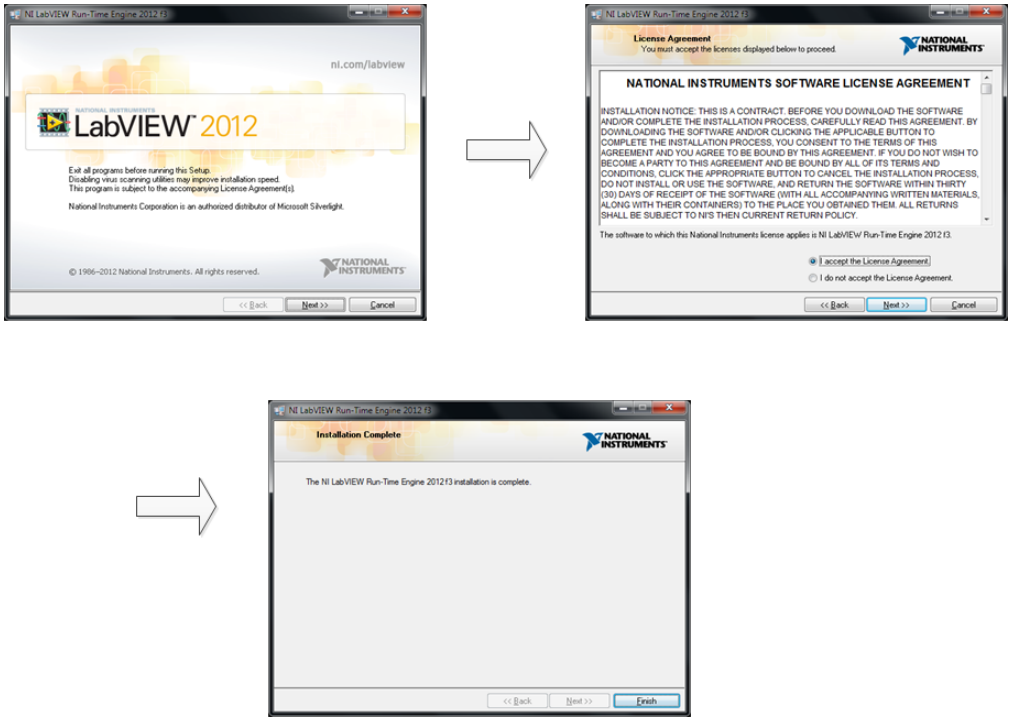


Figure 7. LabVIEW Run-Time Engine Installation

The installation is now complete. The prompts shown in Figure 8 confirm that the software is installed.

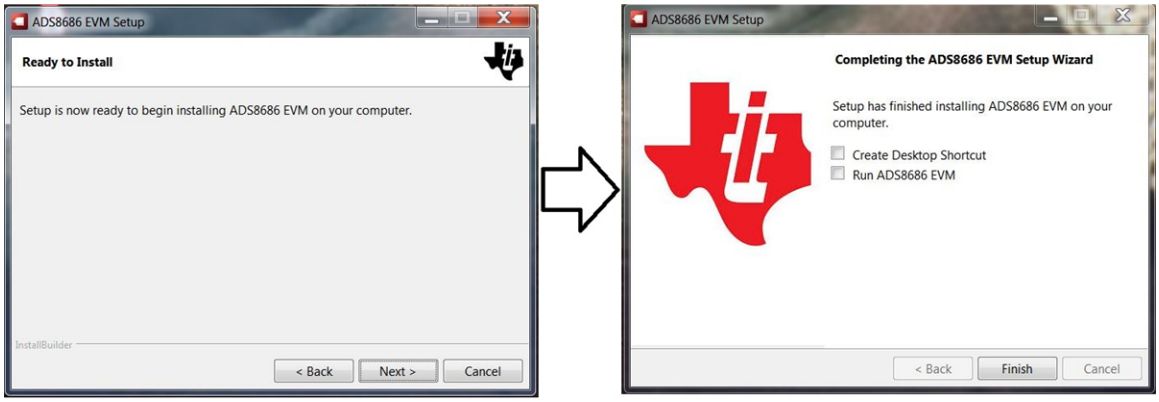


Figure 8. Software Installation Complete Prompts

Verify that the contents of *C:\Program Files (x86)\Texas Instruments\ADS8686 EVM* is as shown in Figure 9 after installation.

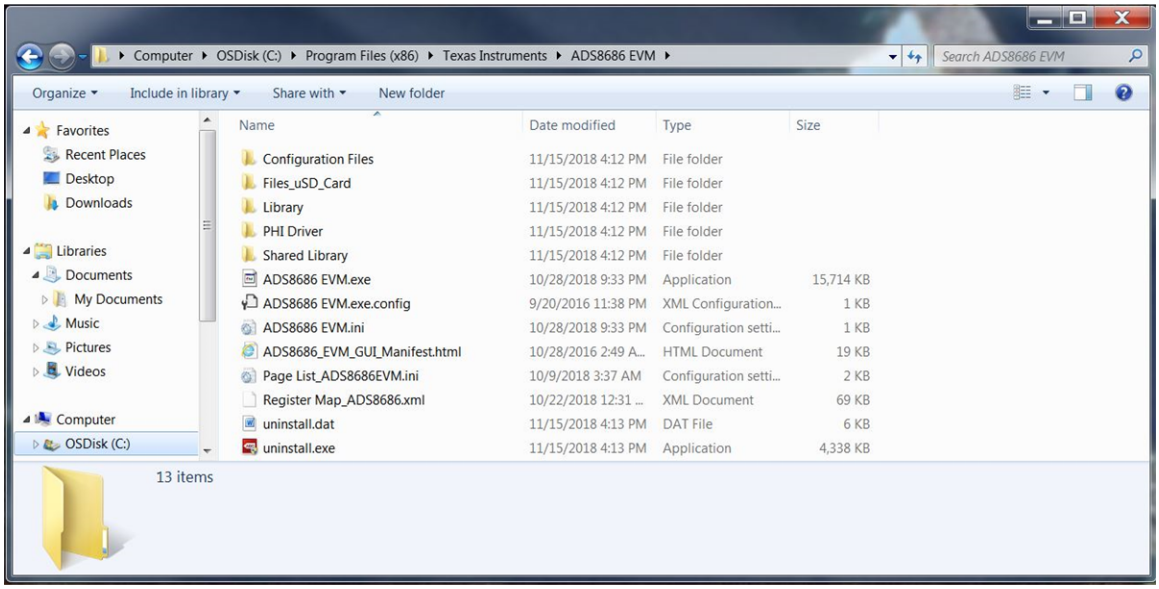


Figure 9. ADS8686S EVM Folder Post-Installation

6 Operation

The following instructions are a step-by-step guide to connecting the ADS8686S to the computer and evaluating the performance of the ADS8686S:

1. Connect the ADS8686SEVM to the PHI. Install the two screws as indicated in Figure 10.
2. Use the USB cable provided to connect the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI starts blinking to indicate that the PHI is booted up and communicating with the PC. Figure 10 shows the resulting LED indicators.

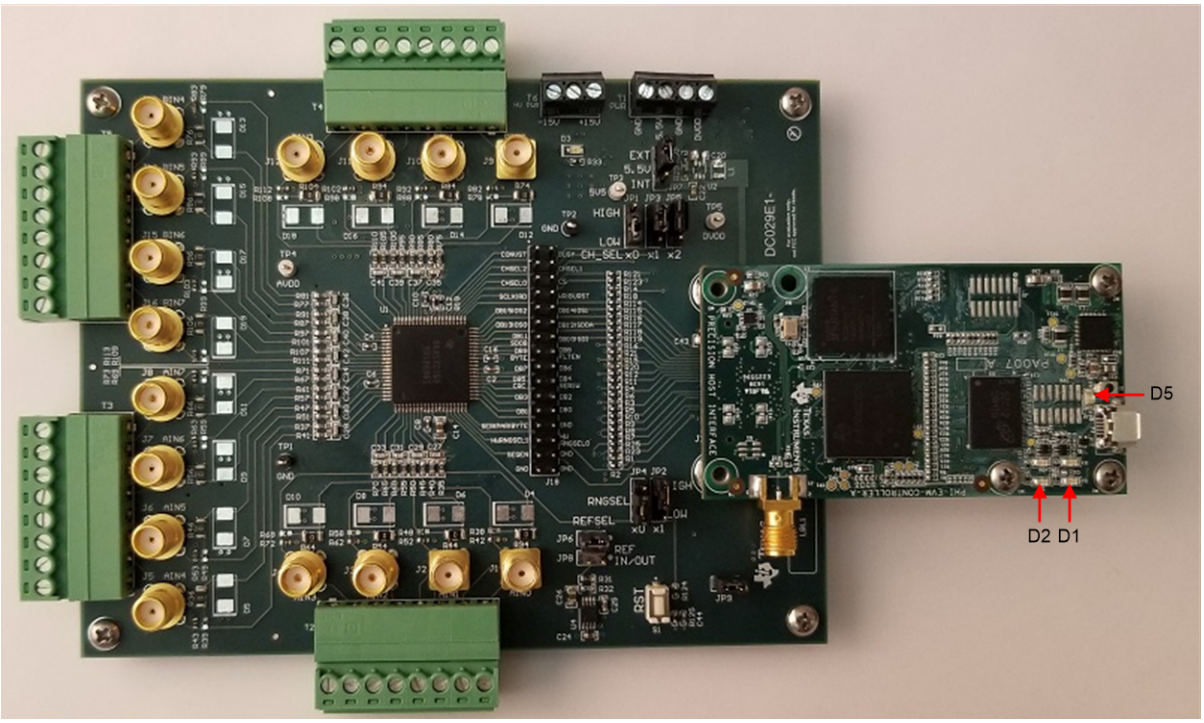


Figure 10. ADS8686SEVM-PDK Hardware Setup and LED Indicators

3. As shown in Figure 11, double click the *ADS8686EVM.exe* file to launch the EVM GUI.

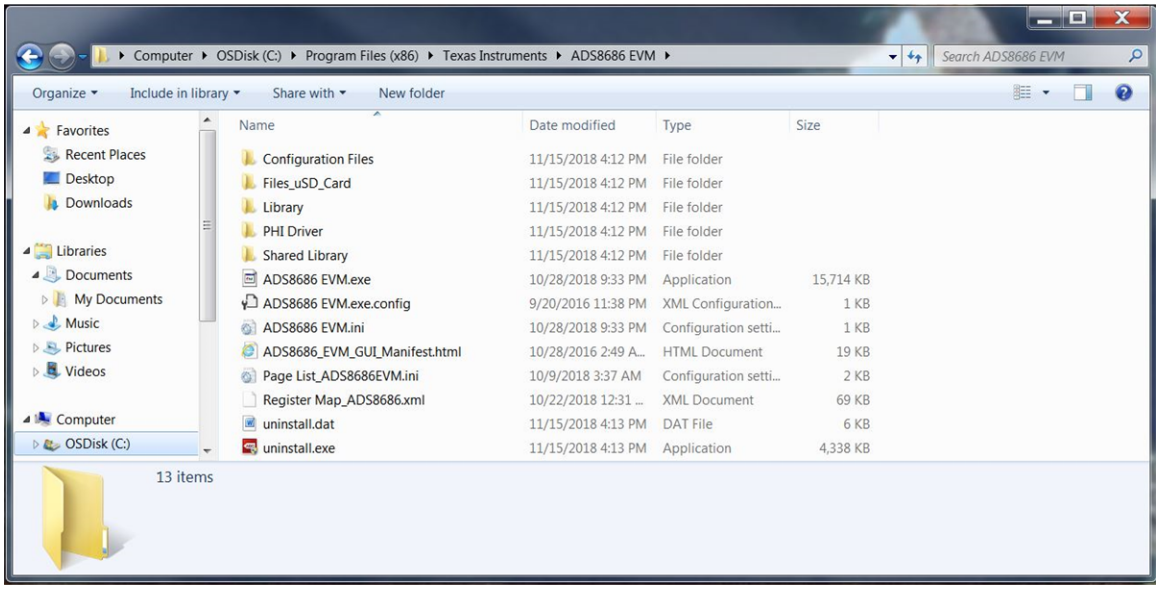


Figure 11. Launch the ADS8686SEVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the voltage levels and timing configuration of the ADC digital interface, the EVM GUI provides high-level control over the ADS8686S interface modes and RD/SCLK clock frequency. In addition, the EVM GUI provides control to device configuration settings such as sampling rate and number of samples to be captured, as well as register mapping such as input range selection, oversampling setting, and channel sequence selection.

Figure 12 shows the *Interface Configuration* pane at the left, through which timing functions of the ADS8686S are exercised. These are global settings and persist across the different GUI *Pages* listed in the top left pane. The*SCLK Frequency (Hz)* and *Sampling Rate (sps)* can be selected on this pane, depending on the selected interface and OSR settings. Enter the targeted values for these two parameters, and the GUI considers the timing constraints of the selected interface and computes the best values that can be achieved. Enter a *Target* value in the *SCLK Frequency (Hz)* field, and the GUI matches this frequency as closely as possible by changing the PHI PLL settings, and then displaying the *Achievable* frequency that may differ from the entered *Target* value. Similarly, adjust the ADC *Sampling Rate (sps)* by entering a *Target* value (Hz = sps). The *Achievable* ADC sampling rate can differ from the *Target* value, depending on the applied RD/SCLK frequency and selected Interface. The closest achievable match is then displayed. Therefore, this pane allows the various settings available on the ADS8686S to be tested in an iterative fashion until the best settings for the corresponding test scenario are achieved.

Displayed above this (TBD this what?) are the *Full Reset* and *Partial Reset* buttons. Each of these buttons initiates its respective reset type through software. A hardware reset can be initiated by pressing S1 RST on the EVM. When a master reset, either through software or hardware occurs the device resets to the default register settings. The GUI automatically generates a reset pulse when required to execute device configurations; there is no need to press the *Full Reset* button. At the bottom left, the *Current Device Mode* pane displays the operational mode the device is currently in, which also persists across the GUI tools and pages.

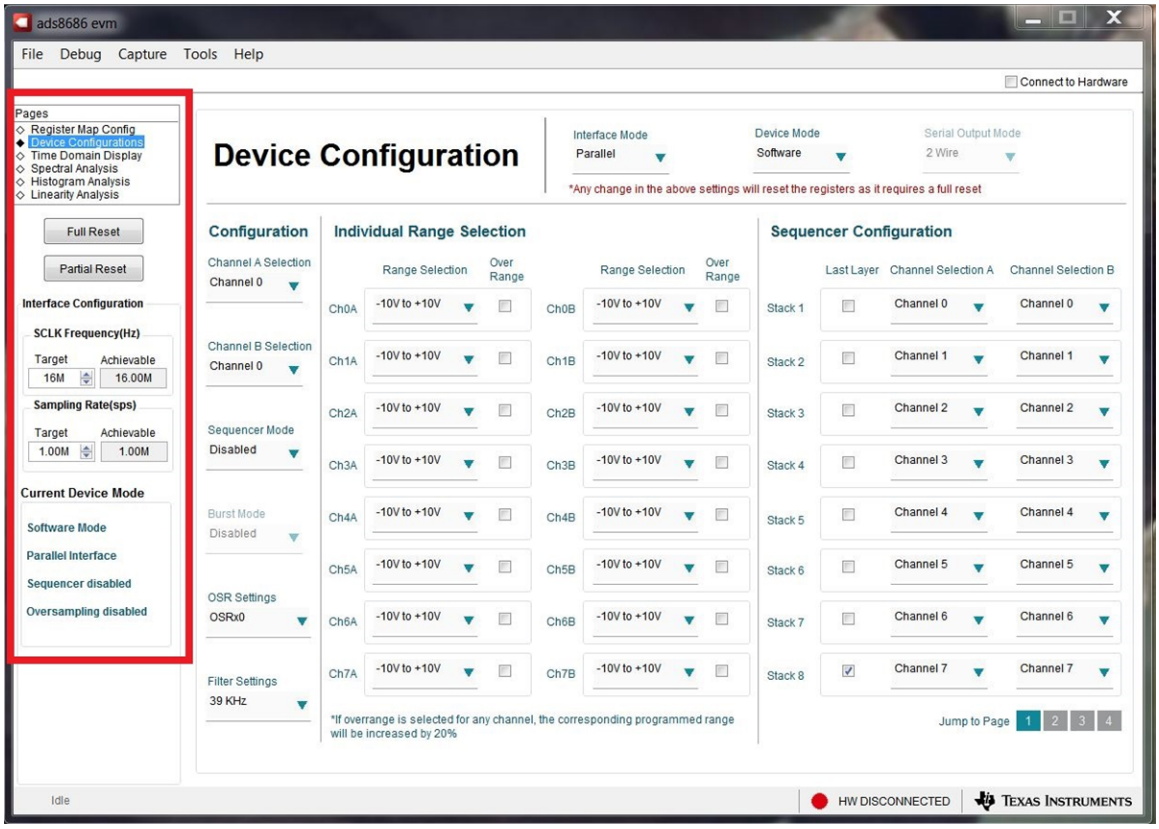


Figure 12. EVM GUI Global Input Parameters

6.2 Register Map Configurations

The *Register Map Config* page (Figure 13) provides access to the device register mapping. Within the page, the user registers listed can be easily changed through a drop down provided under the *Field View* on the right. When a register is selected, the options available are listed, when an option is selected, that option is reflected in the *Value* column. When a register configuration is made, that configuration persists through all GUI pages. See the device data sheet for more information on device registers.

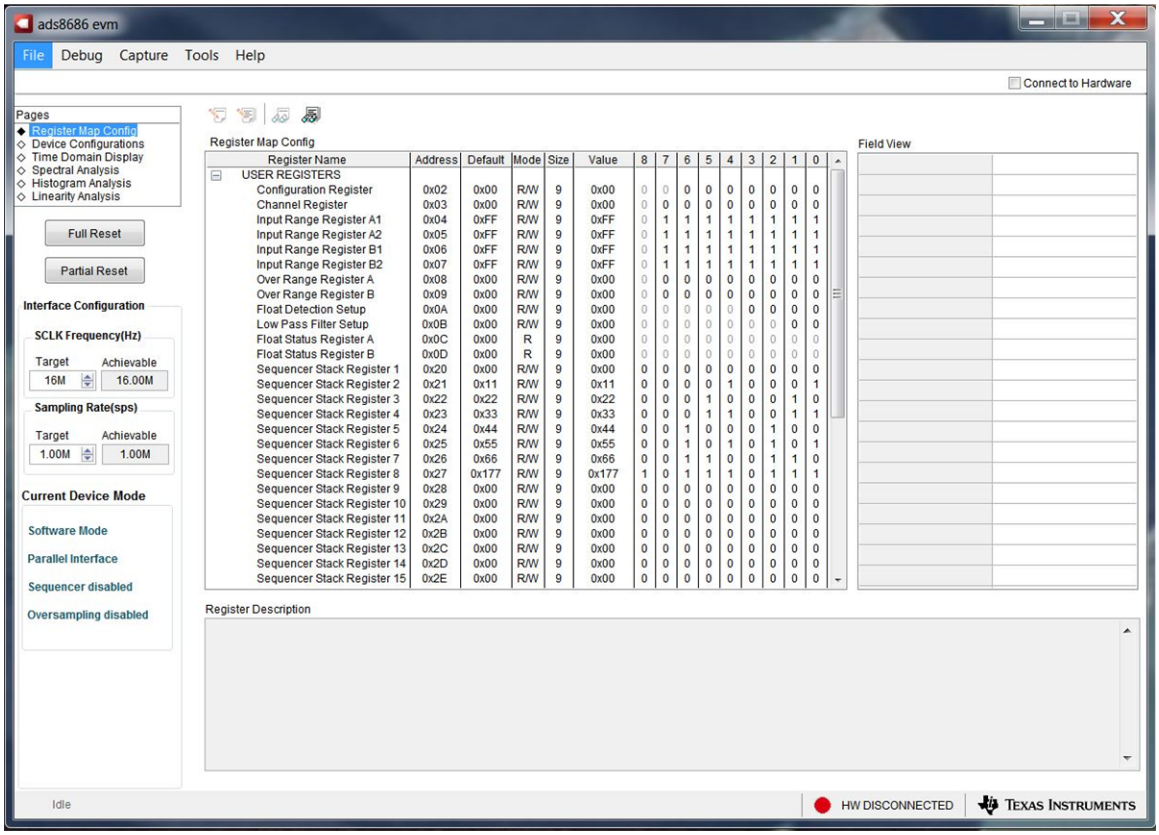


Figure 13. Register Map Configuration Display

6.3 Device Configuration

The device configuration page provides a user-friendly interface to the most common configuration options. When a setting is changed, that setting persists through all GUI pages and is also reflected in the *Current Device Mode* box if listed. When making a change that requires a reset pulse to the device, the GUI provides the pulse when the setting is changed; there is no need to press the *Full Reset* button.

At the top of the page are drop-down menu options for the *Interface Mode*, *Device Mode*, and *Serial Output Mode*. The *Interface Mode* field allows the choice of three interface options: serial, parallel, or parallel byte. Serial interface communication occurs through either single or dual serial output: DB12/SDOA and DB11/SDOB that can be selected in the *Serial Output Mode* field. Parallel interface communication occurs through the DB[15:0] parallel bus, parallel byte through the DB[7:0] parallel bus.

6.3.1 Software Mode

The page displays the setting options as shown in Figure 14 when in software mode. The setting are displayed in three sections, *Configuration*, *Individual Range Selections*, and *Sequencer Configuration*.

In the left-most section, *Configuration*, channel selection options for each ADC is provided. In software mode the device allows the ADC channels sampled not to correspond with each other (for example, channel AIN_0A can be sampled with channel AIN_2B). The device also supports sequencer mode that can be enabled in this section. When this mode is disabled, the *Burst Mode* option is grayed out because burst mode is only available with the *Sequencer Mode* option enabled. To use burst mode, first enable *Sequencer Mode*, then enable *Burst Mode*. The ADS8686S supports an oversampling mode of operation using an on-chip averaging digital filter, as explained in the device data sheet. The oversampling ratio (OSR) settings drop-down menu in this section provides selectable oversampling ratios of 2x, 4x, 8x, 16x, 32x, 64x, and 128x. The *Filter Settings* drop down provides a drop-down field to select the cutoff frequency of the internal second-order, low-pass filter: 15 kHz, 39 kHz, or 300 kHz.

The middle section, *Individual Range Selection*, is used to select the input range of each input channel of the device: ±10 V, ±5 V, or ±2.5 V. Each channel can also support an input range increase of 20% of the selected input range by checking the *Over Range* option. More information on the overrange setting is available in the device data sheet.

The right most section, *Sequencer Configuration*, provides a user-friendly interface to set the channel stack setting in sequencer mode. The device supports up to 32 stack options, navigating through the *Jump to Page* buttons displays these options. The stack length is selected by checking the *Last Layer* box of the final stack desired. Each stack can support non-corresponding input channels between ADC A and ADC B.

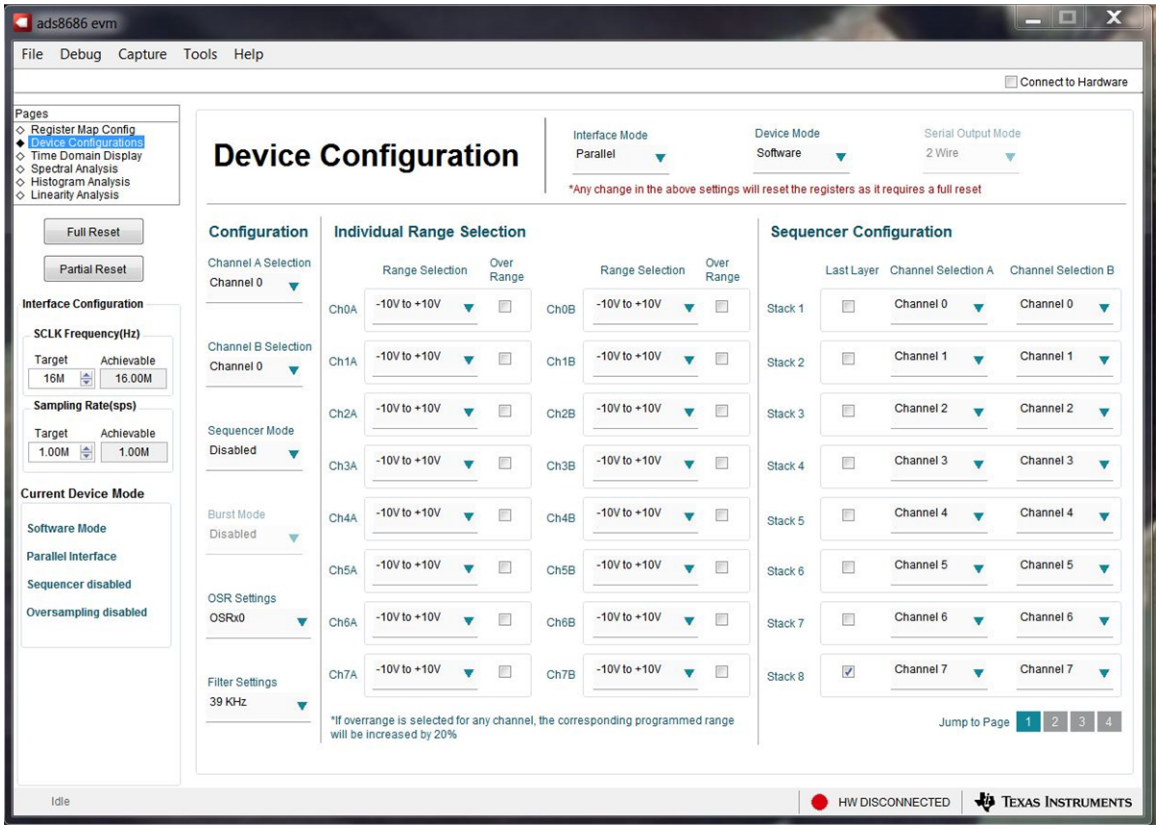


Figure 14. Device Configuration in Software Mode

6.3.2 Hardware Mode

When in hardware mode, Figure 15 shows the setting options for the *Device Configuration* page. The device has limited configuration options in hardware mode, whcih are disabled in the GUI. The *Register Map Config* page is also not accessible in hardware mode.

In hardware mode, simultaneous sampling is restricted to the corresponding ADC A and ADC B channel, that is, channel AIN_0A is always sampled with channel AIN_0B. The diagnostic channels can not be sampled in the hardware mode of operation. All input channels are configured to the same input range in hardware more. Sequencer mode is supported in hardware mode. When sequencer mode is disabled, the *Burst Mode* option is grayed out because burst mode is only available with sequencer mode enabled. The oversampling setting is also available in hardware mode, and can be selected using the drop-down field. The *Float Detection* option is displayed as a drop-down field in the *Device Configurations* page because the *Register Map Config* page is inaccessible in hardware mode.

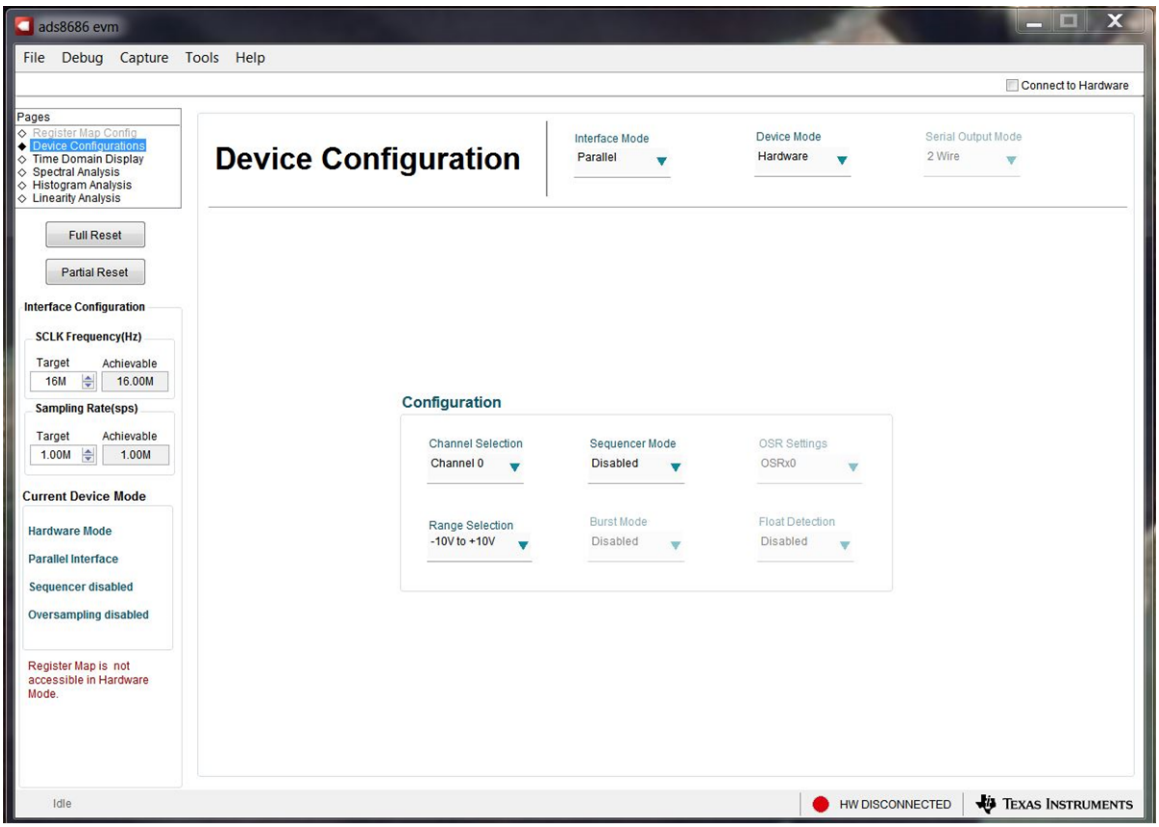


Figure 15. Device Configuration Display in Hardware Mode

6.4 Time Domain Display Tool

The *Time Domain Display* tool (Figure 16) allows visualization of the time domain conversion results given a set of analog input signals.

The GUI *Time Domain Display* shows two time domain voltage plots: the top time domain plot shows the conversion results ADC A and the bottom display shows conversion results for ADC B. The sample indices are on the x-axis and there are two y-axes showing the corresponding converted analog voltages. Any combination of desired channels can be selected using the *Analog CH AINx* selection buttons at the top-right side of the display.

When the *Capture* button is pressed, the software captures a contingent number of samples that are selected in the *Samples* field. In addition, the bottom-right side of the GUI provides information about the converted signals, such as the selected channel maximum and minimum code, maximum and minimum voltage, and the calculated RMS voltage value for the captured signal on each channel.

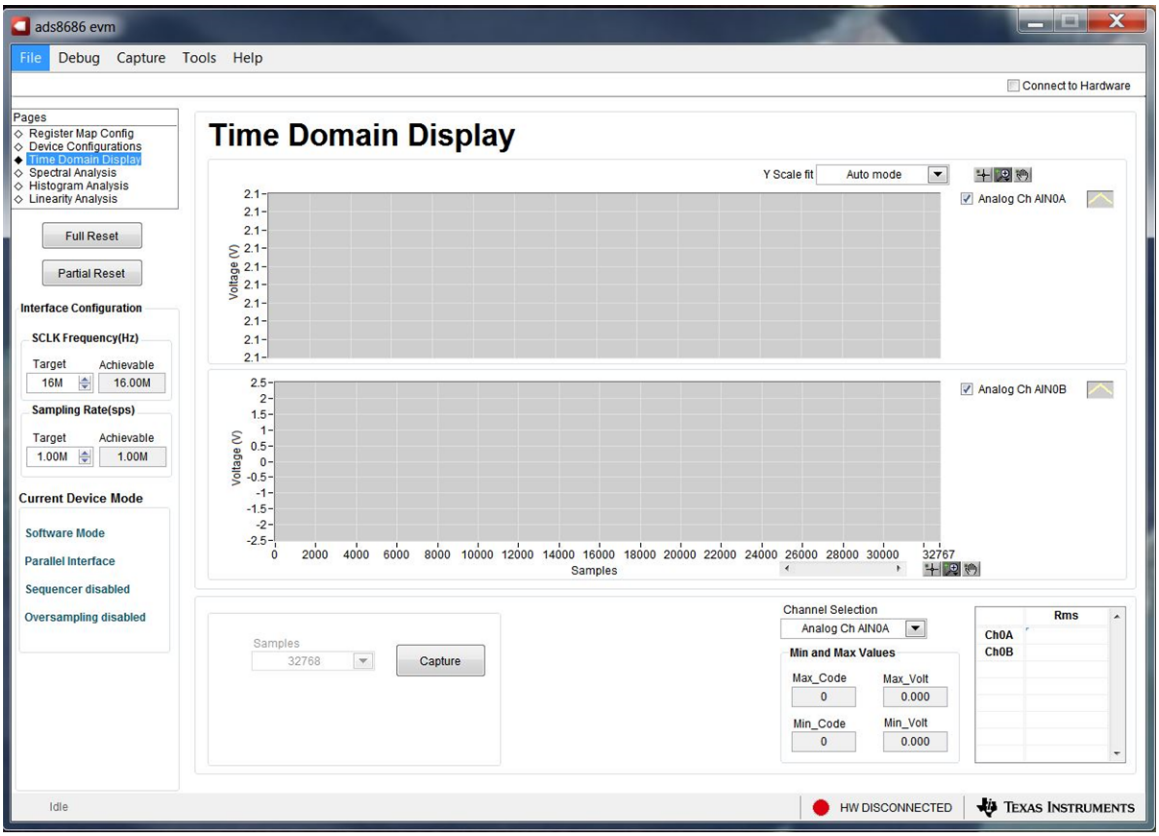


Figure 16. Time Domain Display

6.5 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8686S SAR ADC through a single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting.

For dynamic performance evaluation, the external differential source must have better specifications than the ADS8686S device in order to make sure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 6.

Table 6. External Source Requirements for Evaluation of the ADS8686S

Specification Description	Specification Value
Signal frequency	1 kHz (OSR = 0)
External source type	Single ended
External source common-mode	0 V
Maximum noise	35 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–110 dB

For 1-kHz SNR and ENOB evaluation at a maximum throughput of 200 kSPS, the optimal number of samples is 32768. More samples brings the noise floor so low that the external source phase noise can dominate the SNR and ENOB calculations. Figure 17 shows the spectral analysis tool.

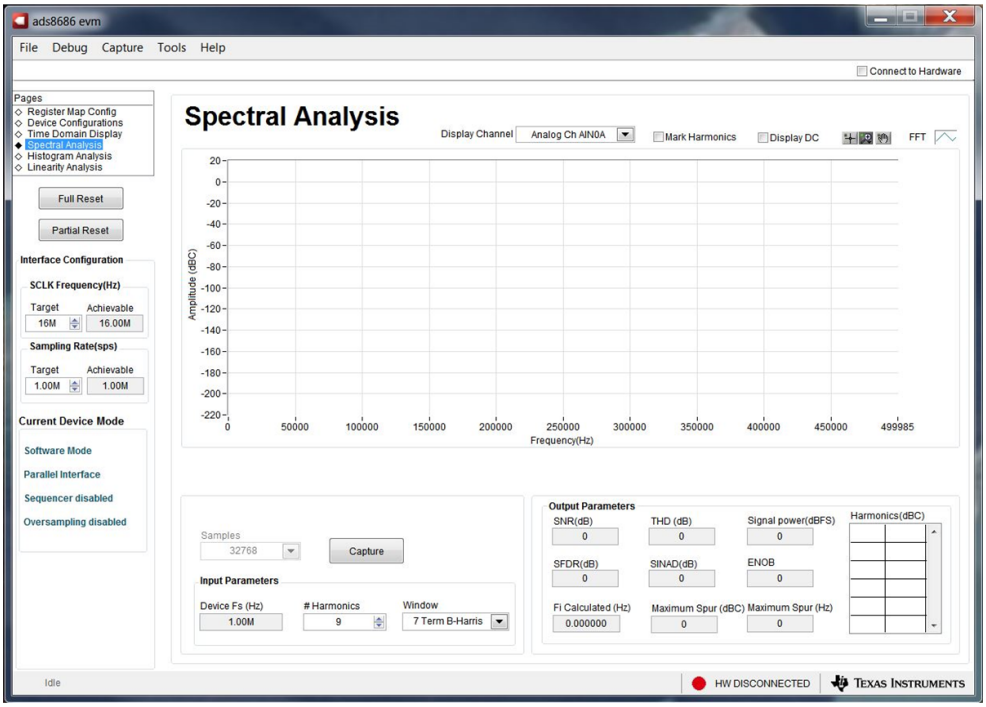


Figure 17. Spectral Analysis Tool

Finally, the FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (a discussion that is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window), and is not recommended.

6.6 Histogram Analysis Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC, is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

As shown in Figure 18, the histogram corresponding to a dc input is displayed on clicking on the *Capture* button.

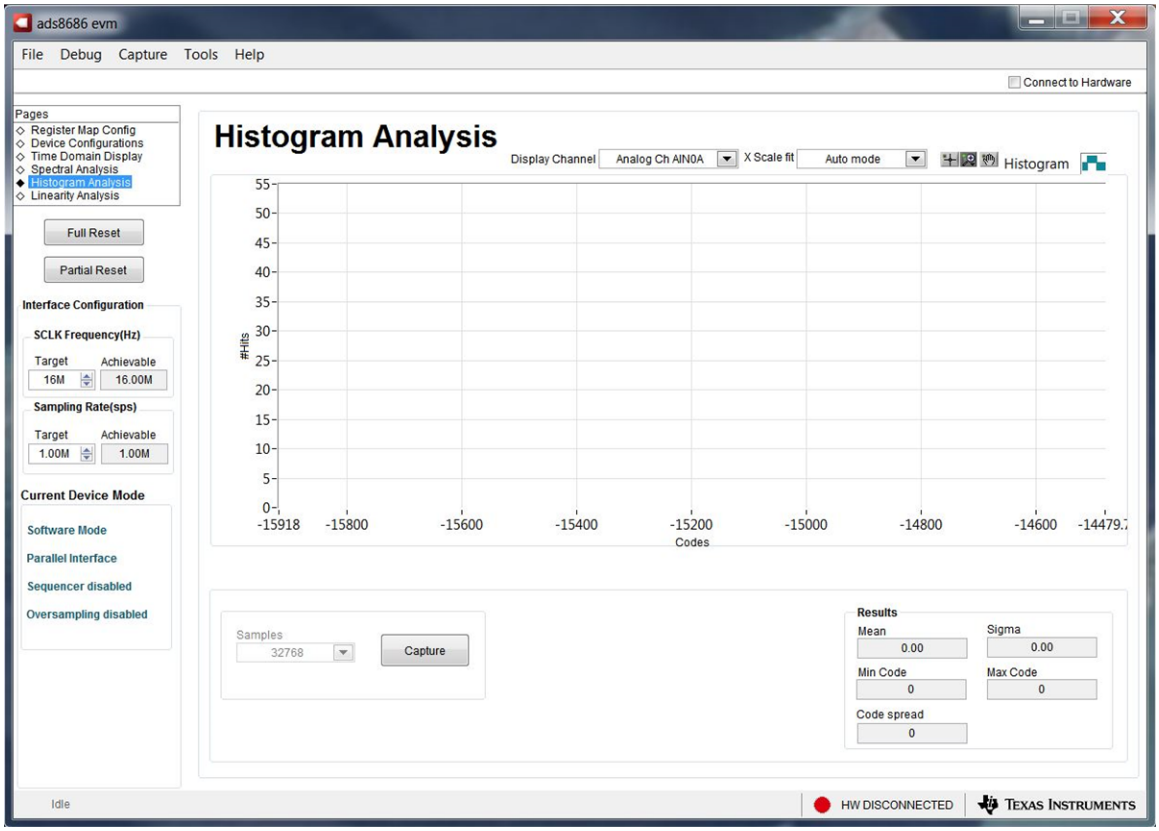


Figure 18. Histogram Analysis Tool

6.7 Linearity Analysis Tool

The linearity analysis tool measures and generates the performance DNL and INL plots over code for the ADS8686S. A 1-kHz sinusoidal input signal is required, which is slightly saturated (100 mV to 200 mV outside the full-scale range) at each input with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. To make sure that the DNL and INL of the ADC are correctly measured, the requirements in Table 7 must be met by the external source.

Table 7. External Source Requirements for ADS8686S Evaluation

Specification Description	Specification Value
Signal frequency	1 kHz
External source type	Single ended, referred to GND
External source common mode	0 V
Signal Amplitude	10.2 Vp (TBD V_{PP}?) for ±10-V range; 5.1 Vp (TBD V_{PP}?) for ±5-V range; 2.55 Vp (TBD V_{PP}?) for ±2.5-V range;
Maximum noise	35 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–110 dB

The *number-of-hits* setting depends on the external noise source. For a 100-dB SNR external source with approximately 30 µVrms of noise, the total number of hits must be 256. Figure 19 shows the linearity analysis tool.

NOTE: This analysis can take a couple of minutes to run; therefore, the evaluation board must remain undisturbed during the complete duration of the analysis.

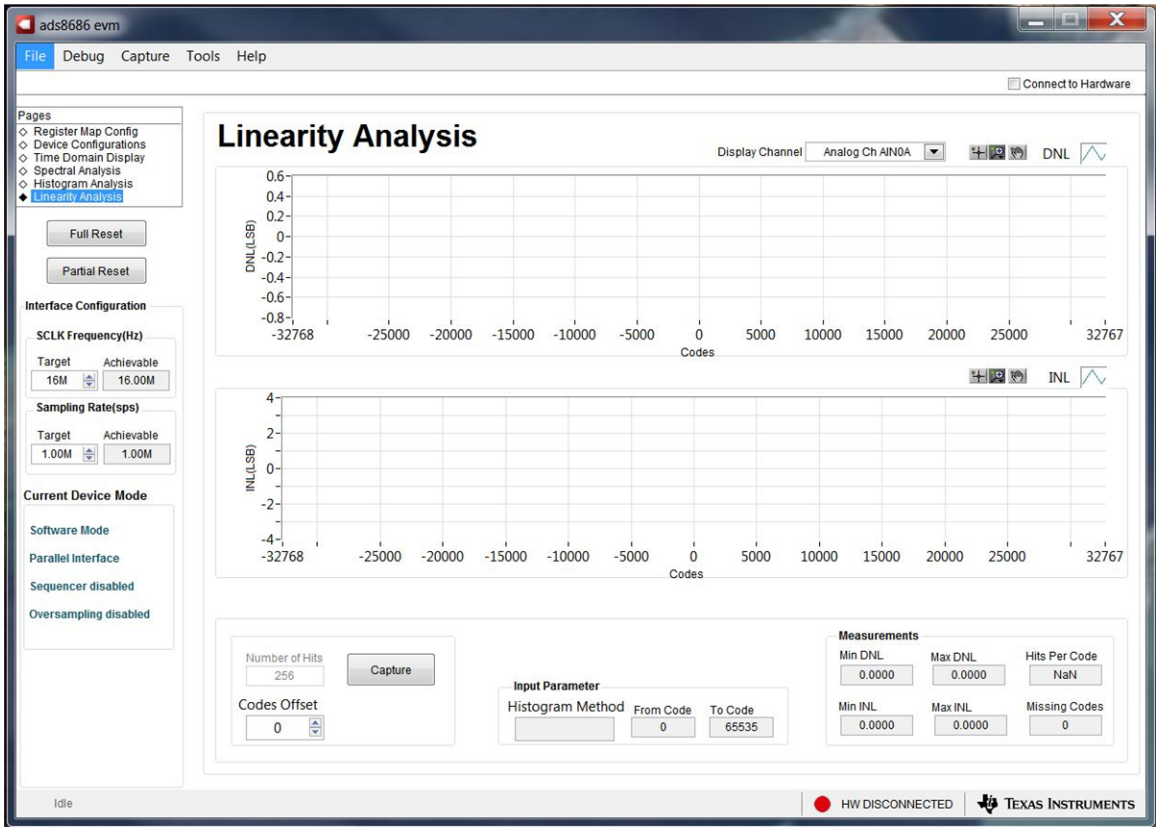


Figure 19. Linearity Analysis Tool

7 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS8686S EVM bill of materials (BOM), printed circuit board (PCB) layout, and the EVM schematics.

7.1 Bill of Materials

Table 8 lists the ADS8686SEVM BOM.

Table 8. ADS8686S EVM Bill of Materials

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
DC029	1	N/A	Any	Printed Circuit Board for Evaluation of ADS8686S
PHI-EVM-CONTROLLER (Edge# 6591636 rev. B)	1	N/A	Texas Instruments	USB Controller Board for ADC EVMs (Kit Item)
GRM188R60J106ME84	10	C1, C3, C5, C7, C9, C11, C15, C17, C18, C21	MuRata	CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0603
550L104KCAT	14	C2, C4, C6, C8, C10, C12, C16, C44, C45, C46, C47, C48, C50, C51	AT Ceramics	CAP, CERM, 0.1 uF, 16 V, +/- 10%, 0402
C0805C104K4RACTU	1	C13	Kemet	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0805
C0805C106K8PACTU	3	C14, C26, C43	Kemet	CAP, CERM, 10 uF, 10 V, +/- 10%, X5R, 0805
GRM31CR61A226ME19L	1	C19	MuRata	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 1206
GRM188R71E105KA12D	5	C23, C24, C25, C49, C52	MuRata	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
GRM1885C1H102FA01J	16	C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42	MuRata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	Machine Screw Pan PHILLIPS 4-40
1891	4	H5, H6, H7, H8	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
9774050360R	2	H9, H10	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
RM3X4MM 2701	2	H11, H12	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
1803633	4	H13, H14, H15, H16	Phoenix Contact	Terminal Block Plug, 8 Pos, 3.81mm
5-1814832-1	4	J1, J2, J9, J10	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
QTH-030-01-L-D-A	1	J17	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
TSW-116-07-G-D	1	J18	Samtec	Header, 100mil, 16x2, Gold, TH
PBC03SAAN	6	JP1, JP2, JP3, JP4, JP5, JP7	Sullins Connector Solutions	Header, 100mil, 3x1, Gold, TH
5-146261-1	3	JP6, JP8, JP9	TE Connectivity	Header, 100mil, 2x1, Gold, TH
CRCW040210K0FKED	5	R2, R27, R122, R126, R132	Vishay-Dale	RES, 10.0 k, 1%, 0.063 W, 0402
CRCW0402100KFKED	19	R5, R6, R7, R8, R9, R10, R11, R12, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R124	Vishay-Dale	RES, 100 k, 1%, 0.063 W, 0402

Table 8. ADS8686S EVM Bill of Materials (continued)

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
CRCW12060000Z0EA	17	R28, R34, R36, R44, R46, R54, R56, R64, R66, R74, R76, R84, R86, R94, R96, R104, R106	Vishay-Dale	RES, 0, 5%, 0.25 W, 1206
RT0603BRD0710KL	1	R31	Yageo America	RES, 10.0 k, 0.1%, 0.1 W, 0603
ERJ-3RQFR22V	1	R32	Panasonic	RES, 0.22, 1%, 0.1 W, 0603
CRCW04022K70JNED	2	R33, R125	Vishay-Dale	RES, 2.7 k, 5%, 0.063 W, 0402
RG1608P-102-B-T5	32	R35, R37, R40, R41, R45, R47, R50, R51, R55, R57, R60, R61, R65, R67, R70, R71, R75, R77, R80, R81, R85, R87, R90, R91, R95, R97, R100, R101, R105, R107, R110, R111	Susumu Co Ltd	RES, 1.00 k, 0.1%, 0.1 W, 0603
CRCW06030000Z0EA	18	R42, R43, R52, R53, R62, R63, R72, R73, R82, R83, R92, R93, R102, R103, R112, R113, R130, R133	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
CRCW040249R9FKED	9	R114, R115, R116, R117, R118, R119, R120, R121, R123	Vishay-Dale	RES, 49.9, 1%, 0.063 W, 0402
RC0402JR-070RL	1	R127	Yageo America	RES, 0, 5%, 0.063 W, 0402
EVQPNF04M	1	S1	Panasonic	Switch, Tactile, SPST-NO, 0.05A, 12V, SMD
382811-6	7	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	AMP	Shunt, 100mil, Gold plated, Black
ED555/4DS	1	T1	On-Shore Technology	Terminal Block, 3.5mm Pitch, 4x1, TH
1803332	4	T2, T3, T4, T5	Phoenix Contact	Header(shrouded), 3.81mm, 8x1, Tin, R/A, TH
ED555/3DS	1	T6	On-Shore Technology	Terminal Block, 3.5mm Pitch, 3x1, TH
5001	2	TP1, TP2	Keystone	Test Point, Miniature, Black, TH
5002	3	TP3, TP4, TP5	Keystone	Test Point, Miniature, White, TH
ADS8686-PZA	1	U1	Texas Instruments	16-Channel DAS with 16-Bit, Bipolar Input, Dual Simultaneous Sampling ADC, PZA0080A (LQFP-80)
TPS7A4700RGWR	1	U3	Texas Instruments	36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A (VQFN-20)
REF5025AIDGKT	1	U4	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin MSOP(DGK), Green (RoHS & no Sb/Br)
BR24G32FVT-3AGE2	1	U5	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
OPA192IDBVT	1	U6	Texas Instruments	Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with E-trim, 4.5 to 36 V, -40 to 125 degC, 8-Pin SOT-23 (DBV), Green (RoHS & no Sb/Br), Tape and Reel
INA149AID	1	U7	Texas Instruments	High Common Mode Voltage Difference Amplifier, -40 to 125 degC, 8-pin SOIC (D8), Green (RoHS & no Sb/Br)
GRM188R60J106ME84	0	C20, C22	MuRata	CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0603
SMBJ14CA	0	D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19	Littelfuse	Diode, TVS, Bi, 14 V, SMB

Table 8. ADS8686S EVM Bill of Materials (continued)

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
5-1814832-1	0	J3, J4, J5, J6, J7, J8, J11, J12, J13, J14, J15, J16	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
1269AS-H-4R7M=P2	0	L1	MuRata Toko	Inductor, Shielded, Metal Composite, 4.7 uH, 1.2 A, 0.25 ohm, SMD
CRCW040210K0FKED	0	R1	Vishay-Dale	RES, 10.0 k, 1%, 0.063 W, 0402
CRCW0402100KFKED	0	R3, R4, R13, R14, R15, R16, R30, R129	Vishay-Dale	RES, 100 k, 1%, 0.063 W, 0402
CRCW04021M00JNED	0	R29	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
CRCW06030000Z0EA	0	R38, R39, R48, R49, R58, R59, R68, R69, R78, R79, R88, R89, R98, R99, R108, R109, R131, R134, R135	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
RC0402JR-070RL	0	R128	Yageo America	RES, 0, 5%, 0.063 W, 0402
TPS61220DCKR	0	U2	Texas Instruments	Low Input Voltage, 0.7V Boost Converter with 5.5uA Quiescent Current, DCK0006A (SOT-SC70-6)

7.2 PCB Layout

Figure 21 through Figure 25 illustrate the EVM PCB layout.

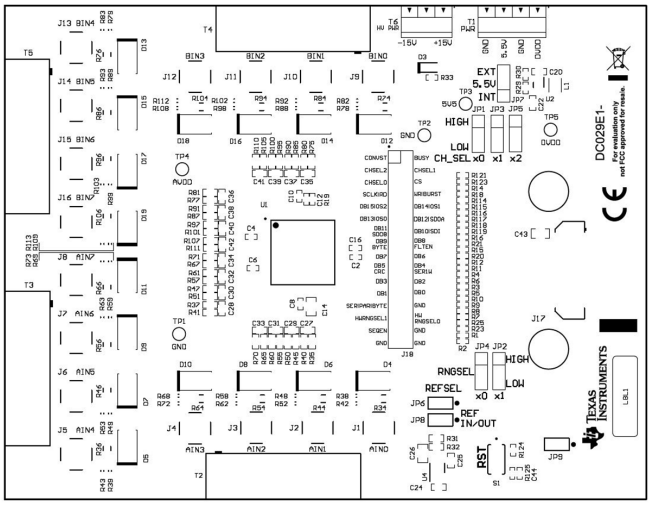


Figure 20. ADS8686S EVM PCB: Top Overlay

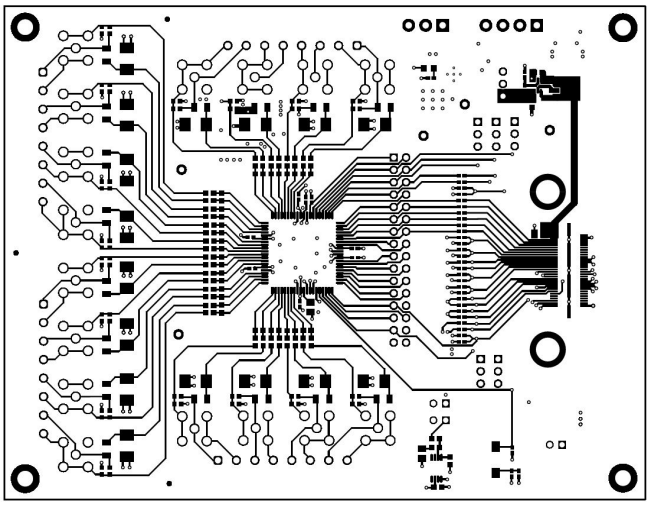


Figure 21. ADS8686S EVM PCB Layer 1: Top Layer

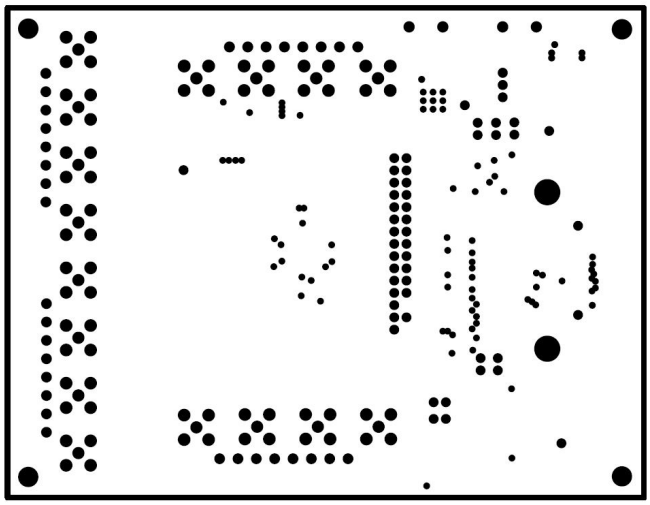


Figure 22. ADS8686S EVM PCB Layer 2: GND Plane

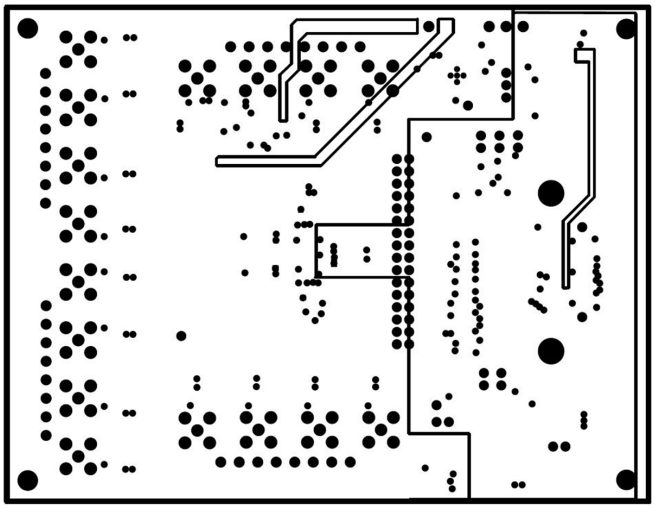


Figure 23. ADS8686S EVM PCB Layer 3: Power Planes

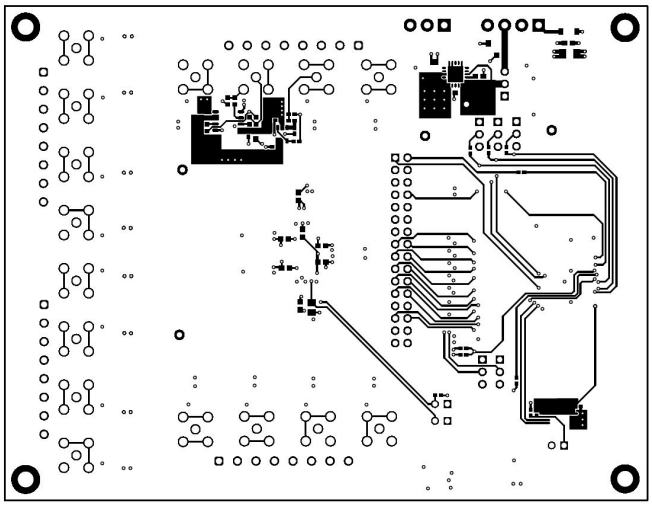


Figure 24. ADS8686S EVM PCB Layer 4: Bottom Layer

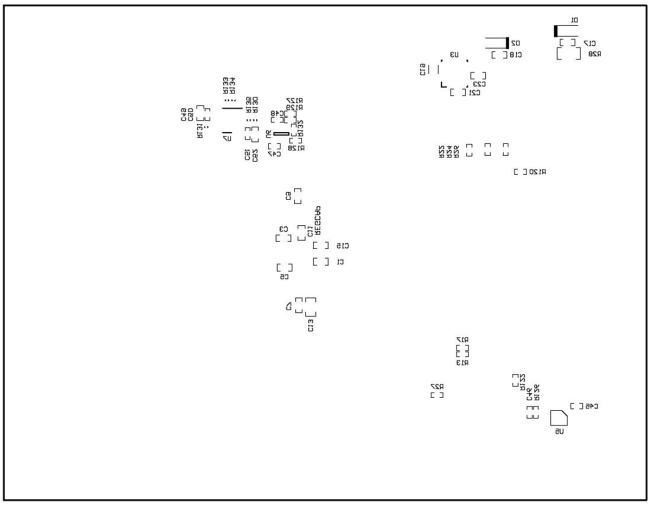


Figure 25. ADS8686S EVM PCB: Bottom Overlay

7.3 Schematics

Figure 26 through Figure 26 illustrate the EVM schematics.

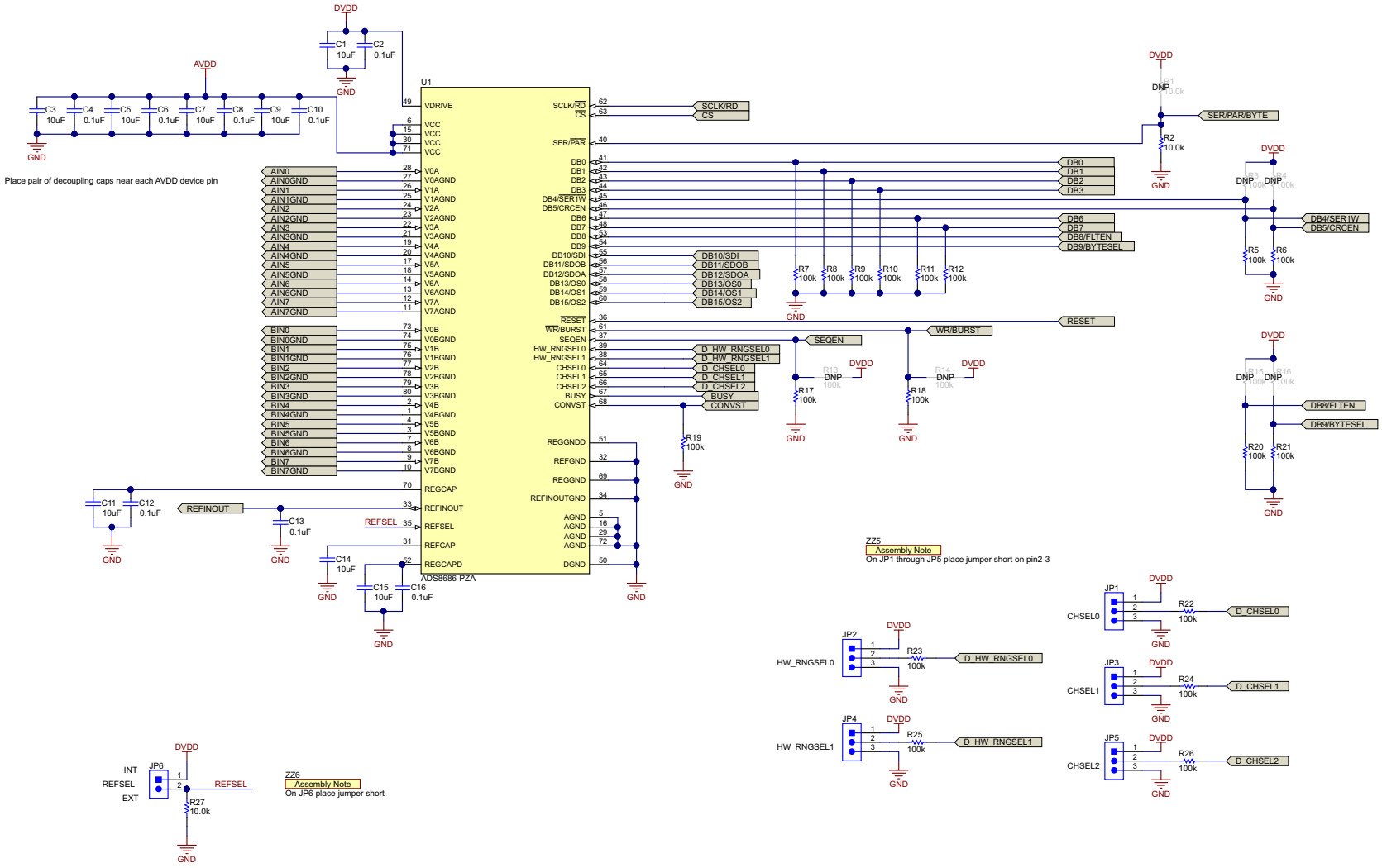


Figure 26. ADS8686SEVM-PDK Schematic

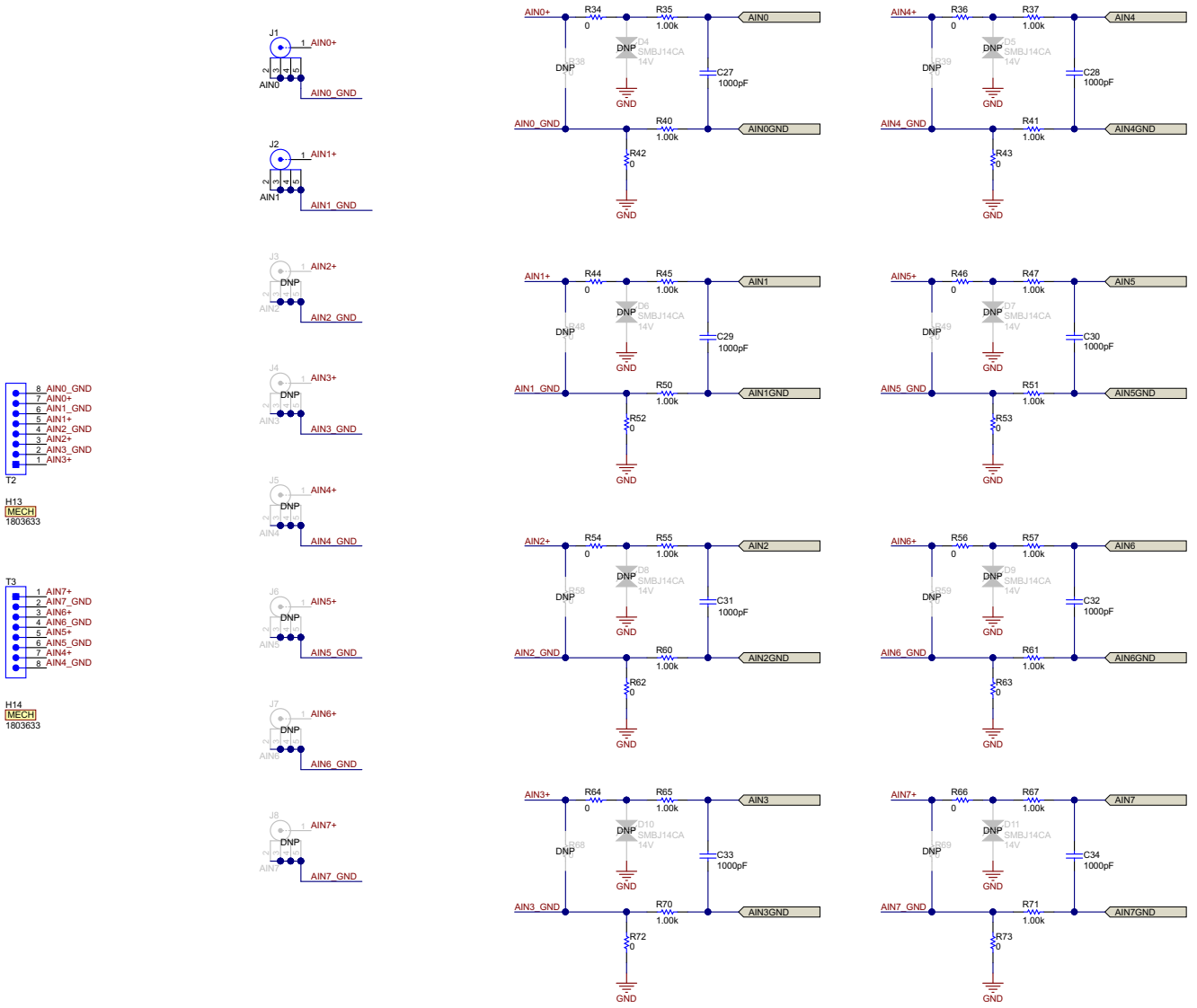


Figure 27. ADS8686SEVM-PDK Schematic

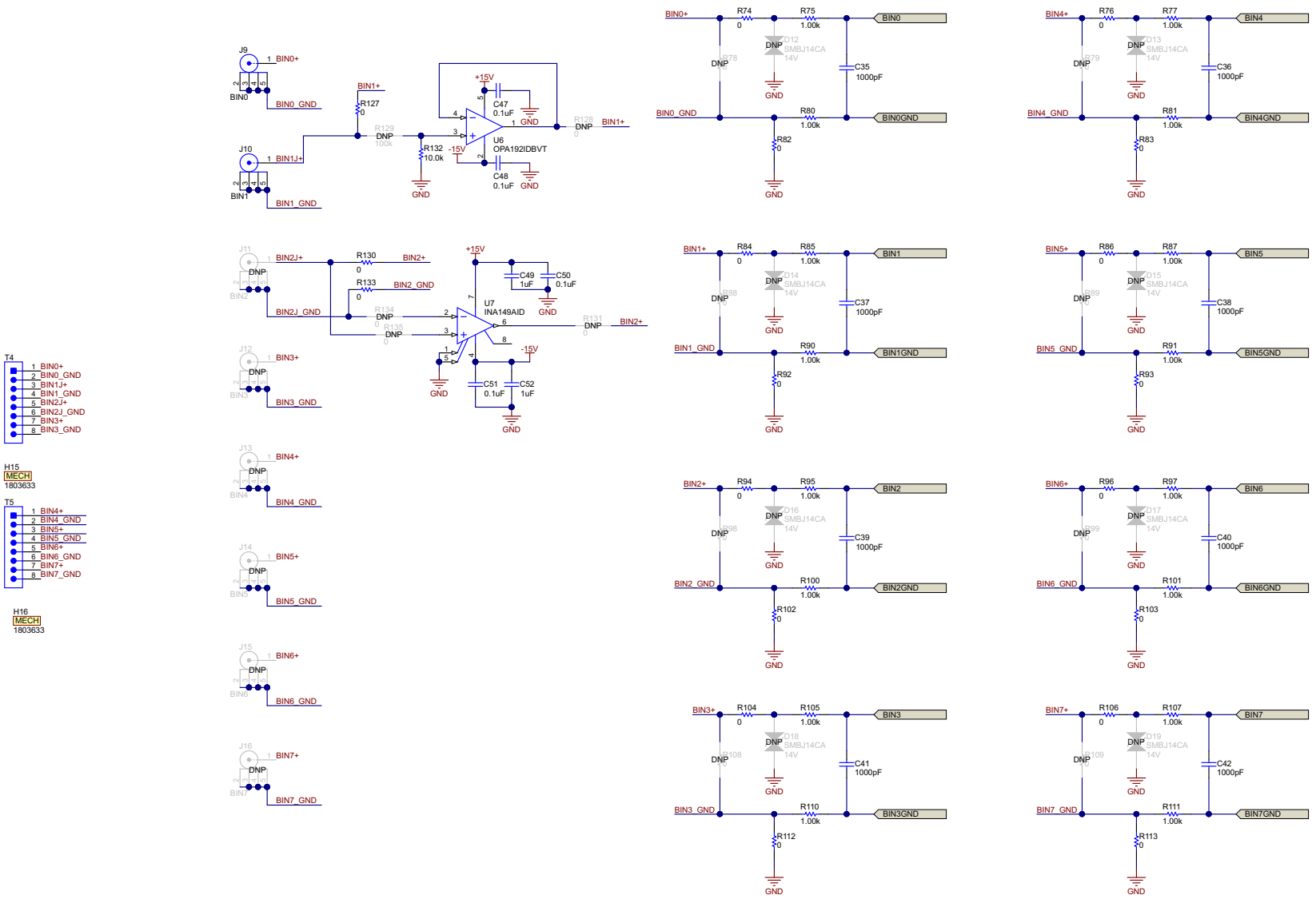


Figure 28. ADS8686SEVM-PDK Schematic

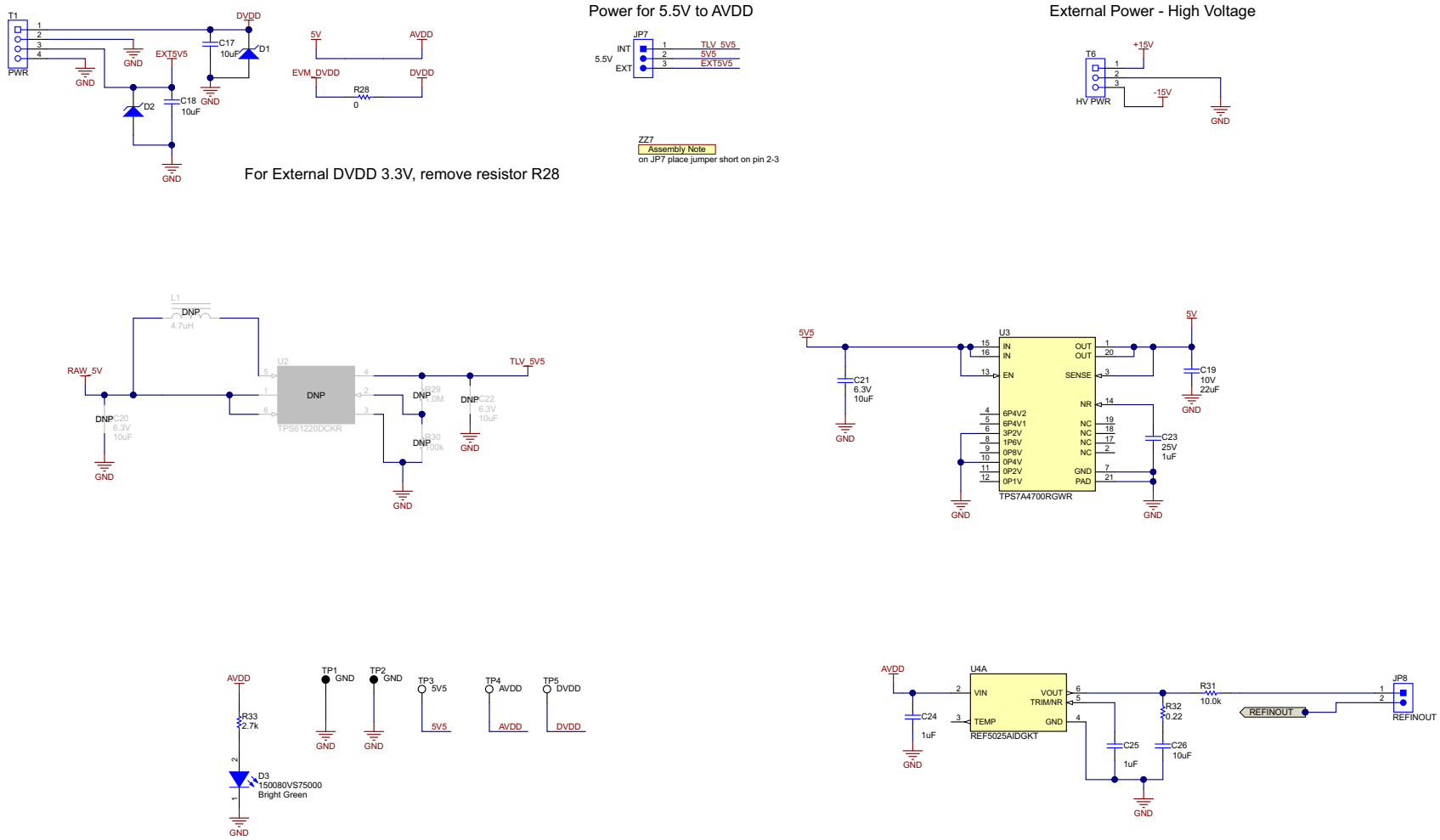


Figure 29. ADS8686SEVM-PDK Schematic

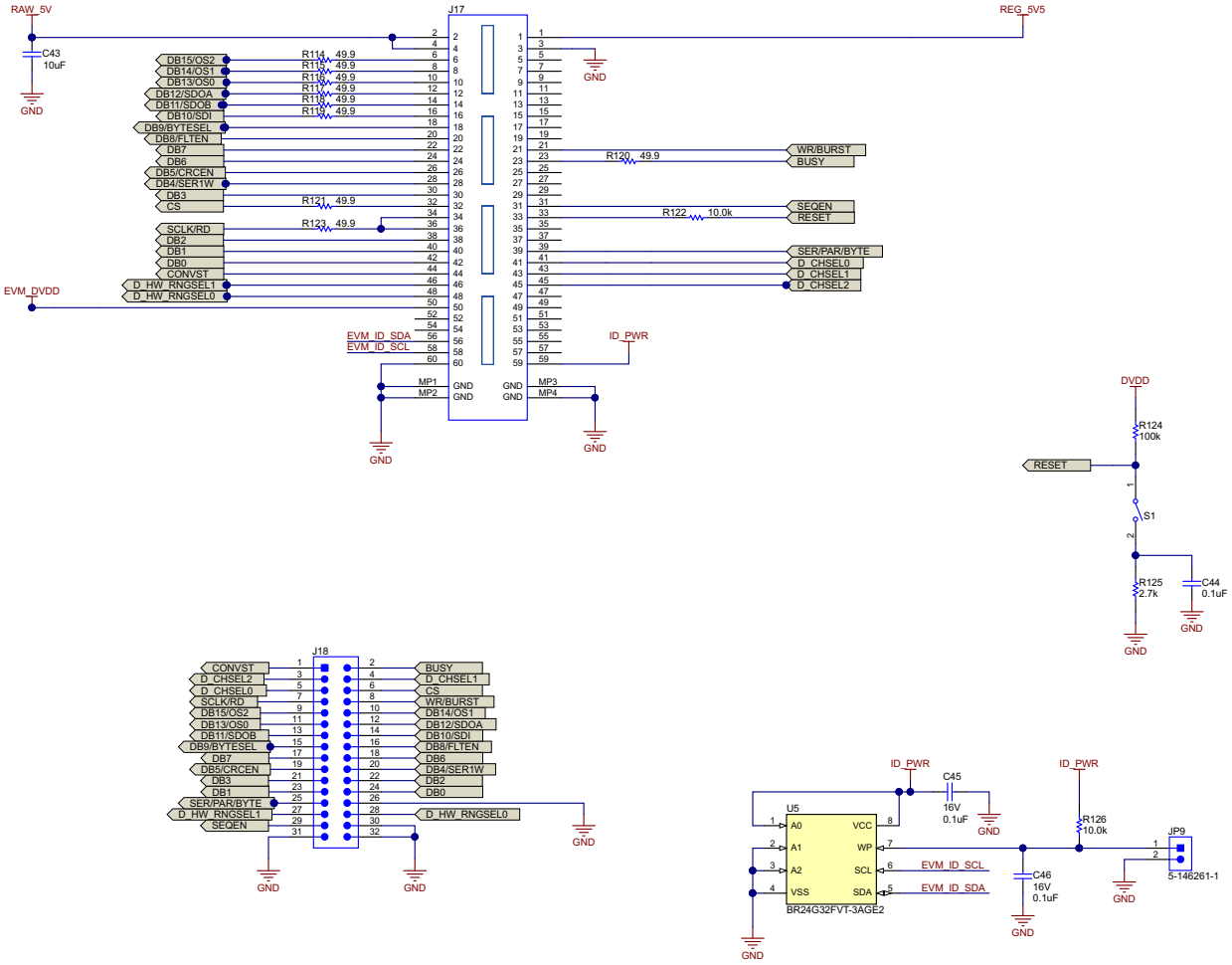


Figure 30. ADS8686SEVM-PDK Schematic

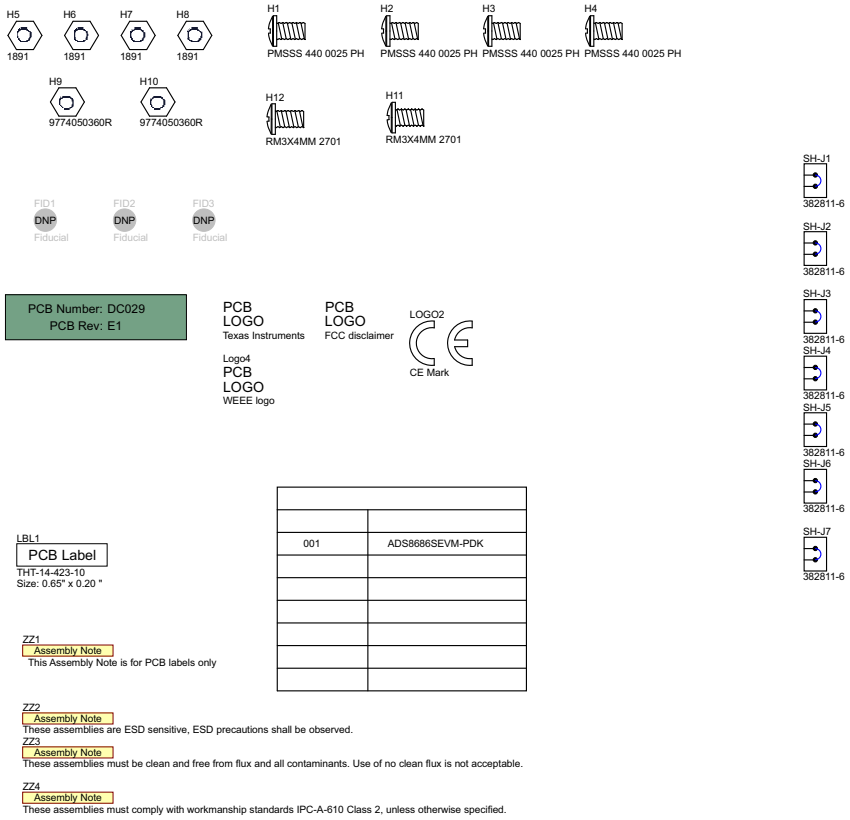


Figure 31. ADS8686SEVM-PDK Schematic

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