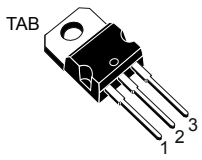
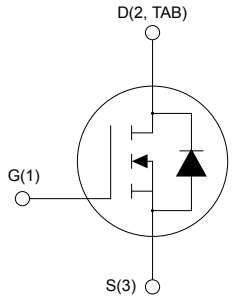
STP150N10F7AG

Datasheet

Automotive N-channel 100 V, 3.6 mΩ typ., 110 A, STripFET F7 Power MOSFET in a TO-220 package



TO-220



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP150N10F7AG	100 V	4.2 mΩ	110 A

- Designed for automotive application
- Standard level $V_{GS(TH)}$
- 175°C junction temperature
- 100% avalanche rated

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STP150N10F7AG

Product summary	
Order code	STP150N10F7AG
Marking	150N10F7AG
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	110	A
	Drain current (continuous) at T_C = 100 °C		
I_{DM} (2)	Drain current (pulsed)	440	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
I_{AV}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	30	A
E_{AS}	Single pulse avalanche energy (T_J = 25 °C, I_D = I_{AV}, V_{DD} = 25 V)	650	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Current limited by package.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.6	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	62.5	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 3. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = max ratings			1	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 55 A		3.6	4.2	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	9000	-	pF
C_{oss}	Output capacitance			2000		pF
C_{rss}	Reverse transfer capacitance			80		pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 110 A, V_{GS} = 10 V (see Figure 13. Test circuit for gate charge behavior)	-	127	-	nC
Q_{gs}	Gate-source charge		-	56	-	nC
Q_{gd}	Gate-drain charge		-	32	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 55 A, R_G = 4.7 mΩ, V_{GS}= 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 16. Unclamped inductive waveform)	-	37	-	ns
t_r	Rise time		-	54	-	ns
$t_{d(off)}$	Turn-off delay time		-	68	-	ns
t_f	Fall time		-	33	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 110 A, V_{GS} = 0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 110 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_j = 25°C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	60	-	ns
Q_{rr}	Reverse recovery charge		-	83	-	nC
I_{RRM}	Reverse recovery current		-	2.75	-	A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

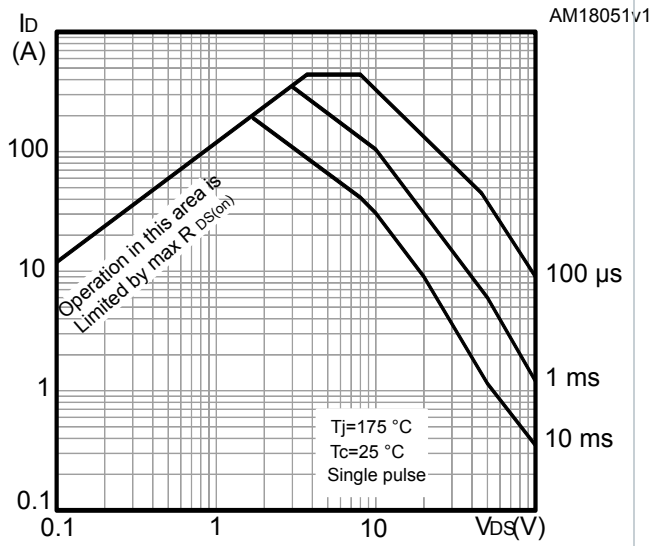


Figure 2. Thermal impedance

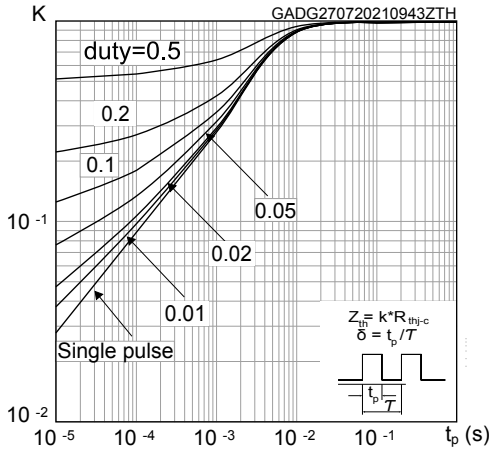


Figure 3. Typical output characteristics

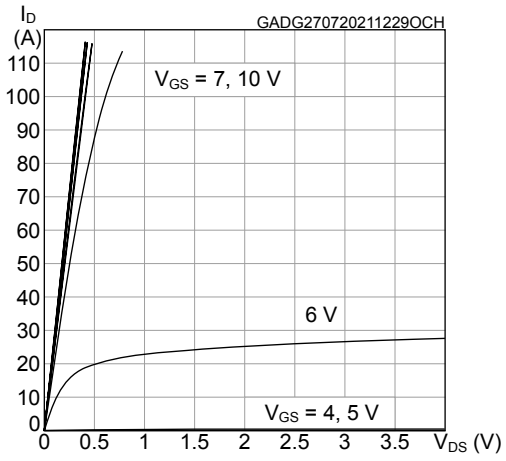


Figure 4. Typical transfer characteristics

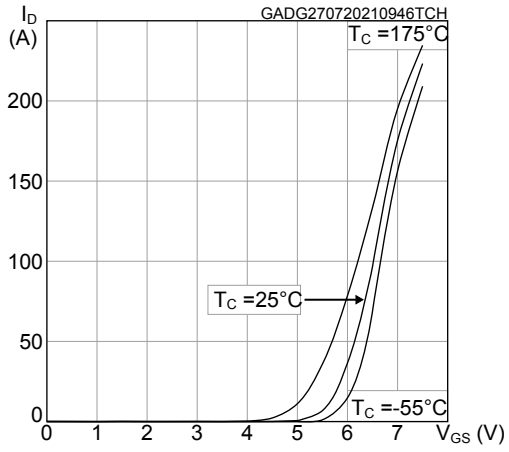


Figure 5. Typical gate charge characteristics

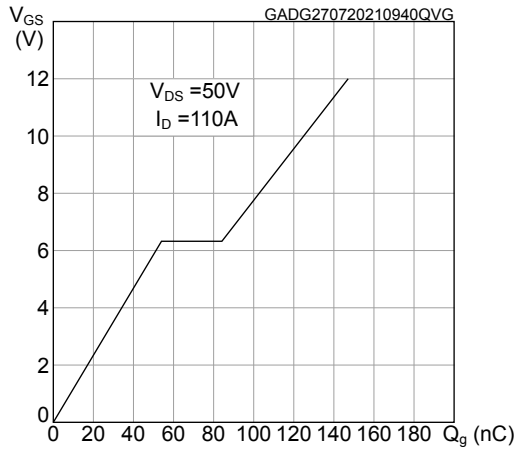


Figure 6. Typical drain-source on-resistance

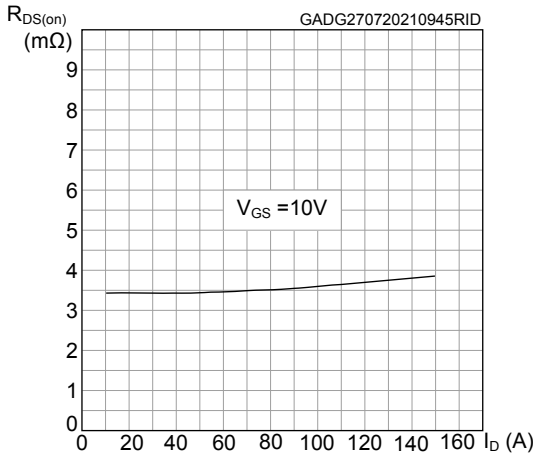


Figure 7. Typical capacitance characteristics

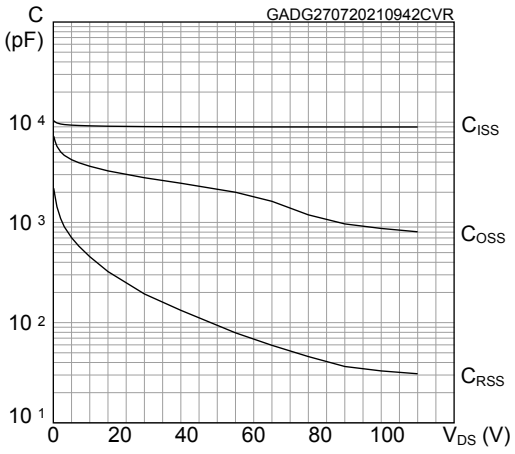


Figure 8. Normalized gate threshold voltage vs temperature

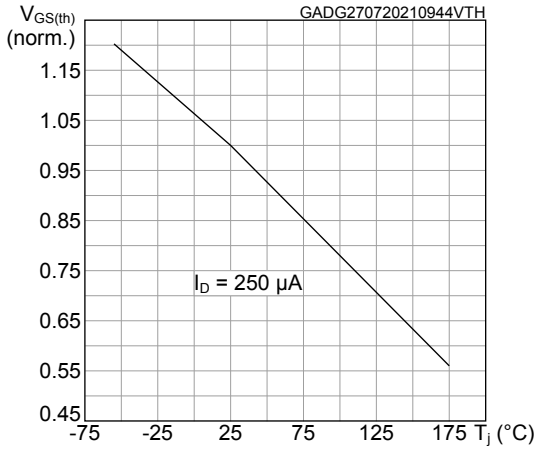


Figure 9. Normalized on-resistance vs temperature

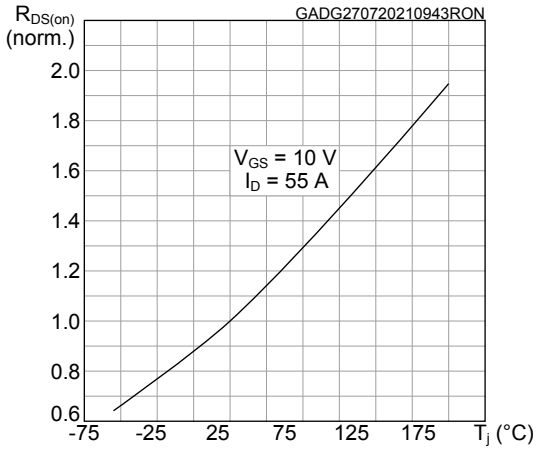


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

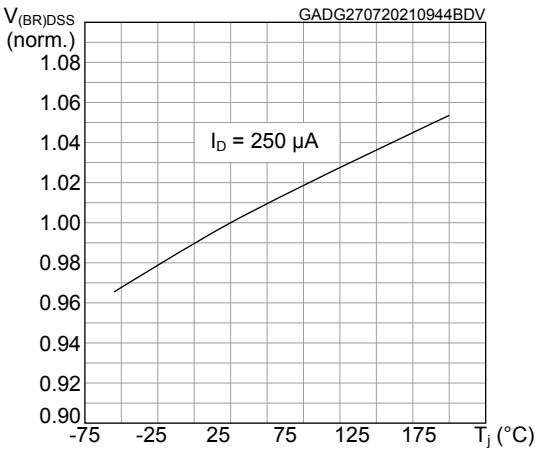
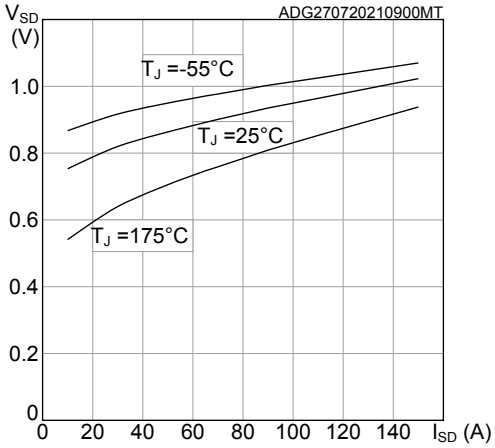
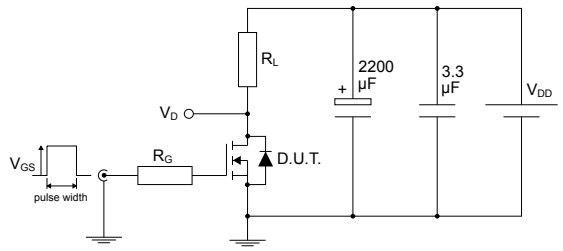


Figure 11. **Source-drain diode forward characteristics**



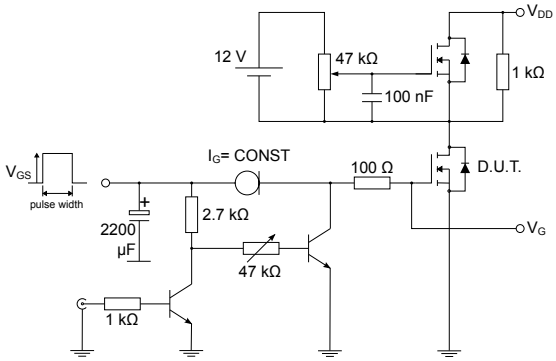
3 Test circuits

Figure 12. Test circuit for resistive load switching times



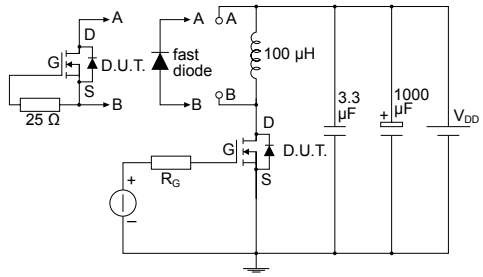
AM01468v1

Figure 13. Test circuit for gate charge behavior



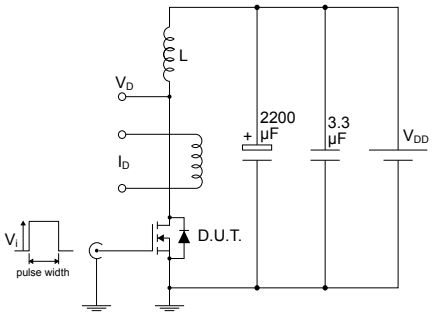
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times



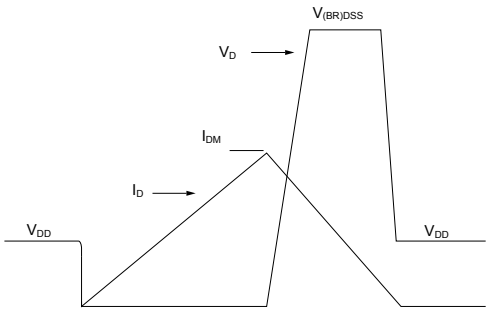
AM01470v1

Figure 15. Unclamped inductive load test circuit



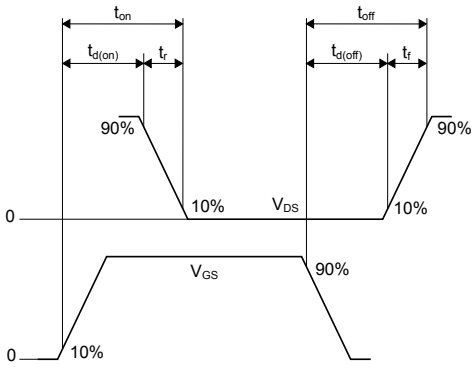
AM01471v1

Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



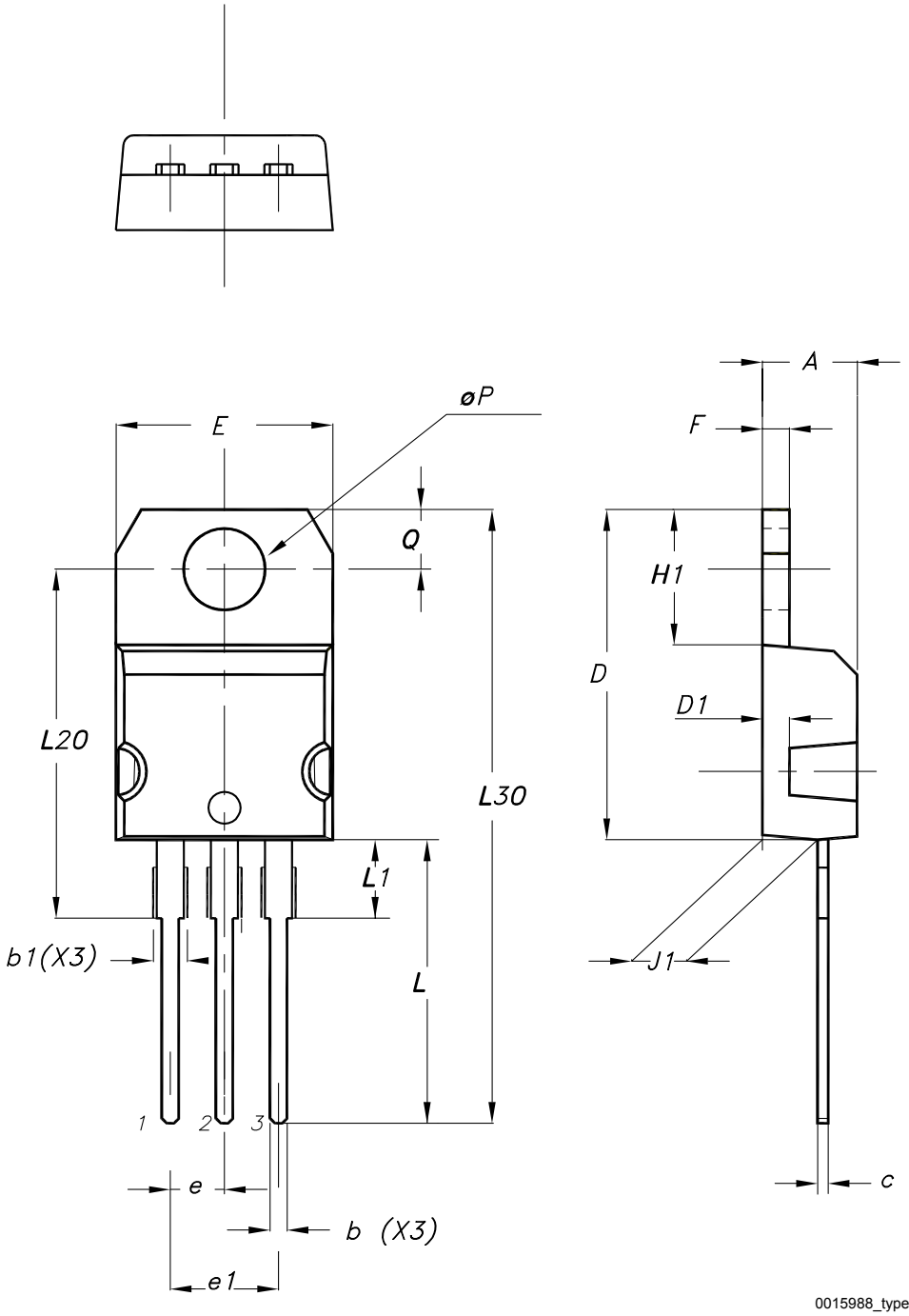
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 18. **TO-220 type A package outline**



0015988_typeA_Rev_23

Table 7. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 8. **Document revision history**

Date	Version	Changes
27-Jul-2021	1	First release
16-Mar-2023	2	Updated title in cover page

Contents