Product Change Notification - SYST-05GMYQ876

Date:

06 Feb 2020

Product Category:

Microprocessors

Affected CPNs:

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Notification subject:

Data Sheet - SAMA5D3 Series Data Sheet

Notification text:

SYST-05GMYQ876

Microchip has released a new Product Documents for the SAMA5D3 Series Data Sheet of devices. If you are using one of these devices please read the document located at SAMA5D3 Series Data Sheet.

Notification Status: Final

Description of Change:

1) Template update: Moved from Atmel to Microchip template.

2) The datasheet is assigned a new document number (DS60001609) and revision letter is reset to A.

3) Document number DS60001609 revision A corresponds to what would have been 11121 revision G.

4) ISBN number assigned.

5) Section 3. Package and Pinout: Table 3-1 SAMA5D3 Pinout for 324-ball LFBGA Package and Table 3-2 SAMA5D3 Pinout for 324-ball TFBGA
Package: modified detail on Reset State for PE26. Added table note on Reset State. Added GMAC to Table 3-3 SAMA5D3 I/O Type Description.

6) Section 4. Power Considerations: updated description of Table 4-1 SAMA5D3 Power Supplies. Updated Section 4.2 Power Sequence Requirements.

7) Section 8. Peripherals: updated ‘Reserved' PIDs in Table 8-1 Peripheral Identifiers.

8) Section 10. Debug and Test: updated Figure 10-1 Debug and Test Block Diagram.

9) Section 11. Standard Boot Strategies: updated nbSectorPerPage description in section NAND Flash Specific Header Detection.

10) Section 14. Bus Matrix (MATRIX): updated Matrix slaves.

11) Section 22. Real-time Clock (RTC): deleted all references to Register Write Protection.

12) Section 25. Clock Generator: added CAL field detail in Section 25.5.2 12 MHz RC Oscillator Clock Frequency Adjustment.

13) Section 29. Multi-port DDR-SDRAM Controller (MPDDRC): modified row range in Table 29-8 Interleaved Mapping DDR-SDRAM Configuration Mapping: 8K Rows, 512/1024/2048 Columns, 4 banks. 14) Section 33. Image Sensor Interface (ISI): added important note to Section 33.4.2 Power Management.

15) Section 36. Gigabit Ethernet MAC (GMAC): updated Section 36.9.10 GMAC Interrupt Status Register, Section 36.9.11 GMAC Interrupt Enable Register, Section 36.9.12 GMAC Interrupt Disable Register, Section 36.9.13 GMAC Interrupt Mask Register with TSUTIMCOMP bit (index 29).

16) Section 37. Ethernet 10/100 MAC (EMAC): updated Section 37.4.14 Physical Interface with support for RMII only.

17) Section 39. Serial Peripheral Interface (SPI): deleted REQCLR bit in Section 39.8.1 SPI Control Register.

18) Section 40. Two-wire Interface (TWI): updated Figure 40-25 Master Performs a General Call. Updated bit descriptions CHDIV, CLDIV in Section 40.8.5 TWI Clock Waveform Generator Register.

19) Section 54. Electrical Characteristics: Table 54-2 DC Characteristics: added RPULL for GMAC pads. Section 54.16 SSC Timings: updated Figure 54-23 SSC Transmitter, TK and TF in Input;

updated Table 54-60 SSC Timings with 3.3V Peripheral Supply and Table 54-61 SSC Timings with 1.8V Peripheral Supply. Added Section 54.20 USART in Asynchronous Modes. Table 54-73 Two-wire Serial Bus Requirements: updated formulae in Note (2).
20) Section 55. Mechanical Characteristics: added reference to Microchip Packaging Specification.
21) Section 56. Schematic Checklist: updated Description for VDDIOM in Table 56-1 Power Supply Connections.
22) Section 59. Errata: Added errata: Section 59.6.2 DMAC: Not possible to transfer data with DMA to the SHA when SHA384 or SHA512 algorithm is selected Section 59.9.3 GMAC: Bad association of timestamps and PTP packets Section 59.11.1 USART: USART Framing error not detected if last data bit is 1

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 6 Feb 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):
SAMA5D3 Series Data Sheet

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Affected Catalog Part Numbers (CPN)

ATSAMA5D3-XPLD
ATSAMA5D31A-CFU
ATSAMA5D31A-CFUR
ATSAMA5D31A-CU
ATSAMA5D31A-CUR
ATSAMA5D33A-CU
ATSAMA5D33A-CUR
ATSAMA5D34A-CU
ATSAMA5D34A-CUR
ATSAMA5D35A-CN
ATSAMA5D35A-CNR
ATSAMA5D35A-CU
ATSAMA5D35A-CUR
ATSAMA5D36A-CN
ATSAMA5D36A-CNR
ATSAMA5D36A-CU
ATSAMA5D36A-CUR
ATSAMA5D36A-W