Circuits from the Lab® Reference Designs

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Devices Connected/Referenced	
LTC4331	I²C Slave Device Extender Over Rugged Differential Link
LTC4332	SPI Extender Over Rugged Differential Link

Robust SPI/I²C Communications for Long Distance Industrial Applications

EVALUATION AND DESIGN SUPPORT

- Circuit Evaluation Boards
  - CN0564 Circuit Evaluation Board (EVAL-CN0564-ARDZ)
- Design and Integration Files
  - Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The serial peripheral interface (SPI) and inter-integrated circuit (I²C) interface are popular de-facto communication standards for short-distance, intra-board connectivity between a controller and external peripherals. SPI and I²C have been widely adopted by sensor, actuator, and data converter manufacturers due to widely available hardware and software support. Implementation of these interfaces is straightforward when the controller and peripheral are on the same circuit board, share a common ground plane, and are not separated by long distances (>1 meter).

However, applications such as condition-based monitoring, factory automation, building automation, and structural monitoring, require peripherals be located remotely, typically far from the controller. System designers have traditionally extended these interfaces using repeaters or drivers with a higher drive strength at the expense of increasing the overall cost, complexity, and power consumption.

The circuit shown in Figure 1 solves the problem of long distance, robust, SPI/I²C communication simply and easily without any sacrifices to circuit component count, operating speed, or software complexity. Error free operation in high noise, harsh industrial environments requires tolerance to large ground potential differences. The SPI/ I²C extenders feature robust transceivers, which operate over an extended common mode range of ±25 V (for SPI communication) and ±15 V (for I²C communication) for distances up to 1200 meters. Each link consists of a single device at either end of the cable, capable of being powered from 3 V to 5.5 V, while a separate logic supply allows the I²C or SPI interface to operate from 1.62 V to 5.5 V. The extenders also provide an internal control interface for fault monitoring, which is critically important when monitoring equipment over long distances.

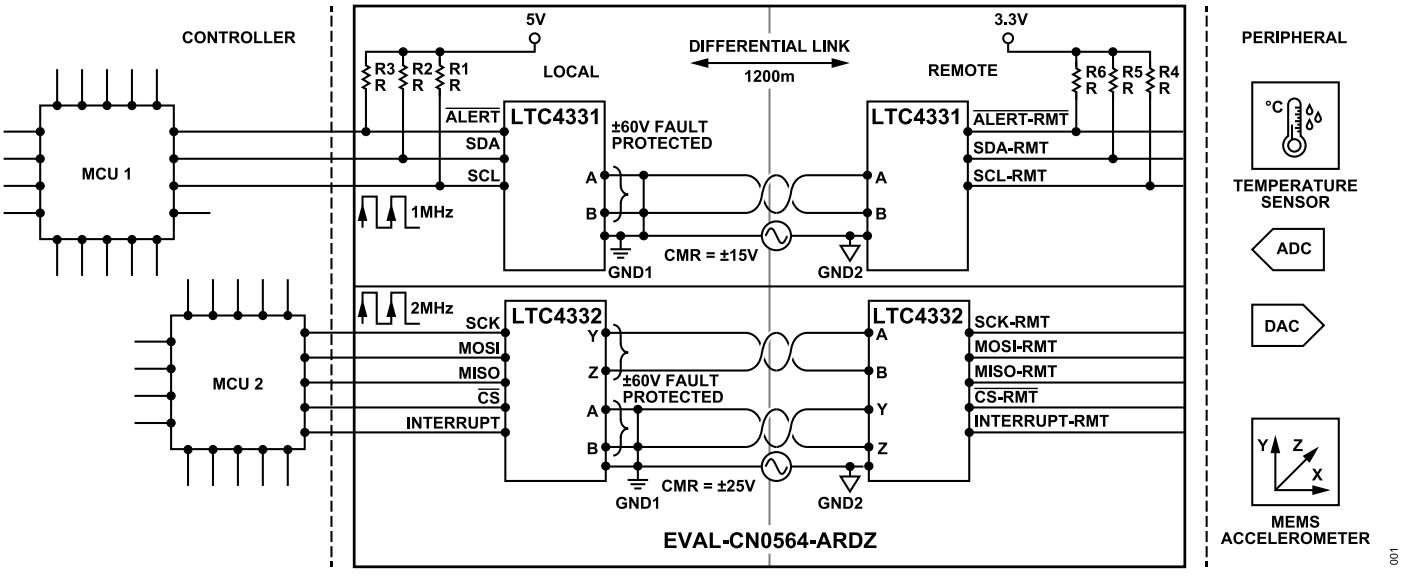

Figure 1. Simplified Block Diagram of EVAL-CN0564-ARDZ

CIRCUIT DESCRIPTION

I²C SIGNALING STANDARD SUMMARY

I²C is a serial protocol for a bidirectional two-wire interface to connect low speed devices like electrically erasable programmable read-only memory (EEPROM), analog-to-digital and digital-to-analog converters, input/output (I/O) interfaces, and other peripheral to an embedded processor. It is a very popular go-to for sensors because of its simplicity and expandability; multiple devices can exist on the bus, each with its own unique address. It requires just two wires to transfer data between devices. The two wires include:

- SCL - the serial clock signal line
- SDA - the serial data line for sending and receiving data between the controller and peripheral

The SCL and SDA signals are open drain logic, with logic levels and timing specifications defined in the I²C bus specification and user manual.

The number of peripheral devices, which can exist on a given I²C bus is limited by the address space and by the maximum total bus capacitance of 400 pF. The relatively high impedance and low noise immunity of open drain logic requires that all peripherals have a low impedance connection to a common ground return, and maximum bus length is restricted to approximately one meter at 100 kHz.

The CN0564 features differential transceivers that extend the length of the bus up to 1200 meters, and tolerate up to ±15 V common-mode difference between the controller and peripheral. The capacitances of the controller side and far side bus segments are isolated from each other and from the differential link, minimizing the impact on bus rise and fall times.

SDA is inherently bidirectional, with direction of data flow between controller and peripheral changing direction over the course of a transaction. I²C supports clock stretching where a peripheral device may hold SLCK low to slow down the clock rate. Thus, SCL is also bidirectional. The bidirectional nature of I²C makes it inconvenient to extend with buffers, isolate, or translate to other physical layers, requiring multiple logic levels and other nonstandard techniques. Analog Devices, Inc. also offers a suite of solutions that deal with bus buffer complexities.

Common I²C bus speeds are 100 kHz for standard mode (Sm) and 400 kHz for fast mode (Fm). The LTC4331 controller interface supports all common I²C clock rates up to 1000 kHz.

At low data rates and with short cables, latency is effectively transparent. At high clock frequencies and/or longer cable lengths, propagation delays begin to erode timing margin. The CN0564 is compatible with controllers that support clock stretching, which effectively slows down the clock frequency such that timing requirements are met, regardless of cable length.

SPI SIGNALING STANDARD SUMMARY

The SPI is a synchronous serial communication interface specification used for short-distance communication, primarily in embedded systems. Unlike I²C, SPI is not rigorously defined; a wide variety of clock frequencies, logic levels, and timing relationships are supported, requiring careful inspection of the controller and peripheral specifications. SPI is full-duplex communication, wherein data can flow from the controller to peripheral and vice versa, simultaneously.

The SPI physical layer typically consists of four signals:

- SCLK - serial clock, usually driven by the controller
- MISO - controller data input, peripheral data output
- MOSI - controller data output, peripheral data input
- $\overline{CS}$ - chip select enables communication with a peripheral. One $\overline{CS}$ line is required per peripheral device.

SPI pins use push-pull logic (rather than open drain), and the logic level between a controller and peripheral must match. Each peripheral device requires its own $\overline{CS}$ signal, further complicating physical extension of the SPI bus.

Four different timing relationships between clock and data are supported, referred to as modes 0, 1, 2, and 3 that correspond to the four possible clocking configurations. Each transaction begins when the chip select line is driven to logic low (chip select is typically an active-low signal). The exact relationship between the chip select, data, and clock lines depends on how the clock polarity (CPOL) and clock phase (CPHA) are configured. The four modes are summarized in Figure 2.

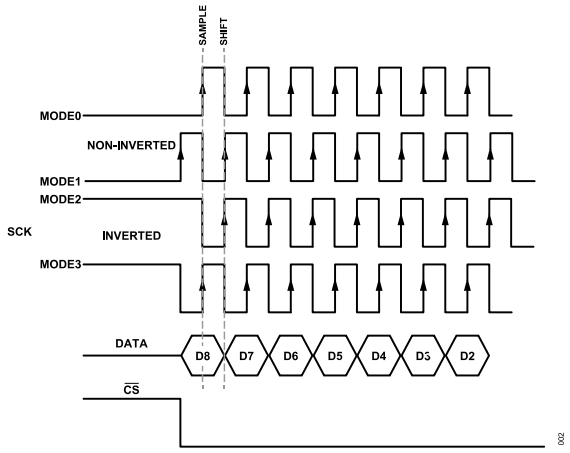

Figure 2. SPI Configuration Modes

The LTC4332 supports up to three remote peripherals, each with their own $\overline{CS}$ line. Each peripheral's SPI modes can be independently programmed to mode 0, 1, 2, or 3. The LTC4332 makes the extension of the SPI bus simple and requires only two twisted pairs to support the several signals. Data is transparently transmitted from the controller to the peripheral, however a one word delay is introduced in the data from peripheral to controller. Refer to the One Word Latency – SPI Read Command section for more details.

SYSTEM TOPOLOGY

The CN0564 uses the LTC4331 and LTC4332 to extend I²C and SPI signals up to 1200 m. Each link consists of a pair of devices, with the controller side configured in local mode (REMOTE pin tied low) and peripheral side device configured in remote mode (REMOTE pin tied high).

The LTC4331 and LTC4332 encode the SPI/I²C signals from the controller into differential signals, which are then transmitted through the twisted pair of cables. At the remote end of the cable, the differential signals are received by the remote LTC4331/LTC4332 and decoded back to SPI/I²C, which is then routed to the remote peripheral device. In normal operation, the remote peripheral device mirrors the events produced by the local controller.

SELECTABLE BAUD RATES

The LTC4331/LTC4332 can change its link baud rate, which is the speed at which data propagates between the local and the remote link using a selectable speed index, as shown in Table 1 & Table 2. This speed index is set by configuring the link and interface timing select pins, SPEED1 and SPEED2, which are both 3-state inputs.

Selectable baud rates over the cable allow balancing performance vs. cable length depending on the application requirements. However, both sides of the link must be set to the same speed configuration.

Table 1. Link Speed vs. Cable Length for LTC4331

Speed Index	Effective I²C Link Rate (kHz)	Max Cable Length (m)
8	1000	30
7	500	60
6	250	200
5	125	600
4	100	1200
3	63	1200+
2	31	1200+
1	20	1200+
0	12.5	1200+

Table 2. Link Speed vs. Cable Length for LTC4332

Speed Index	Max SCLK Frequency (kHz)	Max Cable Length (m)
8	2000	30
7	1000	60
6	500	150
5	250	250
4	125	500
3	83	750
2	63	1000
1	31	1200
0	25	1200+

INCREASED CABLE LENGTH TRANSMISSION

The LTC4332/LTC4331 utilize high speed differential transceivers to communicate over a link of up to 1200 meters in length. I²C/SPI signals are converted to differential signals for high speed, high quality signal transmission, noise immunity, as well as common mode rejection. For a given speed setting, cable length specifications provided in Table 1 for LTC4331 and Table 2 for LTC4332 must be adhered to or the link will not operate. The values in the table were recorded using a Category 5E (Cat5E) Ethernet cable in a lab environment. Note that the actual maximum cable length depends on type of cable and application environment.

COMMON-MODE VOLTAGE AND ESD ROBUSTNESS

The differential transceiver operates over an extended common mode range of ±25 V for SPI extenders and ± 15 V for I²C extenders, making it suitable for noisy environments or systems with ground potential differences (refer to Figure 1).

The interface pins (LTC4331 A&B pins, LTC4332 A, B, Y & Z pins) are fault protected to ±60 V. The interface pins also feature exceptionally robust electrostatic discharge (ESD) protection to ±40 kV human body model (HBM) ESD test with respect to GND and VCC (with a 4.7 µF capacitor to GND) without latch-up or damage, during all modes of operation, or while unpowered.

Both LTC4331/LTC4332 ESD results also survive the International Electrotechnical Commission (IEC) ESD and Electrical Fast Transient (EFT) tests. The IEC ESD stress exceeds that of the HBM test in peak current, amplitude, and rise time, while the EFT test provides a prolonged repetitive stress. This level of protection ensures that the LTC4331/LTC4332 are robust under a wide range of real world hazards.

ONE WORD LATENCY – SPI READ COMMAND

Propagation delay is also a concern for SPI communications, and limits the maximum bus speed when simultaneously reading and writing. The SPI extender solution deals with this issue by inserting one word of latency during read accesses only. Because the data sent from the SPI controller to the peripheral experiences the same delay as the controller-initiated interface clock (SLCK), both remain in sync across the entire data link.

In the opposite direction, the peripheral device sends MISO data to the controller only when the first clock edge reaches the peripheral device. This data experiences a second delay on its way back to the controller, so the MISO data is out of sync by twice the cable's propagation delay. Physically distant devices need a dramatically reduced clock rate to accommodate the propagation delay within each bit width. To overcome this limitation, the LTC4332 introduces a shift register into the MISO signal path, as shown in Figure 3.

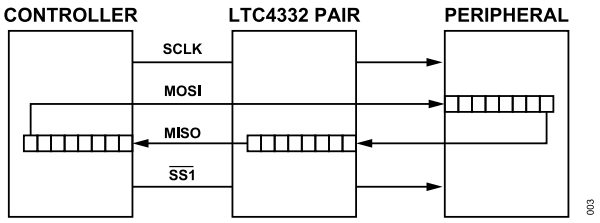

Figure 3. Shift Register Introduced into the MISO Signal Path to Accommodate the Propagation Delay

As a result, SPI write requests to remote peripheral devices are software transparent, but SPI read requests to remote peripherals incur a one word latency, meaning the read command needs to be extended by one word. If not, the last word is lost in the LTC4332 MISO shift register when the chip select is de-asserted. The WORD_LENGTH register (see the register map in the data sheet for LTC4332) indicative of the depth of the shift register in MISO signal path on LTC4332, dictates when the SPI controller begins receiving valid data on the MISO line. For example, if the WORD_LENGTH is 8, the user would begin receiving valid MISO data 8 clock cycles after $\overline{CS}$ is asserted.

FAULT MONITORING

The LTC4331/LTC4332 $\overline{LINK}$ pin indicates the state of the communication link, and is driven low to indicate that the remote I²C/SPI bus has joined the local I²C/SPI bus.

The LTC4331/LTC4332 support interrupt signals, $\overline{ALERT}$ on pin on the LTC4331 and $\overline{INT}$ on the LTC4332. These signals are mirrored from the remote bus to the local bus. On the remote end, the interrupt pins are inputs that can be connected to the interrupt output of the connected I²C/SPI peripheral. On the local side, $\overline{ALERT}/\overline{INT}$ operate as an open-drain output that can be connected to a shared local interrupt line. If enabled, the local LTC4331/LTC4332 control interface uses the $\overline{ALERT}/\overline{INT}$ pin to report link and fault events. The local side $\overline{ALERT}/\overline{INT}$ output is the logical AND of the remote $\overline{ALERT}/\overline{INT}$ and the internal endpoint interrupt signal.

The local side LTC4331/LTC4332 can also trigger a remote side reset by holding the ON pin low for a minimum of 180 ms. If the link is disconnected, the remote LTC4331/LTC4332 automatically resets after 180 ms. A remote reset disables all remote side outputs until link communication is re-established.

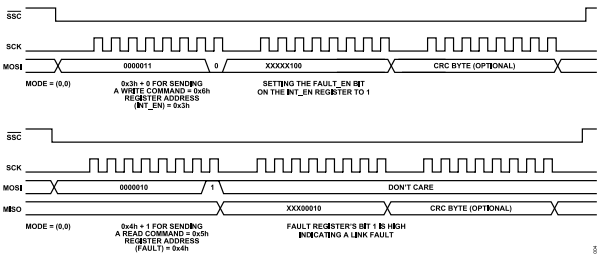

Figure 4. Control Interface Timing Diagram to Read/Write Fault Monitoring Registers

LTC4331/LTC4332 CONTROL INTERFACE

To configure the control interface on the local side of the LTC4331/LTC4332 link, a separate internal addressable peripheral is available. The internal interface on the local LTC4331 is assigned a unique I²C address by configuring the pins A1 and A2. The LTC4332 provides a separate chip select pin, $\overline{SSC}$, that allows a user to communicate with the internal SPI addressable registers.

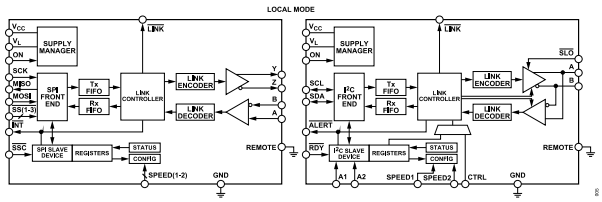

Figure 5. Internal Block Diagram of the LTC4332 (Left Side) and LTC4331 (Right Side)

The LTC4331/LTC4332 control interface allows the speed configuration, link status, and interrupt/alert status to be read, as well as additional I²C/SPI specific options to be accessed. The LTC4331 can be configured to translate the I²C address to the remote peripheral, expanding the I²C address space and preventing address conflicts. The LTC4332 allows independent SPI mode configuration for each CS pin, as well as the word length (which determines the received data latency). Refer to the LTC4331 and LTC4332 data sheet for more information.

PCB SIZE

Increased component density in printed circuit board (PCB) designs leads to complex problems. To encode SPI or I²C, an additional microcontroller is normally required, which increases both the solution cost and size. However, by using the CN0564, there is no requirement for an additional microcontroller on the remote side. This allows a smaller sensor solution to use up less area on the PCB, thus reducing the overall cost of manufacturing and leaving more room for other components for additional features.

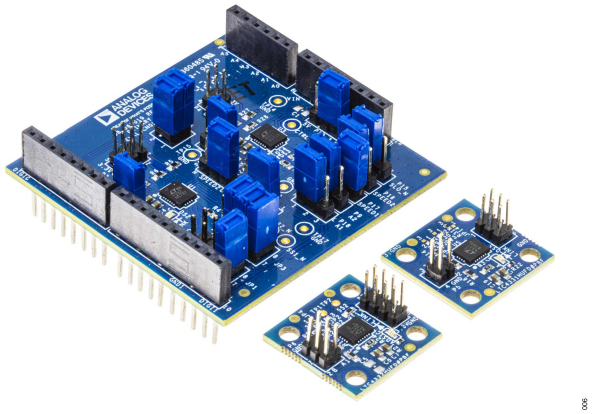

Figure 6. Local EVAL-CN0564-ARDZ Node and Remote Nodes of Both LTC4331 (I²C Extender) and LTC4332 (SPI Extender)

EXPANDING SENSOR INTERFACE CAPABILITIES

Sensor interfaces for longer distance transmission have traditionally used analog signaling techniques, such as 0 V to 10 V or 4 mA to 20 mA. For example, in condition monitoring applications, the integrated electronic piezoelectric (IEPE) sensor interface is the most common signaling standard used for vibration sensors. It supplies a constant current source to the vibration sensor, with the sensor output voltage read back on the same wire. This 2-wire system allows simpler system design when transmitting ac signal content, but provides no additional fault monitoring or configuration options.

The LTC4331/LTC4332 allow flexible configuration, processing, and easy debugging during fault events directly on the digital output sensors.

COMMON VARIATIONS

Galvanic isolation is required in situations wherein the potential difference between local and remote grounds exceeds the allowable ±15 V of the LTC4331 or ±25 V of the LTC4332. The I^2C/SPI signals can be galvanically isolated from the local LTC4331/LTC4332 on EVAL-CN0564-ARDZ using digital isolators such as the ADUM141E or ADUM140E, as shown in Figure 7.

An ADUM5020 provides up to 100 mA isolated power to the local LTC4331/LTC4332.

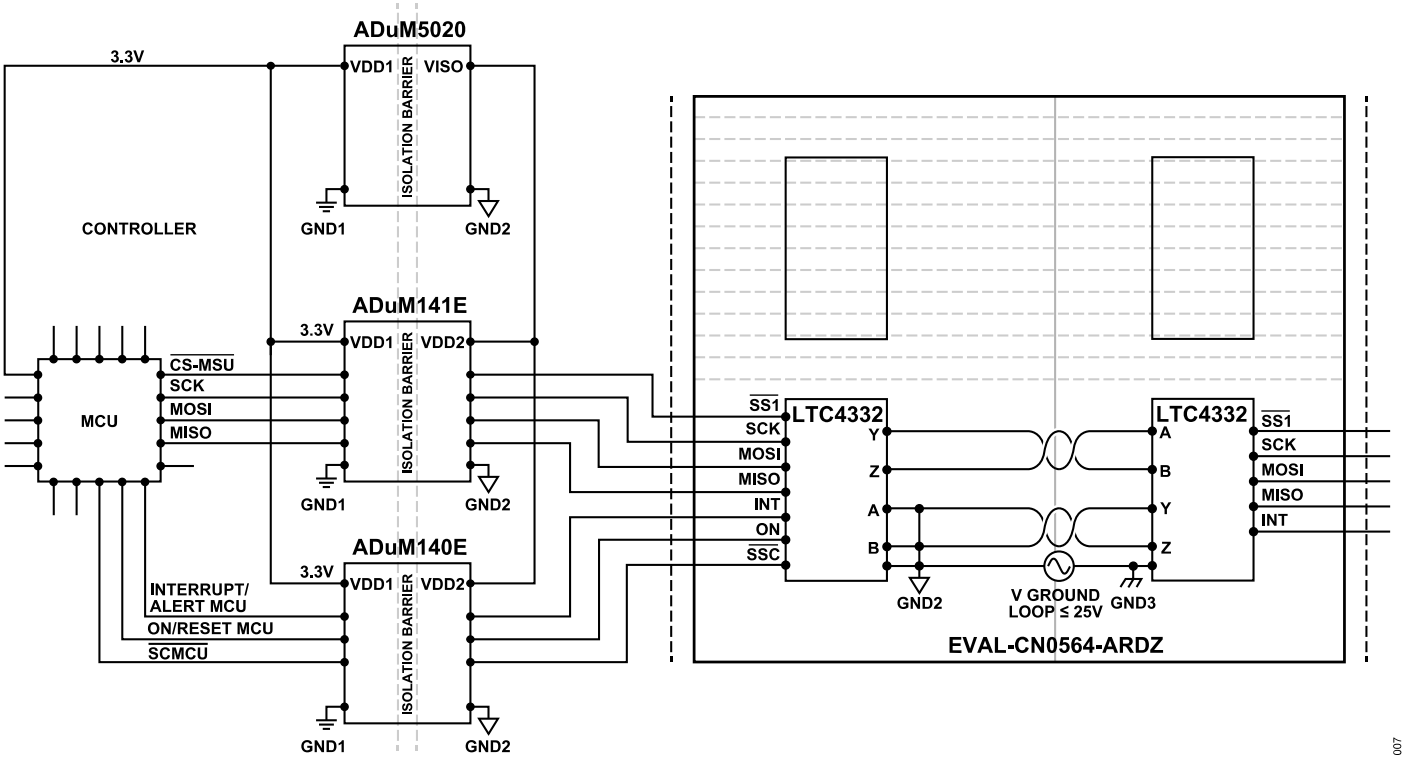

Figure 7. Block Diagram Containing Galvanic Isolation of the Data and Power Signals

CIRCUIT EVALUATION AND TEST

The following section describes how the CN0564 was set up and tested. The EVAL-CN0564-ARDZ can be used with an Arduino or other Arduino compatible devices to read acceleration data with EVAL-ADXL357 for easy evaluation of both its I²C (LTC4331) and SPI (LTC4332) extenders. The following section focuses on setting up the SPI extender (local and remote LTC4332) on the EVAL-CN0564-ARDZ.

For complete setup details and instructions on both the SPI and the I²C extender (local and remote LTC4331/LTC4332), visit the EVAL-CN0564-ARDZ User Guide.

EQUIPMENT NEEDED

- EVAL-CN0564-ARDZ circuit evaluation board
- EVAL-ADXL357
- EVAL-XLMOUNT1
- Arduino UNO Rev. 3
- PC with a USB port
- USB Type A to USB Type B cable
- Jumper wires
- 5 V or 3.3 V power supplies

GETTING STARTED

1. Download the Arduino sketch provided for evaluating either the SPI or the I²C extenders of the EVAL-CN0564-ARDZ and program the Arduino using it.
2. Plug in the EVAL-CN0564-ARDZ into the Arduino UNO Rev 3.
3. Connect the LTC4332 (remote side) on the EVAL-CN0564-ARDZ to the EVAL-ADXL357.
4. Connect the LTC4332 (local side) to the LTC4332 (remote side) using jumper wires in a twisted pair
5. Make the jumper connections as follows:
   a. Insert jumper P10, so Pin 2 and Pin 3 on P10 are connected on the EVAL-CN0564-ARDZ. This jumper placement selects the 5 V power supply option.
   b. Place jumper JP1 in position D to connect the Chip Select pin on the local LTC4332 to the D10 pin on the Arduino UNO Rev 3.
   c. Put jumper JP5 in position A to connect the $\overline{LINK}$ pin on the local LTC4332 to the D6 on the Arduino UNO Rev 3.
   d. Place jumper JP3 in position B to connect the interrupt pin on the local LTC4332 to the D2 on the Arduino UNO Rev 3.
   e. By default, speed index 8 is selected on the remote LTC4332. The speed index on the local side must be the same as the remote side.
   f. Place jumper P1 in the position, so its Pin 2 and Pin 3 are connected. Similarly, jumper P2 must also be placed in the position, so its Pin 2 and 3 are also connected. This configuration selects speed index 8 to match the speed index on the local side.
   g. Insert jumper P19, so its Pin 1 and 2 are connected. This connects the ON pin on the local LTC4332 to IOREF, and enables the input.

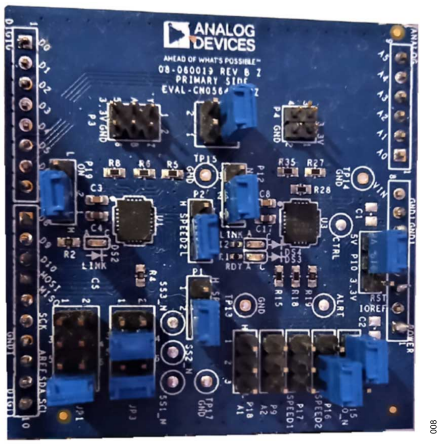

Figure 8. Jumper Configurations on the Local and Remote LTC4332

SYSTEM TESTING

Mount the EVAL-ADXL357 and the remote LTC4332 on the EVAL-XLMOUNT1, then turn on the power supplies that power up the boards. Three LEDs flash on the EVAL-CN0564-ARDZ board (2 LEDs on the local side, 1 on the remote side). See Figure 9 for the entire system block diagram.

The X, Y, and Z data read by the microelectromechanical system (MEMS) accelerometer (on the EVAL-ADXL357 from the remote side) is then printed on the Arduino serial monitor. Exit the Arduino serial monitor and run the Python Real Time ADXL357 Data Plotter Executable to see a real-time plot of the acceleration data like the graphs shown in Figure 10.

The X, Y, and Z acceleration (g) data is stored in three separate files by the python script and can be found in the same location containing the executable file.

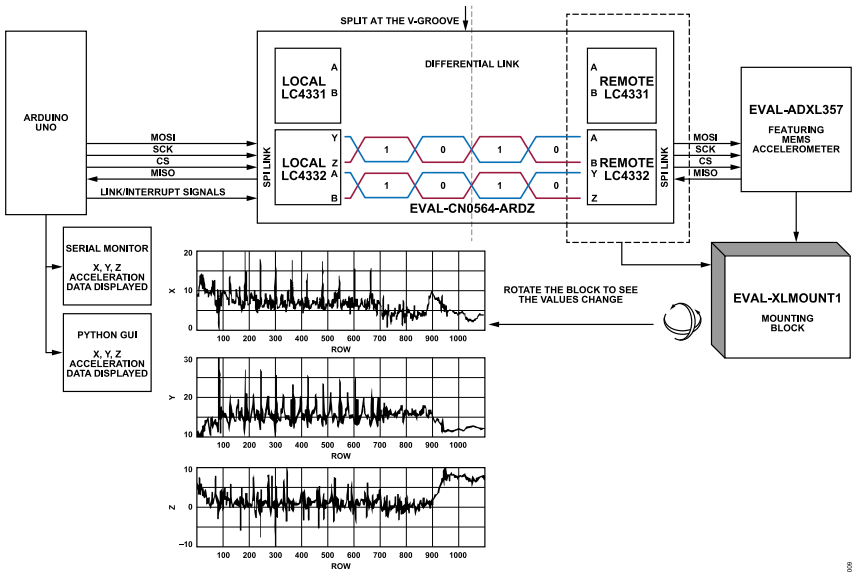

Figure 9. System Test Setup for the EVAL-CN0564-ARDZ Using ADXL357 and an Arduino UNO Rev 3

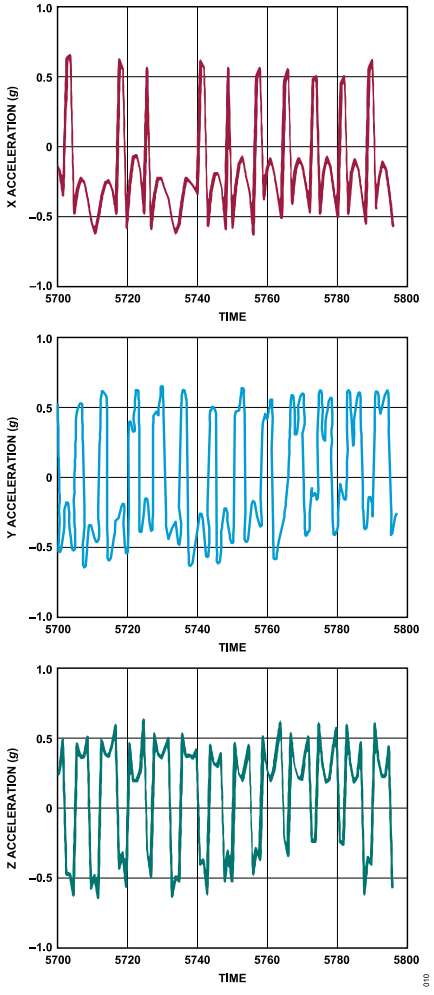

Figure 10. Real Time Plot of the Acceleration Data

A Fast Fourier Transform (FFT) analysis, shown in Figure 11, can also be obtained to identify frequencies of interest using the data obtained for X, Y, and Z. FFT analysis is often used to monitor the health of rotating parts. Predictive maintenance (PdM) is a key component of smart industry that involves monitoring equipment during operation to detect the early warning signs of potential failures. For more information on to how to analyze vibration data in condition-based monitoring (CbM) systems, refer to this article.

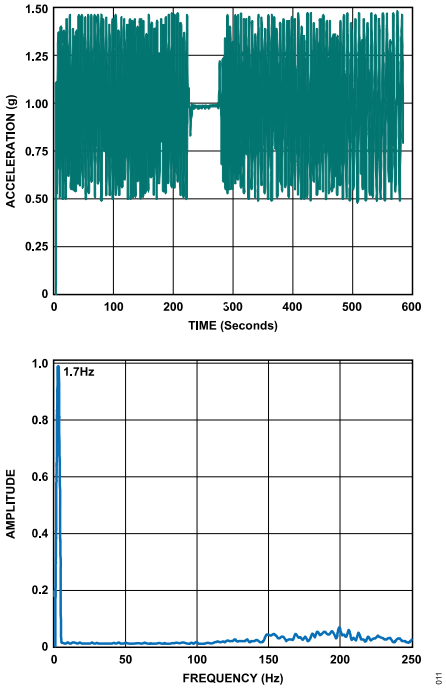

Figure 11. FFT Analysis on Acceleration Data Along the Z-Axis

LEARN MORE

Anslow, Richard. 2021. *Using LTspice for Engineered Power and MEMS Signal Chain Simulation*. Analog Devices.

Bramble, Simon. 2020. *Using LTspice to Analyze Vibration Data in Condition-Based Monitoring Systems*. Analog Devices

Functional SPI Isolation. Analog Devices

O'Brien, Maurice. 2014. *Designing Robust, Isolated I2C/PMBus Data Interfaces*. Analog Devices

LTspice® SPICE Simulation Software

Getting Started with Arduino products. Arduino.cc

DATA SHEETS AND EVALUATION BOARDS

CN0564 Evaluation Board

LTC4331 Data Sheet

LTC4331 Evaluation Board

LTC4332 Data Sheet

LTC4332 Evaluation Board

ADXL357 Data Sheet

EVAL-ADXL357 Evaluation Board

EVAL-XLMOUNT1 Evaluation Board

REVISION HISTORY

10/2022—Rev. 0 to Rev. A

10/2021—Revision 0: Initial Version