PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG/14/8597
Dated 17 Jul 2014

TO-220FP and DO-220FP Back-End line relocation from Longgang to Shenzhen (China)

Table 1. Change Implementation Schedule

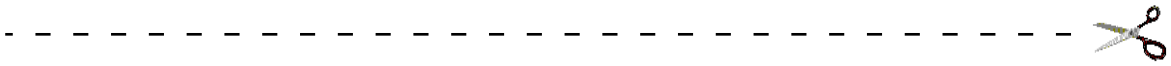
Forecasted implementation date for change	10-Jul-2014
Forecasted availability date of samples for customer	10-Jul-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	10-Jul-2014
Estimated date of changed product first shipment	16-Oct-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change, Testing location change
Reason for change	To improve service to ST Customers and standardize manufacturing processes
Description of the change	Following up on the plan already announced by our CEO over the consolidation of assembly and testing activities in Shenzhen (China), we're going to adopt Shenzhen (China) plant as main Assembly / Testing for TO-220FP and DO-220FP products. These packages have been produced for many years both in Longgang and Shenzhen plants with the same materials, equipment and processes, therefore products manufactured in Shenzhen (China) guarantee the same quality and electrical characteristics as reported in the relevant datasheets.
Change Product Identification	"GK" marked on the package
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG/14/8597**
Please sign and return to STMicroelectronics Sales Office	**Dated 17 Jul 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Giuffrida, Antonino	Marketing Manager
Martelli, Nunzio	Product Manager
Vitali, Gian Luigi	Q.A. Manager

WHAT:

Following up on the plan already announced by our CEO over the consolidation of assembly and testing activities in Shenzhen (China), we're going to adopt Shenzhen (China) plant as main Assembly / Testing for TO-220FP and DO-220FP products.
These packages have been produced for many years both in Longgang and Shenzhen plants with the same materials, equipment and processes, therefore products manufactured in Shenzhen (China) guarantee the same quality and electrical characteristics as reported in the relevant datasheets.

For the complete list of the part numbers affected by this change, please refer to the attached Products List.

Samples, of the test vehicles manufactured in the ST plant of Shenzhen are available under 1 month upon request for customer qualification, while the full availability of products will be granted from wk 30 2014 onwards. Any other sample for granting customer's qualification will be supported upon request.

WHY:

To improve service to ST Customers and optimize manufacturing processes.

HOW:

By transferring the existing equipment from the Longgang ST plant, to the ST Shenzhen assembly and testing premises.

The change here reported will not affect the electrical, dimensional and thermal parameters.
There is as well neither modification in the packing mode or in the standard delivery quantities.

Qualification program and results:

The qualification program consists in a full set of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

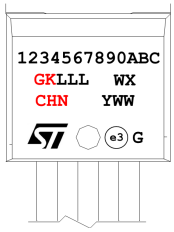
WHEN:

Production start and first shipments will occur as per the scheduling indicated in the tables below.

Affected Product Types	Samples	1st Shipment
Power MOSFET	**Wk 30**	**Wk 41**
IGBT	**Wk 30**	**Wk 41**
Power Bipolar	**Wk 30**	**Wk 41**
Voltage Regulator	**Wk 30**	**Wk 41**
Thyristor	**Wk 30**	**Wk 41**
Rectifier	**Wk 30**	**Wk 41**

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts produced in ST Shenzhen will be ensured by the Q.A. number and plant code identification “GK” marked on the package, as illustrated in the below picture:



Package marking example

Reliability Report – *INTERIM Results and PLAN*

TO-220FP and DO-220FP Back-End line relocation from Longgang to Shenzhen (China).

General Information	
Product Lines:	VJ8L - EZ62 - MD87 - MQ6H - KV65+E03I - EVFE+D39B
Product Families:	Power MOSFET IGBT
P/Ns:	STF25N80K5 (VJ8L) STP4NK60ZFP (EZ62) STF11NM80 (MD87) STF24N60M2 (MQ6H) STGF19NC60KD (KV65+E03I) STGF20V60DF (EVFE+D39B)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	TO-220FP
Silicon Process techn.:	SuperMESH™K5 Power MOSFET MDmesh™ II Power MOSFET IGBT Trench

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (Singapore)* *Catania (Italy)*
EWS Plants:	*Ang Mo Kio (Singapore)* *Catania (Italy)*
Assembly and testing plant:	*ST Shenzhen (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July 2014	11	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for assembling and testing TO-220FP and DO-220FP Back-End line relocation from Longgang to Shenzhen (China)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET
IGBT

4.2 Construction note

D.U.T.: STF25N80K5 LINE: VJ8L PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	SuperMESH™K5 Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	6830 x 5060 μm^2
Metal	AlCu
Passivation type	TEOS/Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTEST

D.U.T.: STP4NK60ZFP LINE: EZ62 PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	SuperMESH™K5 Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3186 x 2654 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Cu Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTEST

D.U.T.: STF11NM80 LINE: MD87 PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	5710 x 4610 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTEST

D.U.T.: STF24N60M2 LINE: MQ6H PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	4400 x 3840 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTEST

D.U.T.: STGF19NC60KD LINE: KV65 PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	IGBT Trench
Die finishing back side	Chromium/Nickel/Silver
Die size	3520 x 4600 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTEST

D.U.T.: STGF20V60DF LINE: EVFE PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	IGBT Trench
Die finishing back side	Al/Ti/NiV/Ag
Die size	3520 x 3580 µm^2
Metal	AlCu/w
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IPTEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STF25N80K5	VJ8L	Power MOSFET
2	STP4NK60ZFP	EZ62	Power MOSFET
3	STF11NM80	MD87	Power MOSFET
4	STF24N60M2	MQ6H	Power MOSFET
5	STGF19NC60KD	KV65+E03I	IGBT
6	STGF20V60DF	EVFE+D39B	IGBT

5.2 Reliability test plan summary

Test	Std ref.	Conditions	SS	Steps	Failure/SS					
					LOT1	LOT2	LOT3	LOT4	LOT5	LOT6
Die Oriented Tests										
HTRB	JESD22 A-108	TA = 150°C BIAS=500V	50 x 6 lots	168 H	0/50	0/50	***wk28***	***wk28***	0/50	0/50
				500 H	***run***	***run***	***run***	***run***	***run***	***run***
				1000 H	***wk30***	***wk30***	***wk34***	***wk34***	***wk30***	***wk33***
HTGB	JESD22 A-108	TA = 150°C BIAS=20V	50 x 6 lots	168 H	0/50	0/50	***wk28***	***wk28***	0/50	0/50
				500 H	***run***	***run***	***run***	***run***	***run***	***run***
				1000 H	***wk30***	***wk30***	***wk34***	***wk34***	***wk30***	***wk33***
Package Oriented Tests										
AC	JESD22 A-102	Pa=2Atm / TA=121°C	50 x 6 lots	96 H	0/50	0/50	***wk28***	***wk28***	0/50	0/50
TC	JESD22 A-104	TA = -65°C/150°C	50 x 6 lots	100 cy	0/50	0/50	***wk28***	***wk28***	0/50	0/50
				200 cy	***run***	***run***	***run***	***run***	***run***	***run***
				500 cy	***wk30***	***wk30***	***wk33***	***wk33***	***wk30***	***wk31***
TF/IOL	Mil-Std 750D Method 1037	ΔTC=105°C	25 x 6 lots	5Kcy	0/25	0/25	***Wk28***	***Wk28***	0/25	0/25
				10Kcy	***wk28***	***wk28***	***wk31***	***wk31***	***wk28***	***Wk29***
H3TRB	JESD22 A-101	TA=85°C , RH=85% BIAS=100V	50 x 6 lots	168 H	0/50	0/50	***wk28***	***wk28***	0/50	0/50
				500 H	***run***	***run***	***run***	***run***	***run***	***run***
				1000 H	***wk30***	***wk30***	***wk34***	***wk34***	***wk30***	***wk33***

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Reliability Report

Qualification of TO-220FP and DO-220FP Back-End line relocation from Longgang to Shenzhen (China)

General Information	
Product Line	*Rectifiers & AC Switch-Thyristor*
Product Description	*Planar products*
Product Group	*IPG*
Product division	*ASD&IPAD*
Package	*TO-220FP/ DO-220FP*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST TOURS (FRANCE)* *ST ANG MO KIO (SINGAPORE)*
Assembly plant	*ST SHENZHEN (CHINA)*
Reliability Lab	*ST TOURS (FRANCE)*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	04/07/2014	6	Aude DROMEL	Gilles DUTRANNOY	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
IOLT	Intermittent Operating Life Test
PCT	Pressure Cooker Test (Autoclave)

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the assembly and testing activities in ST plant of Shenzhen for the rectifiers and AC Switch products in TO-220FP and DO-220FP packages. These packages have been produced for many years both in Longgang and Shenzhen plants with the same materials, equipment and processes, therefore products manufactured in Shenzhen (China) guarantee the same quality and electrical performances.

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology » and is package oriented.

The following reliability tests are:

.

- TC to ensure the mechanical robustness of the products.
- uHAST to check the robustness to corrosion and the good package hermeticity.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Devices descriptions

TO-220FP

DO-220FP

4.2 Construction Note

	Rectifiers and AC Switch in TO/DO-220FP
Wafer/Die fab. information	
Wafer fab manufacturing location	ST AMK – SINGAPORE & ST TOURS -FRANCE
Technology / Process family	PLANAR
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST AMK – SINGAPORE & ST TOURS -FRANCE
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO 220 ISOL FULL PACK & DO 220 ISOL FULL PACK
Molding compound	ECOPACK®2 (“Halogen-free”)
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN -CHINA

Tests results SUMMARY

4.3 Test vehicle

Lot #	Part Number	Package	Technology family	Comments
L1	PS30H60CFP	TO-220FP	Power Schottky	Planar die technology in qualified package

Detailed results in below chapter will refer to these references.

4.4 Test plan and results summary

Test	Std ref.	Conditions	SS	Steps / duration	Failure/SS
					L1
TC	JESD22 A-104	-65 / +150°C 2 cycles/hour	75	500cy	0/75
uHAST	JESD22-A118	130°C 2.3bar 85% RH	25	96h	0/25

ANNEXES: Tests description

Test name	Description	Purpose
Package Oriented		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Reliability Evaluation Report

TO-220FP Back-End line relocation from Longgang to Shenzhen (China).

TVs: L7805, LM317

General Information	
Product Line	*L317* *LX05*
Product Group	*IPG*
Product division	*IPC* Linear Voltage Regulators & Vref
Package	*TO220FP* *Cu Wire*
Silicon Process technology	*LM317 in BIP (>6um)* *L7805 in HBIP40*

Locations	
Wafer fab	*BIP (>6um) – AMK6* *HBIP40 - AMK6*
Assembly plant	*ST SHENZHEN (CHINA)*
Reliability Lab	*IPG Catania* *Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July 2014	6	Cesario De Luca	Giovanni Presti	Preliminary report

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 RELIABILITY EVALUATION PLAN

2.1 Objectives

Relocation Plan from Longgang to Shenzhen (China) for the package TO220FP.

TV1: LM317 in BIP (>6um)

TV2: L7805 in HBIP40

2.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

3 DEVICE CHARACTERISTICS

3.1 Device description

LM317: ADJ. POS. VR @1.5A

L7805: POSITIVE VR 1.5A 5V

4 CONSTRUCTION NOTE

4.1 Construction note

Lot 1	**P/N:** L7805CP$5Z
Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6
Technology	HBIP40V
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die finish front	P-VAPOX/NITRIDE
Die size	1320 x 1630 micron
Assembly information	
Assembly site	ST SHENZHEN
Package description	TO 220 ISOL FULL PACK
Molding Compound	HF Epoxy Resin
Frame Material	Bare copper
Die attach material	Pb/Ag/Sn
Wire bonding	Cu D2
Final testing information	
Testing location	ST SHENZHEN
Tester	QT200

Lots 2, 3	**P/N:** LM317P/4ZM
Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6
Technology	BIP (>6um)
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die finish front	SiN (nitride)
Die size	2410 x 1920 micron
Assembly information	
Assembly site	ST SHENZHEN
Package description	TO 220 ISOL FULL PACK
Molding Compound	HF Epoxy Resin
Frame Material	Bare copper
Die attach material	Pb/Ag/Sn
Wire bonding	Cu D2
Final testing information	
Testing location	ST SHENZHEN
Tester	QT200

5 SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Technology	Package	FG	Comments
1	63521HL	GK4190S804	HBIP40	TO 220 ISOL FULL PACK Cu wire	L7805CP$5Z	
2	63330YV	GK41920301	BIP (>6um)		LM317P/4ZM	
3	6338NV1	GK41920401			LM317P/4ZM	

5.2 Test plan and Results

Test		Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
						LX05	L317	L317	
Die Oriented Tests									
HTOL		JESD22 A-108	Tj = 125°C, BIAS= 35V		168 H	0/77		0/77	
					500 H	run		run	
					1000 H				
HTSL		JESD22 A-103	Ta = 150°C		168 H	0/25	0/25	0/25	
					500 H	run	run	run	
					1000 H				
Package Oriented Tests									
AC		JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/25	0/25	0/25	
TC		JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	0/25	0/25	
					200 cy	run	run	run	
					500 cy				
THB		JESD22 A-101	Ta = 85°C, RH = 85%, BIAS= 24V		168 H	0/25	0/25	0/25	
					500 H	run	run	run	
					1000 H				
Other Tests									
ESD		ANSI/ESD S5.3.1	CDM		+/- 500V	0/3		0/3	

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.

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