



Click [here](#) for the 3D model.

### Dimensions

D	6.35mm +/-0.635mm
L	6.35mm MIN
H	2.54mm NOM
F	1.397mm +/-0.25mm
A	5.3mm MAX
B	7.078mm MAX
C	6.35mm +/-0.635mm
E	7.62mm MAX
K	0.5mm NOM

### Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	50

### General Information

Series	KPS-MCC Indust COG HT200C
Style	Leaded Stacked Chip
Description	Low ESR, Stacked Ceramic Chips
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance
RoHS	With Exemptions
REACH	SVHC (Pb - CAS 7439-92-1)
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24
Termination	Silver
Lead	Straight Leads
AEC-Q200	No
Notes	Number of chips in this stack: 2.

### Specifications

Capacitance	0.013 uF
Capacitance Tolerance	10%
Voltage DC	1500 VDC
Dielectric Withstanding Voltage	1800 VDC
Temperature Range	-55/+200°C
Temperature Coefficient	COG
Dissipation Factor	0.1% 1 kHz 25C
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	76.92 GOhms