

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^c	Q_g (Typ.)
- 20	0.140 at $V_{GS} = - 4.5$ V	- 2.1	4 nC
	0.160 at $V_{GS} = - 3.6$ V	- 1.9	
	0.222 at $V_{GS} = - 2.5$ V	- 1.6	

FEATURES

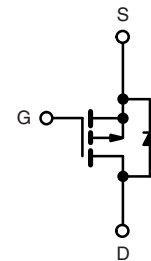
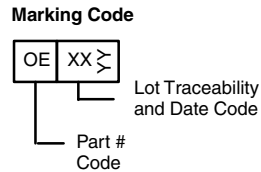
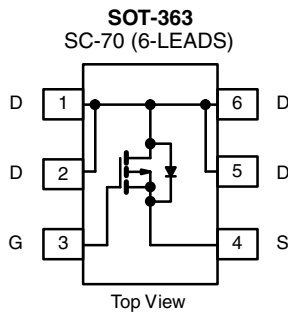
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch for Portable Devices
- DC/DC Converters



Ordering Information: Si1403CDL-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 20	V	
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	- 2.1	A
		$T_C = 70$ °C	- 1.6	
		$T_A = 25$ °C	- 1.6 ^{a, b}	
		$T_A = 70$ °C	- 1.3 ^{a, b}	
Pulsed Drain Current (10 μ s Pulse Width)	I_{DM}	- 5		
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	- 1.75	
		$T_A = 25$ °C	- 0.5 ^{a, b}	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	0.9	W
		$T_C = 70$ °C	0.6	
		$T_A = 25$ °C	0.6 ^{a, b}	
		$T_A = 70$ °C	0.4 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, d}	R_{thJA}	180	220	°C/W	
Maximum Junction-to-Foot (Drain)	R_{thJF}	115	140		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- Based on $T_C = 25$ °C.
- Maximum under steady state conditions is 230 °C/W.

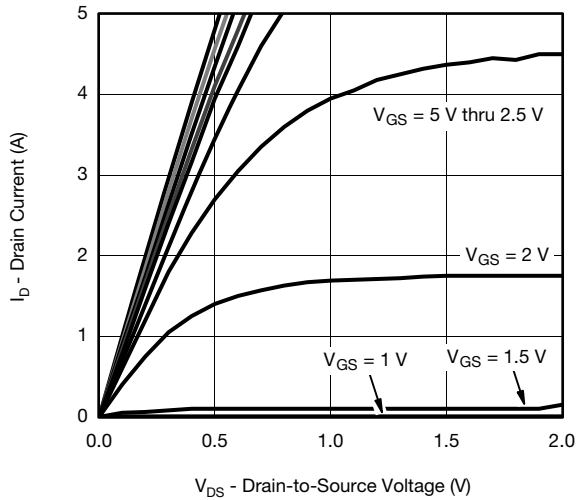
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-15		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.6		-1.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = -4.5\text{ V}$	-2			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}$		0.116	0.140	Ω
		$V_{GS} = -3.6\text{ V}, I_D = -1.5\text{ A}$		0.133	0.160	
		$V_{GS} = -2.5\text{ V}, I_D = -0.5\text{ A}$		0.177	0.222	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -1.6\text{ A}$		5		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		281		μF
Output Capacitance	C_{oss}			73		
Reverse Transfer Capacitance	C_{rss}			54		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}$		4	8	nC
Gate-Source Charge	Q_{gs}			0.7		
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_g	$f = 1\text{ MHz}$	2	7	14	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 7.7\text{ }\Omega$ $I_D \cong -1.3\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		18	27	ns
Rise Time	t_r			17	26	
Turn-Off Delay Time	$t_{d(off)}$			19	30	
Fall Time	t_f			9	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 7.7\text{ }\Omega$ $I_D \cong -1.3\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			17	26	
Fall Time	t_f			7	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-1.75	A
Pulse Diode Forward Current	I_{SM}				-5	
Body Diode Voltage	V_{SD}	$I_S = -1.3\text{ A}, V_{GS} = 0\text{ V}$		-0.83	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		12	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			4	8	nC
Reverse Recovery Fall Time	t_a			7		ns
Reverse Recovery Rise Time	t_b			5		

Notes:

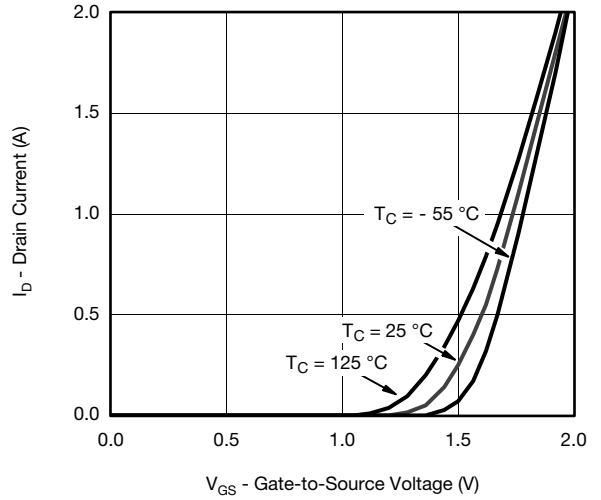
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

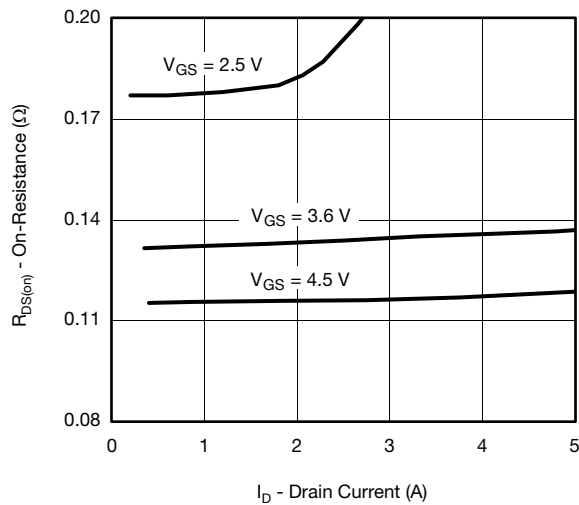
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



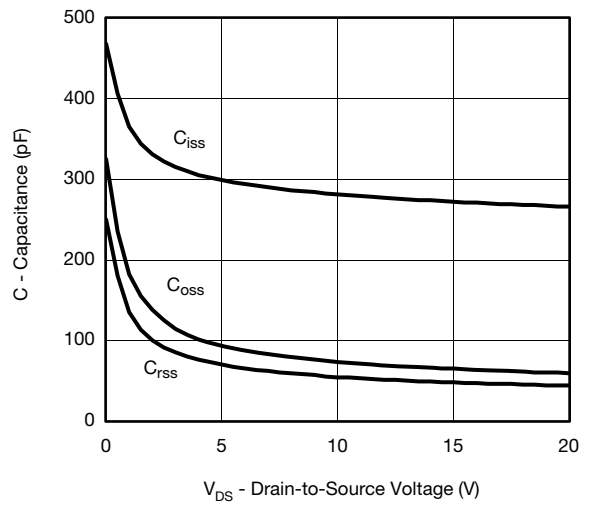
Output Characteristics



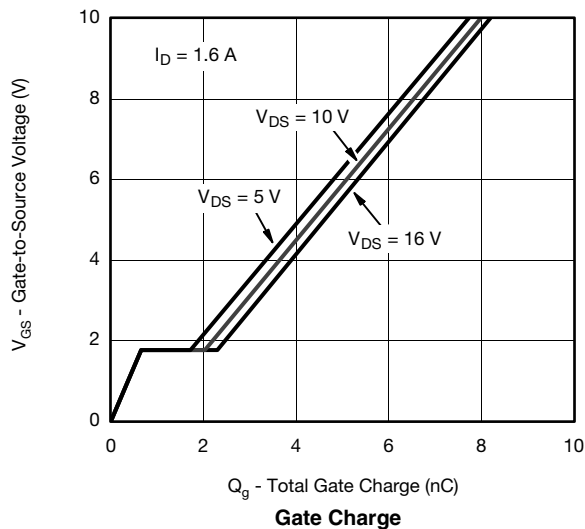
Transfer Characteristics



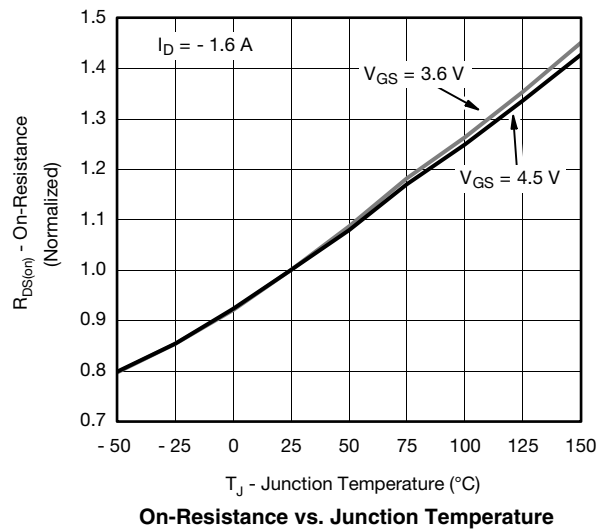
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

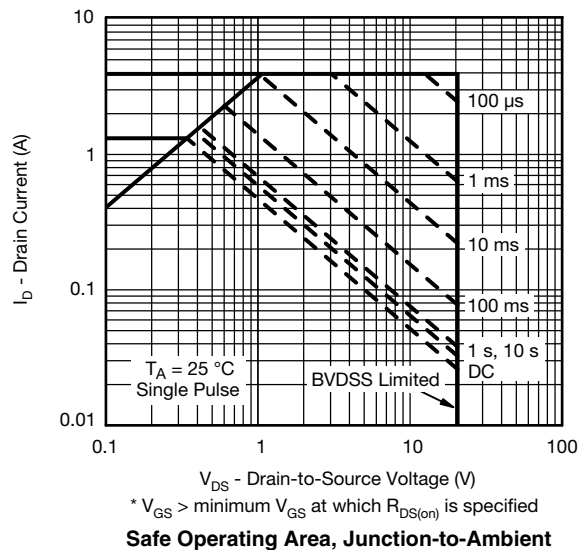
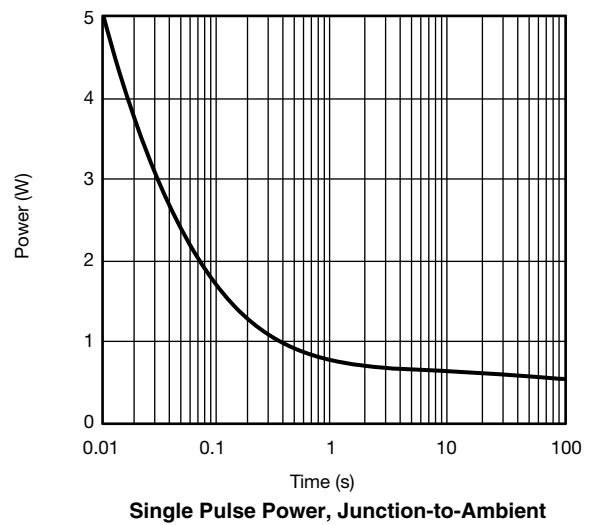
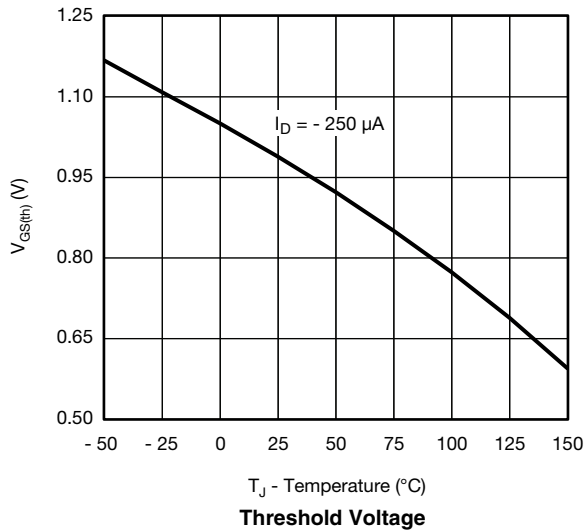
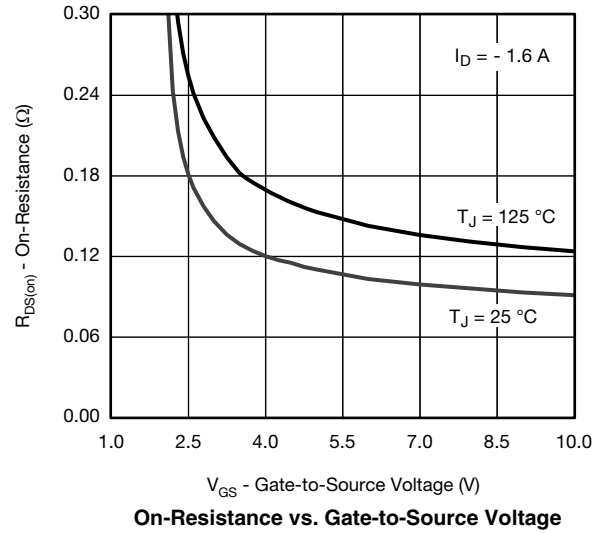
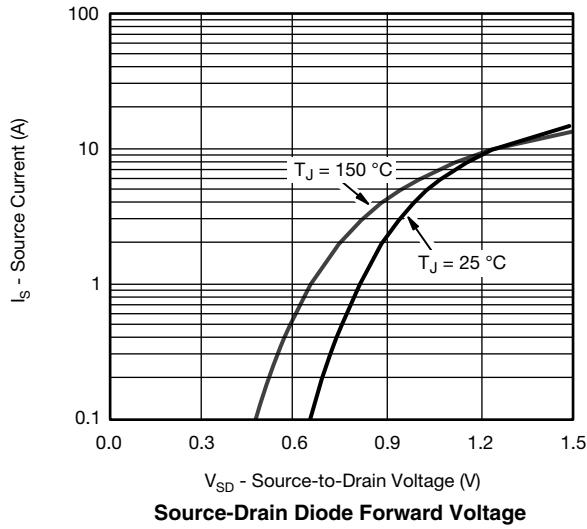


Gate Charge

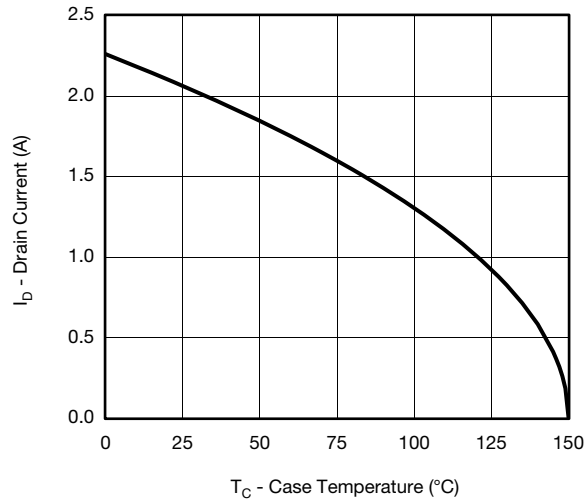


On-Resistance vs. Junction Temperature

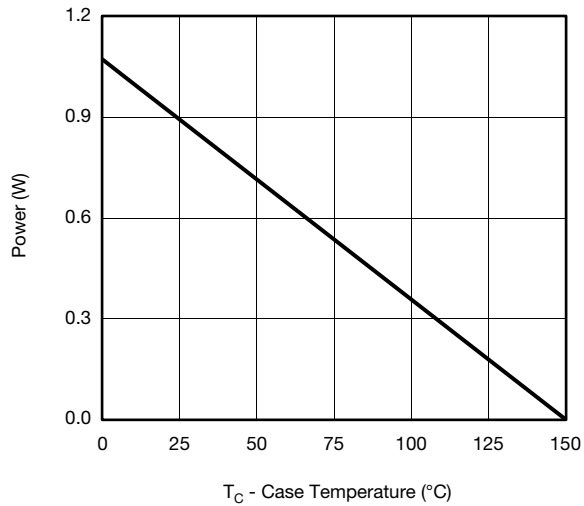
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



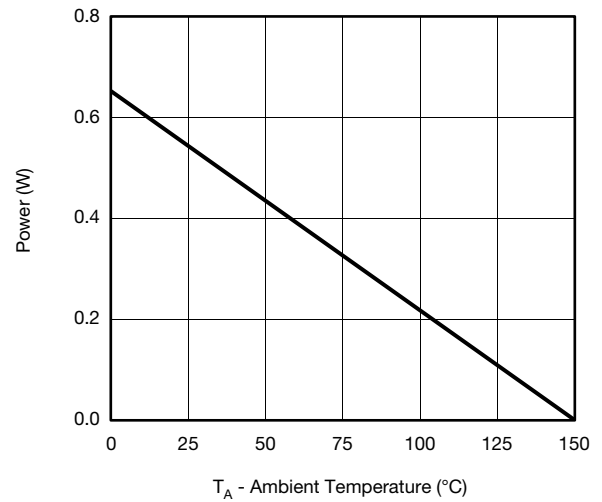
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



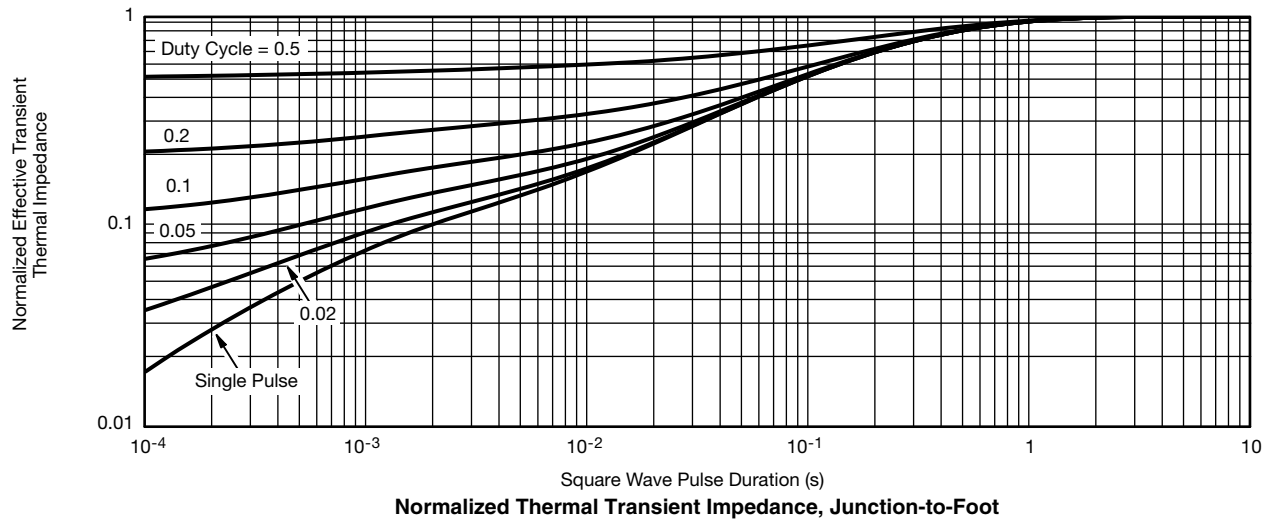
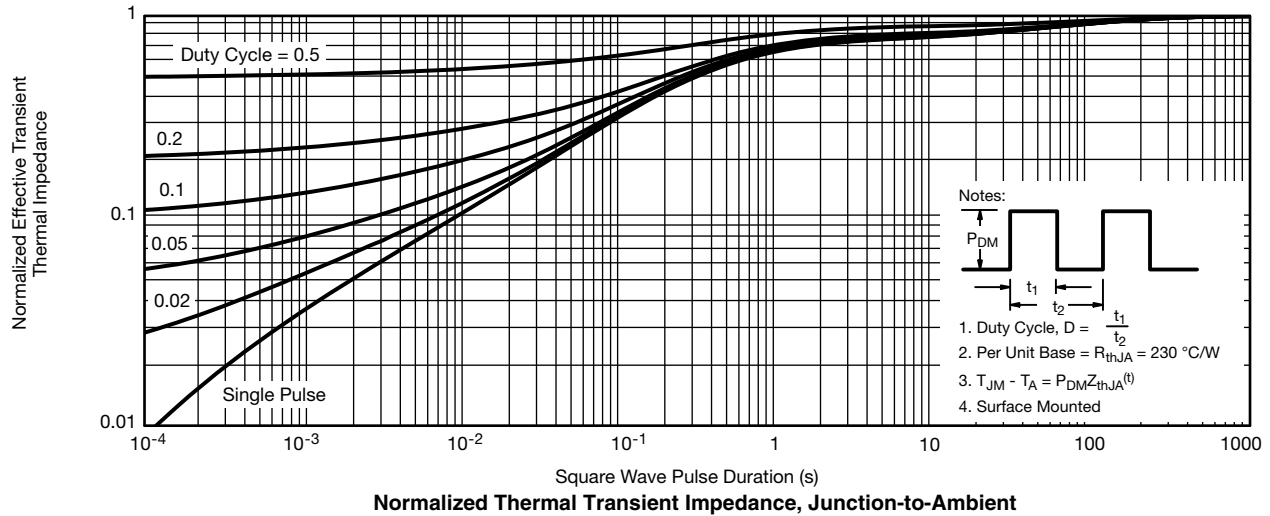
Power Derating, Junction-to-Foot



Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67093.



SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A ₁	-	-	0.10	-	-	0.004
A ₂	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Single-Channel LITTLE FOOT® SC-70 3-Pin and 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for single-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 350 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these single devices with a range of on-resistance specifications and in both traditional 3-pin and new 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance compared to the 3-pin package.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the single-channel SC-70 device in both 3-pin and 6-pin configurations. The pin-out of the 6-pin device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

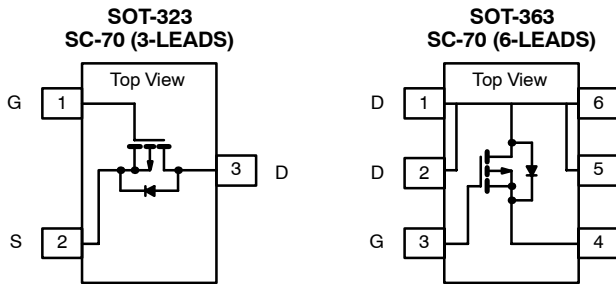


FIGURE 1.

For package dimensions see outline drawings:
 SC-70 (3-Leads) (<http://www.vishay.com/doc?71153>)
 SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the basic pad layout and dimensions for the 3-pin SC-70 and the 6-pin SC-70. These pad patterns are sufficient for the low-power applications for which this package is intended. Increasing the pad pattern has little effect on thermal resistance for the 3-pin device, reducing it by only 10% to 15%. But for the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 35% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB). The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

EVALUATION BOARDS FOR THE SINGLE SC70-3 AND SC70-6

Figure 2 shows the 3-pin and 6-pin SC-70 evaluation boards (EVB). Both measure 0.6 inches by 0.5 inches. Their copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. Both boards allow interrogation from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the single SC-70 has been measured on the EVB for both the 3-pin and 6-pin devices, the results shown in Figures 3 and 4. The minimum recommended footprint on the evaluation board was compared with the industry standard of 1-inch square FR4 PCB with copper on both sides of the board.

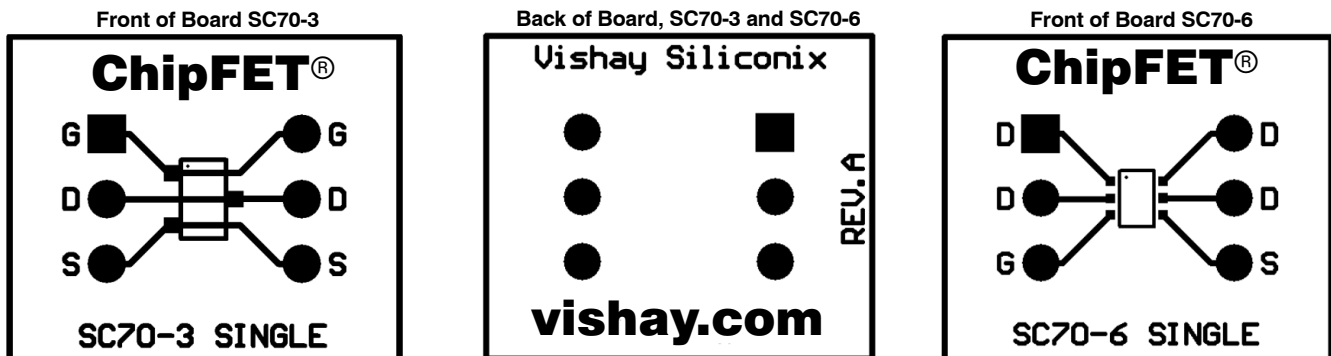


FIGURE 2.

Vishay Siliconix

THERMAL PERFORMANCE

**Junction-to-Foot Thermal Resistance
(the Package Performance)**

Thermal performance for the 3-pin SC-70 measured as junction-to-foot thermal resistance is 285°C/W typical, 340°C/W maximum. Junction-to-foot thermal resistance for the 6-pin SC70-6 is 105°C/W typical, 130°C/W maximum — a nearly two-thirds reduction compared with the 3-pin device. The “foot” is the drain lead of the device as it connects with the body. This improved performance is obtained by the increase in drain leads from one to four on the 6-pin SC-70. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

**Junction-to-Ambient Thermal Resistance
(dependent on PCB size)**

The typical $R\theta_{JA}$ for the single 3-pin SC-70 is 360°C/W steady state, compared with 180°C/W for the 6-pin SC-70. Maximum ratings are 430°C/W for the 3-pin device versus 220°C/W for the 6-pin device. All figures are based on the 1-inch square FR4 test board. The following table shows how the thermal resistance impacts power dissipation for the two different pin-outs at two different ambient temperatures.

SC-70 (3-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{360^\circ\text{C/W}}$	$P_D = \frac{150^\circ\text{C} - 60^\circ\text{C}}{360^\circ\text{C/W}}$
$P_D = 347 \text{ mW}$	$P_D = 250 \text{ mW}$

SC-70 (6-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{180^\circ\text{C/W}}$	$P_D = \frac{150^\circ\text{C} - 60^\circ\text{C}}{180^\circ\text{C/W}}$
$P_D = 694 \text{ mW}$	$P_D = 500 \text{ mW}$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.5 W.

Testing

To aid comparison further, Figures 3 and 4 illustrate single-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state and produce a graphic account of the thermal performance variation between the two packages. The measured steady state values of $R\theta_{JA}$ for the single 3-pin and 6-pin SC-70 are as follows:

LITTLE FOOT SC-70	3-Pin	6-Pin
1) Minimum recommended pad pattern (see Figure 4) on the EVB.	410.31°C/W	329.7°C/W
2) Industry standard 1" square PCB with maximum copper both sides.	360°C/W	211.8°C/W

The results show that designers can reduce thermal resistance $R\theta_{JA}$ on the order of 20% simply by using the 6-pin device rather than the 3-pin device. In this example, a 80°C/W reduction was achieved without an increase in board area. If increasing board size is an option, a further 118°C/W reduction could be obtained by utilizing a 1-inch square PCB area.



FIGURE 3. Comparison of SC70-3 and SC70-6 on EVB



FIGURE 4. Comparison of SC70-3 and SC70-6 on 1" Square FR4 PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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