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Kind regards,

Team Nexperia



# PESD5V0V1USF

Very low capacitance unidirectional ESD protection diode

Rev. 1 — 16 July 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Very low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is encapsulated in a leadless super small DSN0603-2 (SOD962) Surface-Mounted Device (SMD) package.

### 1.2 Features and benefits

- ESD protection of one line
- Low diode capacitance  $C_d = 4$  pF
- Super small SMD package
- Ultra low leakage current  $I_{RM} < 1$  nA
- ESD protection up to 12 kV
- IEC 61000-4-2; level 4 (ESD)

### 1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics

### 1.4 Quick reference data

Table 1. Quick reference data


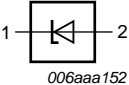
$T_{amb} = 25$  °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage		-	-	5	V
$C_d$	diode capacitance	$f = 1$ MHz; $V_R = 0$ V	-	4	5	pF



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	cathode <a href="#">[1]</a>	 <p>Transparent top view</p>	 <p>006aaa152</p>
2	anode		

[1] The marking bar indicates the cathode.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PESD5V0V1USF	DSN0603-2	leadless ultra small package; 2 terminals; body 0.6 × 0.3 × 0.3 mm	SOD962

## 4. Marking

**Table 4. Marking code**

Type number	Marking code
PESD5V0V1USF	3

## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-55	+150	°C
$T_{stg}$	storage temperature		-65	+150	°C

**Table 6. ESD maximum ratings**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

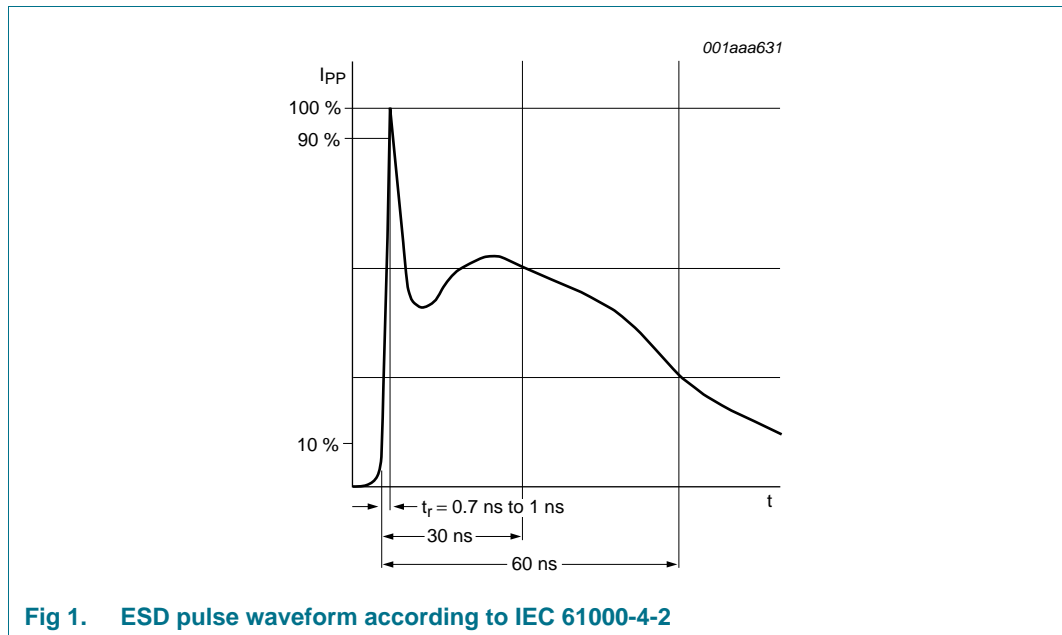
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	-	12 kV
		IEC 61000-4-2 (air discharge)	[1][2]	-	12 kV
		machine model	[2]	-	400 V
		MIL-STD-883 (human body model)		-	10 kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to pin 2.

**Table 7. ESD standards compliance**

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 8 kV (contact)
MIL-STD-883; class 3B (human body model)	> 8 kV



**Fig 1. ESD pulse waveform according to IEC 61000-4-2**

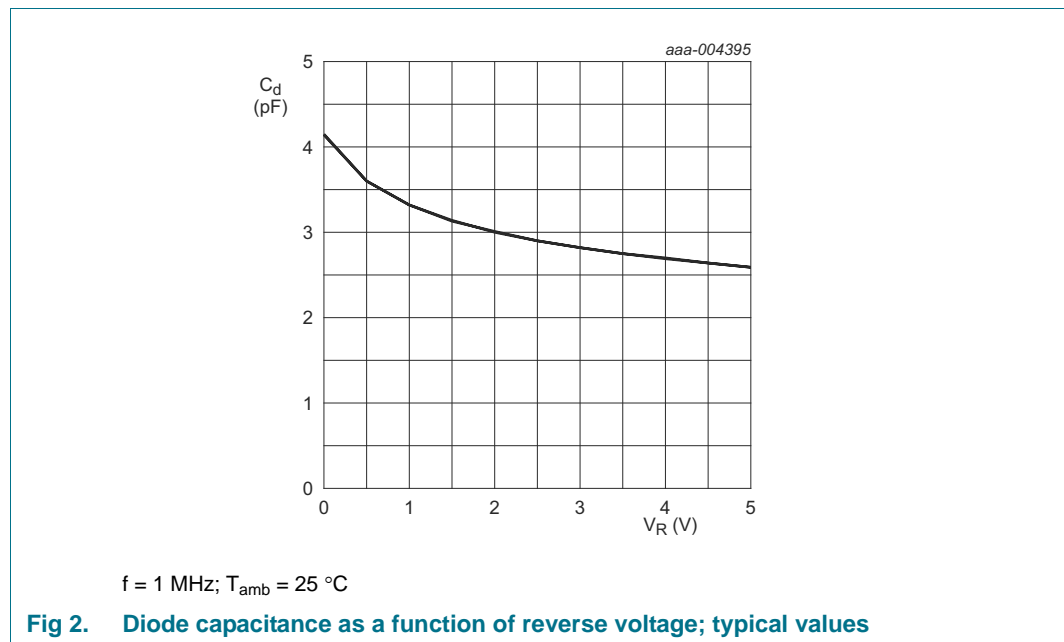
## 6. Characteristics

**Table 8. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage		-	-	5	V
$I_{RM}$	reverse leakage current	$V_{RWM} = 5\text{ V}$	-	1	100	nA
$V_{BR}$	breakdown voltage	$I_R = 1\text{ mA}$	6	7	8	V
$C_d$	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$	-	4	5	pF
$r_{dyn}$	dynamic resistance	$I_R = 10\text{ A}$	[1] -	2	-	$\Omega$

[1] Non-repetitive current pulse, Transmission Line Pulse (TLP)  $t_p = 100\text{ ns}$ ; square pulse; ANS/IESD STM5-1-2008.



**Fig 2. Diode capacitance as a function of reverse voltage; typical values**

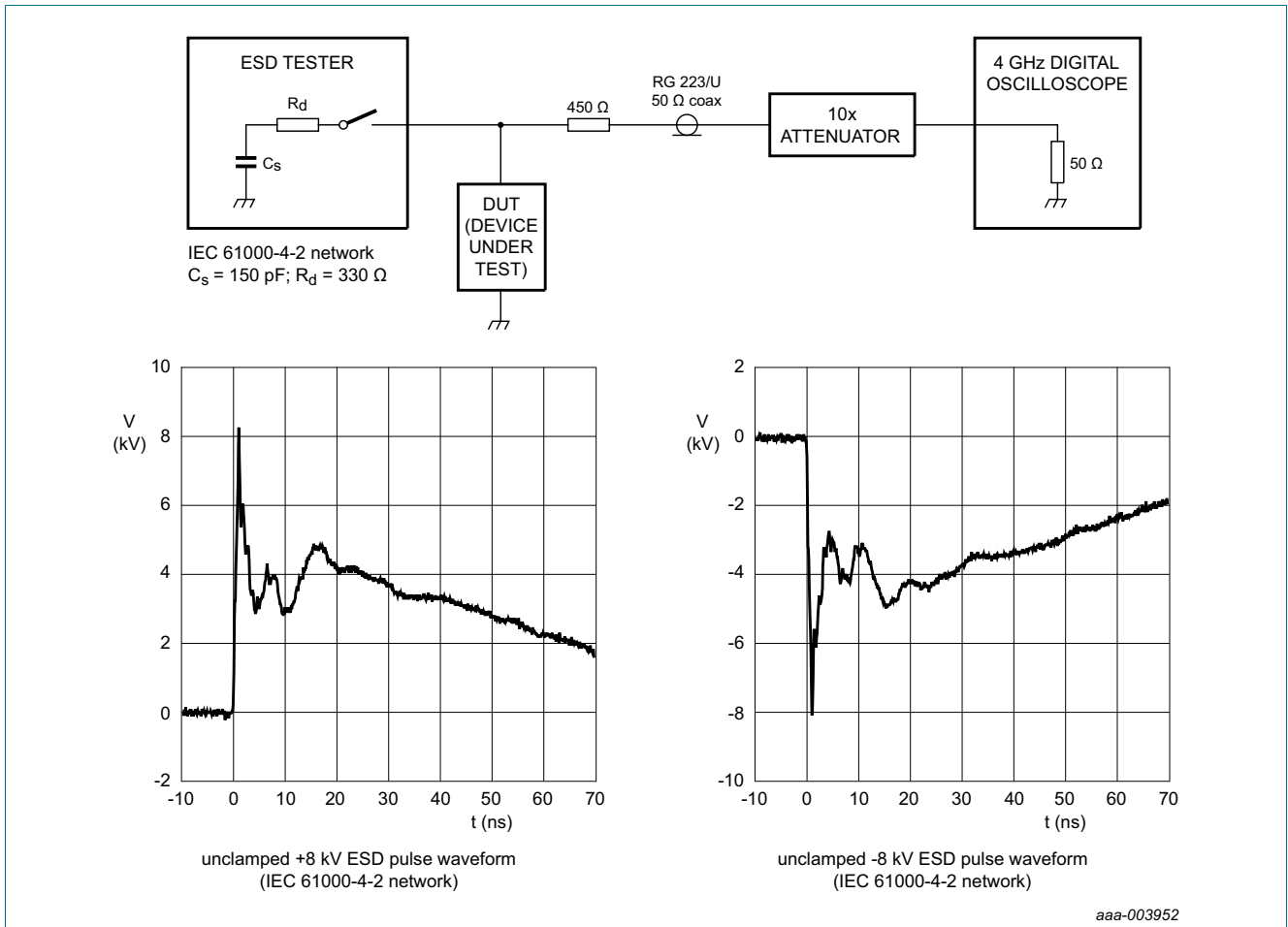
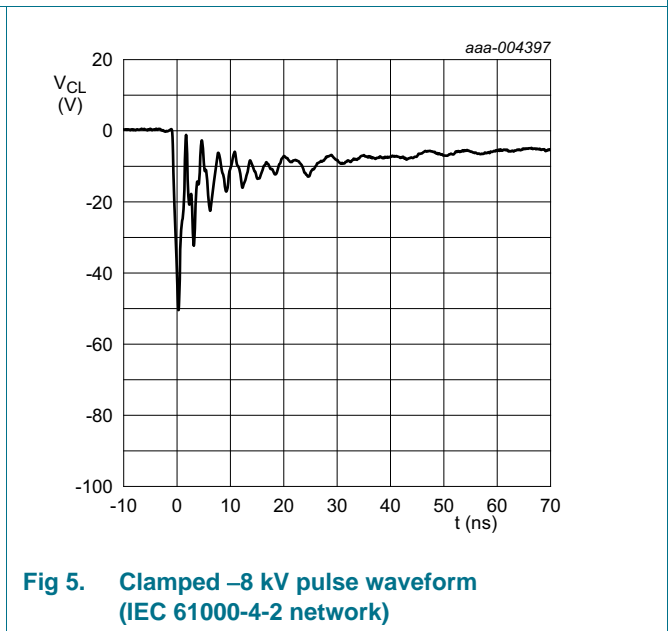
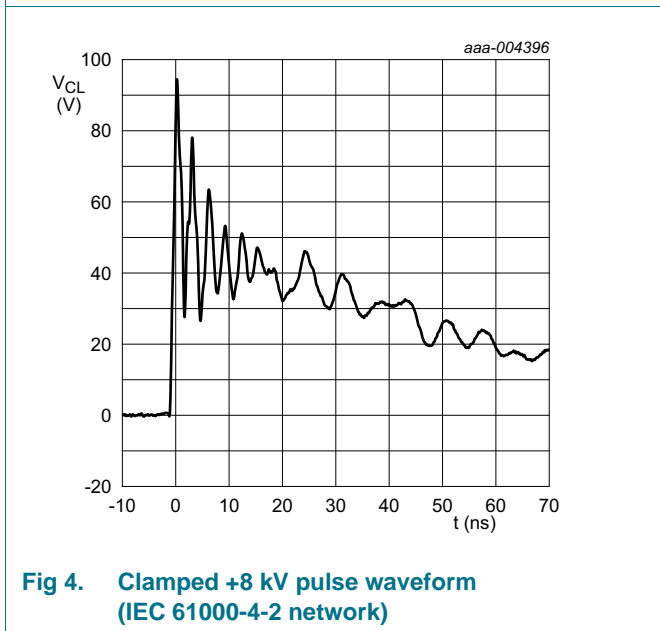
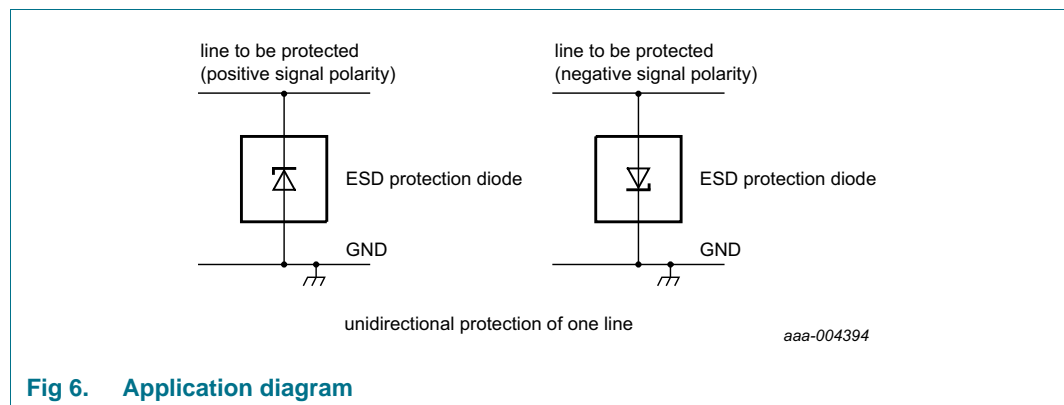


Fig 3. ESD clamping test setup



## 7. Application information

The device is designed for the protection of one unidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground.



**Fig 6. Application diagram**

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 8. Package outline

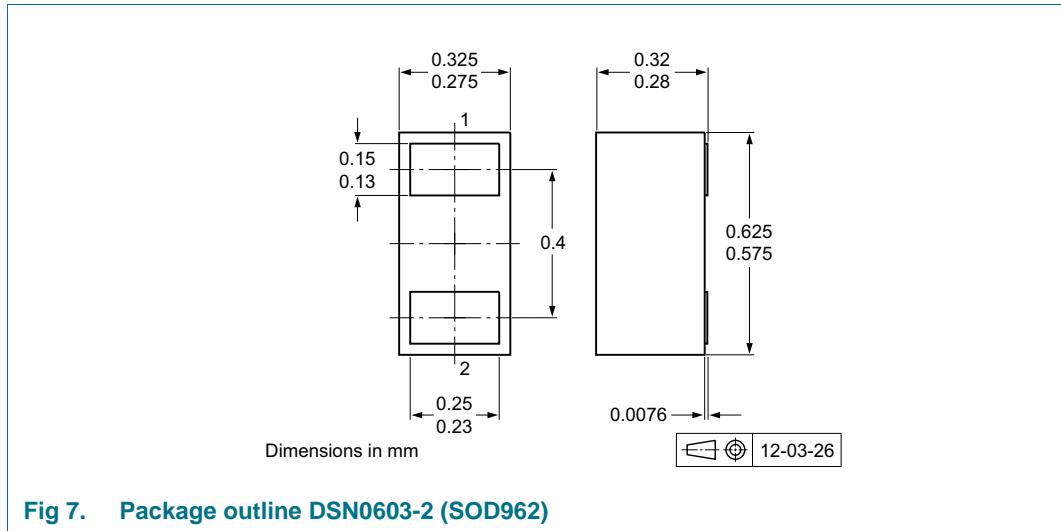


Fig 7. Package outline DSN0603-2 (SOD962)

## 9. Packing information

**Table 9. Packing methods**

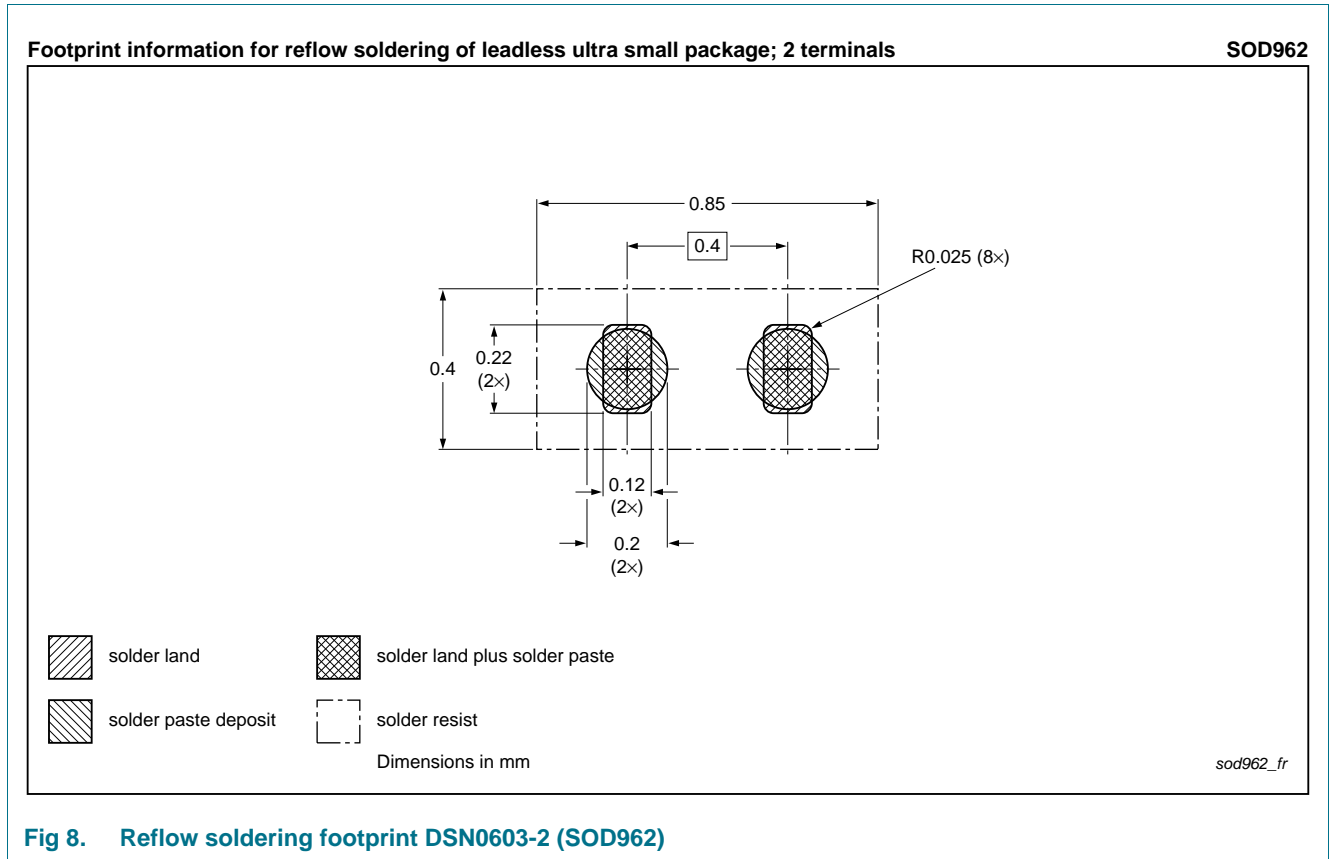
The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity
			9000
PESD5V0V1USF	DSN0603-2 (SOD962)	2 mm pitch, 8 mm tape and reel	-315

[1] For further information and the availability of packing methods, see [Section 13](#).



## 10. Soldering



## 11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0V1USF v.1	20120716	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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