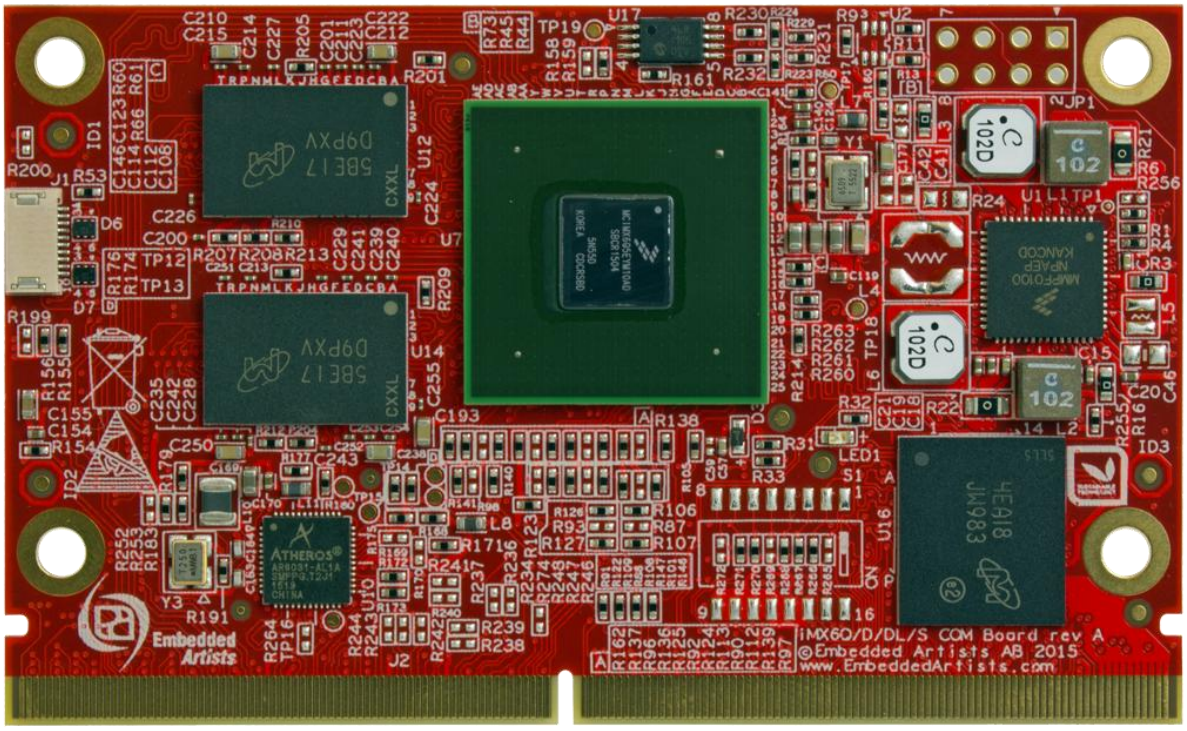
iMX6 Quad/Dual COM Board Datasheet



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1 Document Revision History

Revision	*Date*	*Description*
PA1	2016-08-09	First version.
PA2	2016-10-24	Minor corrections.
PA3	2017-07-31	Added information about boot pins.

2 Introduction

This document is a datasheet that specifies and describes the *iMX6 Quad COM Board* and *iMX6 Dual COM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

The manual will refer to just the *iMX6 COM Board* when addressing bother versions of the board. Similarly, the term *i.MX 6 SoC* will refer to both i.MX 6Quad and i.MX 6Dual SoC versions.

2.1 Hardware

The *iMX6 COM Board* is a Computer-on-Module (COM) based on NXP's quad/dual-core ARM Cortex-A9 i.MX 6 System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-A9 based design. The Cortex-A9 cores runs at up to 1GHz (up to 800 MHz for industrial temperature range).

The *iMX6 COM Board* delivers high computational and graphical performance at very low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a DDR3L memory sub-system reduce the power consumption to a minimum.

The SoC is part of the scalable i.MX 6 product family. There is a range of i.MX 6 (and i.MX 7) COM Boards from Embedded Artists with single, dual and quad Cortex-A9/A7 cores, with or without a heterogeneous Cortex-M4 core. All boards share the same basic pinning for maximum flexibility and performance scalability.

The *iMX6 COM Board* has a very small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX6 COM Board* targets a wide range of applications, such as:

- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- HMI/GUI solutions
- Smart Toll Systems
- Connected vending machines
- Digital signage
- Point-of-Sale (POS) applications
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- Portable systems
- ...and much more

The picture below illustrates the block diagram of the *iMX6 COM Board*.

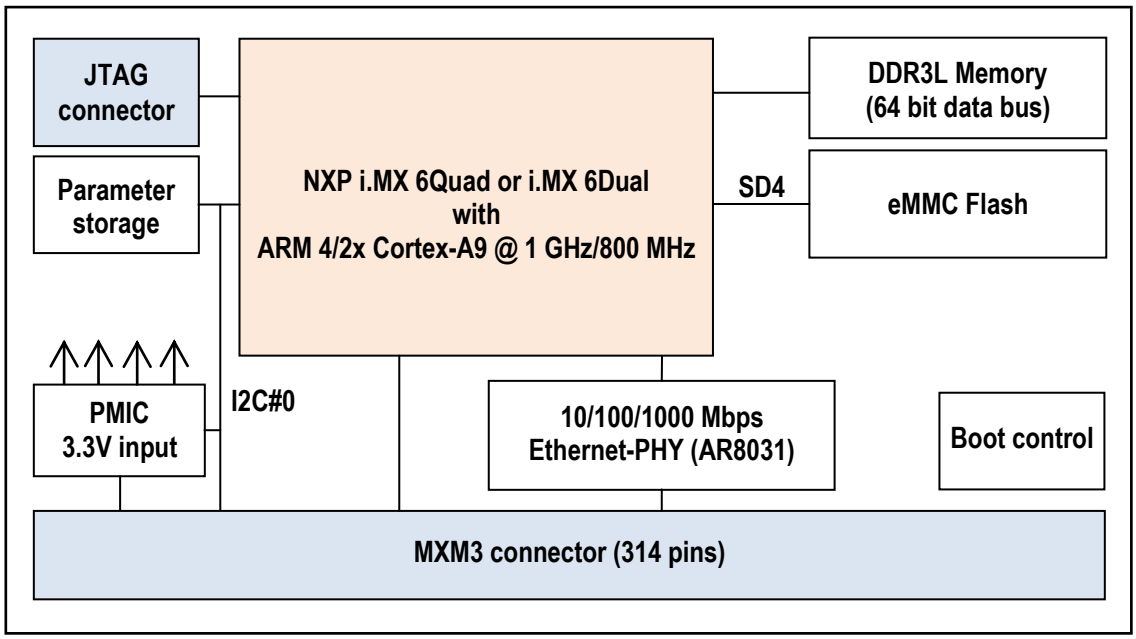


Figure 1 – iMX6 COM Board Block Diagram

The *iMX6 COM Board* pin assignment focus on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX6/7 COM Boards* from Embedded Artists and the general, so called, EACOM specification is found in separate document.

2.2 Software

The *iMX6 COM Board* has Board Support Packages (BSPs) for Embedded Linux. Precompiled images are available. Embedded Artists works with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the iMX6 COM Board for more information about software development.

2.3 Features and Functionality

The i.MX 6 is an advanced and powerful SoC. The full specification can be found in NXP's *i.MX 6Dual/Quad Application Processor Datasheet* and *i.MX 6Dual/6Quad Applications Processor Reference Manual*. The table below lists the main features and functions of the *iMX6 COM Board* - which represents Embedded Artists integration of the i.MX 6 SoC. Due to pin configuration some functions and interfaces of the i.MX 6 are not available on the *iMX6 COM Board*. See pin multiplexing Excel sheet for details.

Group	Feature		iMX6 COM Board Commercial temp. range	iMX6 COM Board Industrial temp. range
CPU	NXP SoC	i.MX 6Quad i.MX 6Dual	MCIMX6Q5EYM10AD MCIMX6D5EYM10AD	MCIMX6Q7CVT08AD MCIMX6D7CVT08AD
	CPU Cores		4/2x Cortex-A9	4/2x Cortex-A9
	L1 Instruction cache		32 KByte on each Cortex-A9	32 KByte on each Cortex-A9
	L1 Data cache		32 KByte on each Cortex-A9	32 KByte on each Cortex-A9

	Unified I/D L2 Cache	1 MByte	1 MByte
	NEON SIMD media accelerator	✓	✓
	Maximum CPU frequency	996 MHz	792 MHz
Security Functions	ARM TrustZone	✓	✓
	Advanced High Assurance Boot	✓	✓
	Cryptographic Acceleration and Assurance Module	✓	✓
	Secure Non-Volatile Storage, incl. Secure Real-Time Clock	✓	✓
	System JTAG controller	✓	✓
Memory	DDR3L RAM Size i.MX 6Quad i.MX 6Dual	2 GByte 1 GByte	2 GByte 1 GByte
	DDR3L RAM Speed	1066 MT/s	1066MT/s
	DDR3L RAM Memory Width	64 bit	64 bit
	eMMC NAND Flash (8 bit)	4 GByte	4 GByte
Graphical Processing	GPU 2D/3D	Vivante GC2000/GC355/GC320	Vivante GC2000/GC355/GC320
	Open GL ES 2.1 (176Mtri/s 1000Mpxl/s)	✓ 4 shaders	✓ 4 shaders
	PiXel Processing Pipeline (PXP)	✓	✓
Graphical Output	LVDS, 18/24-bit	✓ dual	✓ dual
	RGB, 24-bit parallel interface	✓	✓
	HDMI, v1.4	✓	✓
	MIPI-DSI, 2 lanes	✓	✓
Graphical Input	CMOS sensor interface (camera), digital 20-bit parallel interface	✓	✓
	MIPI-CSI1, serial interface, 4 lanes	✓	✓
Interfaces (all functions are not available at the same time)	10/100/1000 Mbps Gigabit Ethernet controllers **Note:** about 400 Mbps maximum throughput due to errata on SoC	✓ with on-board PHY	✓ with on-board PHY
	PCIe v2.0 (1 lane)	✓	✓
	SATA-II	✓	✓
	2x USB 2.0 ports, OTG and Host	✓	✓
	3x SD/MMC 4.5	✓ SD4 interface used on-board	✓ SD4 interface used on-board
	5x SPI, 5x UART, 3x I²C, 3x I²S/SSI, S/PDIF TX/RX	✓	✓
	Dual FlexCAN, CAN bus 2.0B	✓	✓
Other	PMIC (MMPF0100) supporting DVFS techniques for low power modes	✓	✓

	On-board boot configuration to select either eMMC or USB OTG boot source	✓	✓
	E2PROM storing board information including Ethernet MAC address and memory bus setup parameters	✓	✓
	i.MX6 on-chip RTC	✓	✓
	On-board watchdog functionality	✓	✓

2.4 Interface Overview

The table below lists the interfaces that are specified in the EACOM specification (see separate document for details) and what is supported by the *iMX6 COM board*.

Interface	EACOM specification	iMX6 COM Board	Note
UART	3 ports (two 4 wire and one 2 wire)	3 ports	More ports available as alternative pin functions
SPI	2 ports	2 ports	More ports available as alternative pin functions
I2C	3 ports	3 ports	
SD/MMC	2 ports (one 4 databits and one 8 databits)	2 ports	
Parallel LCD	24 databits and CLK/HS/VS/DE	Full support	
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	Full support	1 PWM and 4 GPIO
LVDS LCD	2 ports (18/24 bit LVDS data)	2 ports	
HDMI (TDMS)		1 port	
Parallel Camera		1 port	
Serial Camera	CSI, 4 lane	4 lanes	
Gigabit Ethernet	2 ports	1 ports	
PCIe	1 post, 1 lane	1 port, 1 lane	
SATA	1 port	1 port	
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	1 USB2.0 OTG 1 USB2.0 Host	
SPDIF	1 TX/RX port	1 port	
CAN	2 ports	2 ports	
I2S/SSI/AC97	1 port (4 wire synchronous plus MCLK)	1 port	Shared pins are used. More ports available as alternative pin functions.
Analog audio	Stereo output	-	

GPIO	9 pins	9 pins	More GPIO pins are available as alternative pin functions.
PWM	1 pin	1 pin	More pins are available as alternative pin functions.
ADC	8 inputs	-	
Type specific	39 pins	39 pins	All type specific pins connected to i.MX 6 pins.
Power	10 VIN, VBAT and 47 GND	10 VIN, VBAT and 47 GND	About 15% of the pins are ground pins.

2.5 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX6 COM board*:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX6DQCEC, i.MX 6Dual/6Quad Applications Processors for Consumer Products - Data Sheet, latest revision
- IMX6DQIEC, i.MX 6Dual/6Quad Applications Processors for Industrial Products - Data Sheet, latest version
- IMX6DQRM, i.MX 6Dual/6Quad Applications Processor Reference Manual, latest revision
- IMX6DQCE, Chip Errata for the i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN4509, i.MX 6Dual/6Quad Power Consumption Measurement, latest revision
- AN4724, i.MX 6Dual/6Quad/6DualPlus/6QuadPlus Product Usage Lifetime Estimates, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)

- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- PCI Express Specifications (www.pci-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPDIF (aka S/PDIF) (Sony Philips Digital Interface) - IEC 60958-3
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- USB Specifications (www.usb.org)
- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- HDMI Specification, Version 1.3a, November 10, 2006 © 2006 Hitachi and other companies (www.hdmi.org)
- Serial ATA Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org)

3 EACOM Board Pinning

Embedded Artists has created the *EACOM Board Specification* that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

The carrier board connector has 314 pins with 0.5 mm pitch and the EACOM board is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

Overall assembly height of the EACOM board/Carrier board connector can be as low as 6 mm. There are different stack height options available, including 2.7 mm (resulting in overall 6 mm height), 5 mm and 8 mm.

3.1 Pin Numbering

The figures below show the pin numbering for EACOM. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

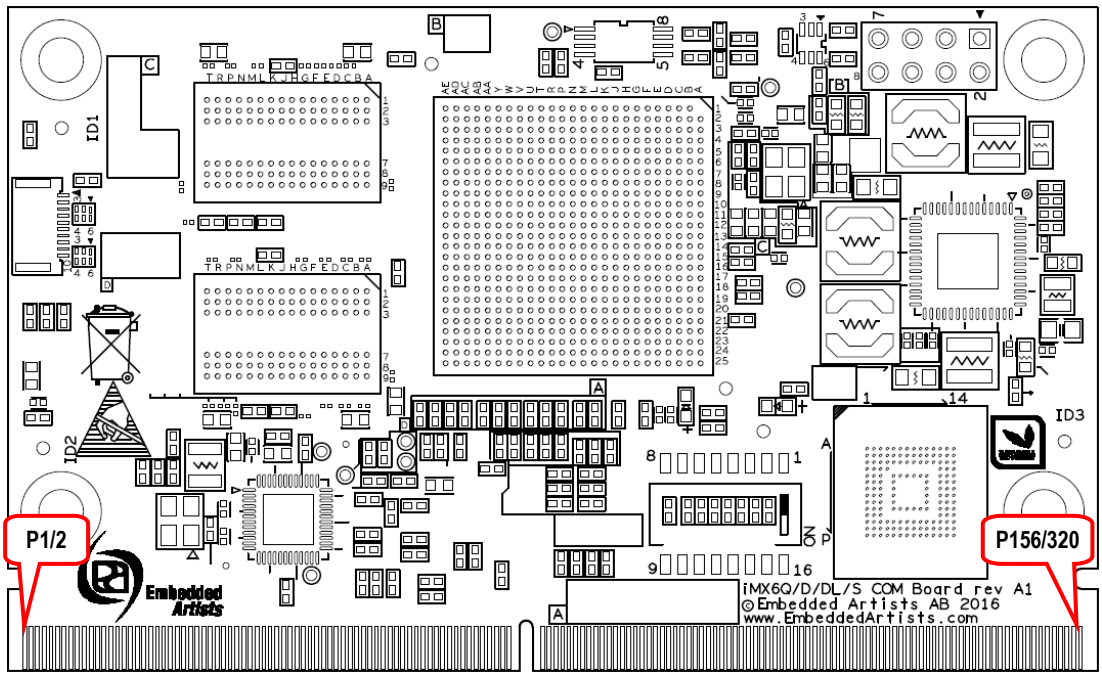


Figure 2 – EACOM Board Pin Numbering, Top Side

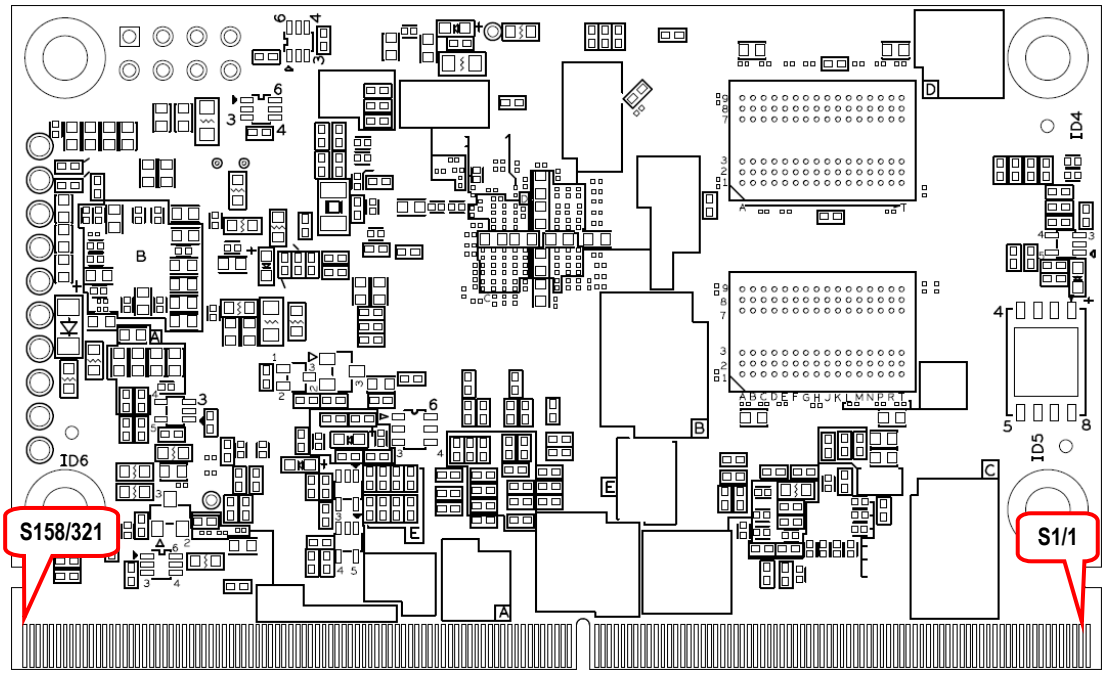


Figure 3 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different EACOM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 6 Ball Name	The name of the ball of the i.MX 6 SoC (or other component on the EACOM board) that is connected to this pin.
Notes	When relevant, the preferred pin function is listed.

There are 47 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EACOM Board	i.MX 6 Ball Name	Alternative pin functions?	Notes
P1/2	GPIO6	NAND_CS0	Yes	GPIO6 controlled by alternative pin function GPIO6_IO11
P2/4	GPIO5	NAND_READY	Yes	GPIO5 controlled by alternative pin function GPIO6_IO10
P3/6	GPIO4	NAND_WP	Yes	GPIO4 controlled by alternative pin function GPIO6_IO09
P4/8	GPIO3	SD3_RESET	Yes	GPIO3 controlled by alternative pin function GPIO7_IO08
P5/10	SD_D1	SD2_DATA1	Yes	

P6/12	SD_D0	SD2_DATA0	Yes	
P7/14	SD_CLK	SD2_CLK	Yes	
P8/16	SD_CMD	SD2_CMD	Yes	
P9/18	SD_D3	SD2_DATA3	Yes	
P10/20	SD_D2	SD2_DATA2	Yes	
P11/22	SD_VCC			Supply voltage for SD interface (3.3V). Should only supply the SD interface.
P12/24	MMC_D1	SD3_DATA1	Yes	
P13/26	MMC_D0	SD3_DATA0	Yes	
P14/28	MMC_D7	SD3_DATA7	Yes	
P15/30	MMC_D6	SD3_DATA6	Yes	
P16/32	MMC_CLK	SD3_CLK	Yes	
P17/34	MMC_D5	SD3_DATA5	Yes	
P18/36	MMC_CMD	SD3_CMD	Yes	
P19/38	MMC_D4	SD3_DATA4	Yes	
P20/40	MMC_D3	SD3_DATA3	Yes	
P21/42	MMC_D2	SD3_DATA2	Yes	
P22/44	GND			
P23/46	HDMI_TXC_N	HDMI_CLKM	No	
P24/48	HDMI_TXC_P	HDMI_CLKP	No	
P25/50	GND			
P26/52	HDMI_TXD0_N	HDMI_D0N	No	
P27/54	HDMI_TXD0_P	HDMI_D0P	No	
P28/56	HDMI_HPD	HDMI_HDP	No	
P29/58	HDMI_TXD1_N	HDMI_D1N	No	
P30/60	HDMI_TXD1_P	HDMI_D1P	No	
P31/62	GND			
P32/64	HDMI_TXD2_N	HDMI_D2N	No	
P33/66	HDMI_TXD2_P	HDMI_D2P	No	
P34/68	HDMI_CEC	EIM_ADDR25	No	CEC_IN controlled by alternative pin function GPIO5_IO02
P35/70	GND			
P36/72	ETH1_MD1_P			Connects to Ethernet-PHY AR8031 #1, pin 14
P37/74	ETH1_MD1_N			Connects to Ethernet-PHY AR8031 #1, pin 15
P38/76	GND			
P39/78	ETH1_MD0_P			Connects to Ethernet-PHY AR8031 #1, pin 11
P40/80	ETH1_MD0_N			Connects to Ethernet-PHY AR8031 #1, pin 12
P41/82	ETH1_LINK1000			Connects to Ethernet-PHY AR8031 #1, pin 24
P42/84	ETH1_ACT			Connects to Ethernet-PHY AR8031 #1, pin 23
P43/86	ETH1_LINK			Connects to Ethernet-PHY AR8031 #1, pin 26
P44/88	ETH1_MD3_N			Connects to Ethernet-PHY AR8031 #1, pin 21
P45/90	ETH1_MD3_P			Connects to Ethernet-PHY AR8031 #1, pin 20
P46/92	GND			

P47/94	ETH1_MD2_N			Connects to Ethernet-PHY AR8031 #1, pin 18
P48/96	ETH1_MD2_P			Connects to Ethernet-PHY AR8031 #1, pin 17
P49/98	GND			
P50/100	ETH2_MD1_P			ETH2 interface not assigned on this COM board.
P51/102	ETH2_MD1_N			ETH2 interface not assigned on this COM board.
P52/104	GND			
P53/106	ETH2_MD0_P			ETH2 interface not assigned on this COM board.
P54/108	ETH2_MD0_N			ETH2 interface not assigned on this COM board.
P55/110	ETH2_LINK1000			ETH2 interface not assigned on this COM board.
P56/112	ETH2_ACT			ETH2 interface not assigned on this COM board.
P57/114	ETH2_LINK			ETH2 interface not assigned on this COM board.
P58/116	ETH2_MD3_N			ETH2 interface not assigned on this COM board.
P59/118	ETH2_MD3_P			ETH2 interface not assigned on this COM board.
P60/120	GND			
P61/122	ETH2_MD2_N			ETH2 interface not assigned on this COM board.
P62/124	ETH2_MD2_P			ETH2 interface not assigned on this COM board.
P63/126	GND			
P64/128	USB_O1_DN	USB_OTG_DN	No	
P65/130	USB_O1_DP	USB_OTG_DP	No	
P66/132	USB_O1_OTG_ID	ENET_RX_ER	Yes	Controlled by alternative pin function USB_OTG1_ID
P67/134	USB_O1_SSTXN			USB OTG port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P68/136	USB_O1_SSTXP			USB OTG port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P69/138	GND			
P70/140	USB_O1_SSRXN			USB OTG port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P71/142	USB_O1_SSRXP			USB OTG port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P72/144	USB_O1_VBUS	USB_OTG_VBUS	No	
P73/146	USB_O1_PWR_EN	EIM_DATA22	Yes	Controlled by alternative pin function USB_OTG1_PWR
P74/148	USB_O1_OC	EIM_DATA21	Yes	Controlled by alternative pin function USB_OTG1_OC
150	Non existing pin			
152	Non existing pin			
154	Non existing pin			
156	Non existing pin			
P75/158	USB_H1_PWR_EN	GPIO_0	Yes	Controlled by alternative pin function USB_H1_PWR
P76/160	USB_H1_OC	GPIO_3	Yes	Controlled by alternative pin function USB_H1_OC
P77/162	GND			
P78/164	USB_H1_DN	USB_H1_DN	No	
P79/166	USB_H1_DP	USB_H1_DP	No	
P80/168	USB_H1_SSTXN			USB Host port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P81/170	USB_H1_SSTXP			USB Host port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.

P82/172	GND			
P83/174	USB_H1_SSRXN			USB Host port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P84/176	USB_H1_SSRXP			USB Host port #1 on i.MX 6 does not support USB 3.0 so this pin is unconnected.
P85/178	USB_H1_VBUS	USB_H1_VBUS	No	
P86/180	USB_H2_PWR_EN	SNVS_TAMPER	No	USB Host port #2 on i.MX 6 does not exist. Non-standard pin allocation. Pin carry signal SNVS_TAMPER, i.MX 6Quad ball E11.
P87/182	USB_H2_OC	ONOFF	No	USB Host port #2 on i.MX 6 does not exist. Non-standard pin allocation. Pin carry signal ONOFF, i.MX 6Quad ball D12.
P88/184	GND			
P89/186	USB_H2_DN	CSI0_VSYNC	Yes	USB Host port #2 on i.MX 6 does not exist. Non-standard pin allocation.
P90/188	USB_H2_DP	CSI0_DATA_EN	Yes	USB Host port #2 on i.MX 6 does not exist. Non-standard pin allocation.
P91/190	GND			
P92/192	COM board specific	KEY_ROW1		
P93/194	COM board specific	KEY_ROW0		
P94/196	COM board specific	KEY_COL1		
P95/198	COM board specific	KEY_COL0		
P96/200	COM board specific	NAND_DATA07		
P97/202	COM board specific	NAND_DATA06		
P98/204	COM board specific	NAND_DATA05		
P99/206	COM board specific	NAND_DATA04		
P100/208	COM board specific	NAND_DATA03		
P101/210	COM board specific	NAND_DATA02		
P102/212	COM board specific	NAND_DATA01		
P103/214	COM board specific	NAND_DATA00		
P104/216	COM board specific	NAND_CS3		
P105/218	COM board specific	EIM_DATA31		
P106/220	COM board specific	EIM_DATA30		
P107/222	COM board specific	EIM_DATA29		
P108/224	COM board specific	EIM_DATA28		
P109/226	COM board specific	EIM_DATA27		
P110/228	COM board specific	EIM_DATA26		
P111/230	COM board specific	EIM_DATA25		
P112/232	COM board specific	EIM_DATA24		
P113/234	COM board specific	EIM_DATA23		
P114/236	COM board specific	EIM_EB3		
P115/238	COM board specific	EIM_LBA		
P116/240	COM board specific	EIM_DATA20		
P117/242	COM board specific	EIM_DATA19		

P118/244	GND			
P119/246	SPI-B_SSEL	SD1_DATA1	Yes	Controlled by alternative pin function ECSPI5_SS0
P120/248	SPI-B_MOSI	SD1_CMD	Yes	Controlled by alternative pin function ECSPI5_MOSI
P121/250	SPI-B_MISO	SD1_DATA0	Yes	Controlled by alternative pin function ECSPI5_MISO
P122/252	SPI-B_CLK	SD1_CLK	Yes	Controlled by alternative pin function ECSPI5_SCLK
P123/254	SPI-A_SSEL	EIM_RW	Yes	Controlled by alternative pin function ECSPI2_SS0
P124/256	SPI-A_MOSI	EIM_CS1	Yes	Controlled by alternative pin function ECSPI2_MOSI
P125/258	SPI-A_MISO	EIM_OE	Yes	Controlled by alternative pin function ECSPI2_MISO
P126/260	SPI-A_CLK	EIM_CS0	Yes	Controlled by alternative pin function ECSPI2_SCLK
P127/262	GND			
P128/264	UART-C_RXD	CSI0_DATA11	Yes	Controlled by alternative pin function UART1_RX_DATA
P129/266	UART-C_TXD	CSI0_DATA10	Yes	Controlled by alternative pin function UART1_TX_DATA
P130/268	UART-B_RXD	CSI0_DATA15	Yes	Controlled by alternative pin function UART5_RX_DATA
P131/270	UART-B_CTS	CSI0_DATA19	Yes	Controlled by alternative pin function UART5_CTS_B
P132/272	UART-B_RTS	CSI0_DATA18	Yes	Controlled by alternative pin function UART5_RTS_B
P133/274	UART-B_TXD	CSI0_DATA14	Yes	Controlled by alternative pin function UART5_TX_DATA
P134/276	UART-A_RXD	CSI0_DATA13	Yes	Controlled by alternative pin function UART4_RX_DATA
P135/278	UART-A_CTS	CSI0_DATA17	Yes	Controlled by alternative pin function UART4_CTS_B
P136/280	UART-A_RTS	CSI0_DATA16	Yes	Controlled by alternative pin function UART4_RTS_B
P137/282	UART-A_TXD	CSI0_DATA12	Yes	Controlled by alternative pin function UART4_TX_DATA
P138/284	PWM	SD1_DATA3	Yes	Controlled by alternative pin function PWM1_OUT.
P139/286	GPIO2	GPIO_1	Yes	GPIO2 controlled by alternative pin function GPIO1_IO01
P140/288	GPIO1	GPIO_4	Yes	GPIO1 controlled by alternative pin function GPIO1_IO04
P141/290	PERI_PWR_EN	GPIO_17	Yes	Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EACOM Board specification*.
P142/292	RESET_IN			Reset input, active low. Pull signal low to activate reset. No need to pull signal high externally.
P143/294	RESET_OUT			Reset (open drain) output, active low. Driven low during reset. 1.5K pull-up resistor to VIN.
P144/296	GND			
P145/298	VBAT			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	E2PROM_WP			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM AND place the i.MX 6 SoC in USB OTG boot mode after a power cycle).
P147/302	VIN			Main input voltage supply (3.3V)
P148/304	VIN			Main input voltage supply (3.3V)
P149/306	VIN			Main input voltage supply (3.3V)
P150/308	VIN			Main input voltage supply (3.3V)
P151/310	VIN			Main input voltage supply (3.3V)
P152/312	VIN			Main input voltage supply (3.3V)
P153/314	VIN			Main input voltage supply (3.3V)
P154/316	VIN			Main input voltage supply (3.3V)
P155/318	VIN			Main input voltage supply (3.3V)

P156/320	VIN	Main input voltage supply (3.3V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	i.MX 6 Ball Name	Alternative pin functions?	Notes
S1/1	MQS_RIGHT	GPIO_8	Yes	Note that the i.MX 6 does not have MQS peripheral.
S2/3	MQS_LEFT	GPIO_7	Yes	Note that the i.MX 6 does not have MQS peripheral.
S3/5	GND			
S4/7	AUDIO_TXFS	CSI0_DATA06	Yes	Controlled by alternative pin function AUD3_TXFS.
S5/9	AUDIO_RXD	CSI0_DATA07	Yes	Controlled by alternative pin function AUD3_RXD.
S6/11	AUDIO_TXC	CSI0_DATA04	Yes	Controlled by alternative pin function AUD3_TXC.
S7/13	AUDIO_TXD	CSI0_DATA05	Yes	Controlled by alternative pin function AUD3_TXD.
S8/15	AUDIO_MCLK	GPIO_19	Yes	Controlled by alternative pin function CCM_CLKO1.
S9/17	GND			
S10/19	SPDIF_IN	GPIO_16	Yes	Controlled by alternative pin function SPDIF_IN
S11/21	SPDIF_OUT	ENET_RX_DATA0	Yes	Controlled by alternative pin function SPDIF_OUT
S12/23	CAN2_TX	KEY_COL4	Yes	Controlled by alternative pin function CAN2_TX
S13/25	CAN2_RX	KEY_ROW4	Yes	Controlled by alternative pin function CAN2_RX
S14/27	CAN1_TX	KEY_COL2	Yes	Controlled by alternative pin function CAN1_TX
S15/29	CAN1_RX	KEY_ROW2	Yes	Controlled by alternative pin function CAN1_RX
S16/31	GND			
S17/33	LVDS1_D3_P	LVDS1_DATA3_P	No	
S18/35	LVDS1_D3_N	LVDS1_DATA3_N	No	
S19/37	GPIO9	NAND_CLE	Yes	
S20/39	LVDS1_D2_P	LVDS1_DATA2_P	No	
S21/41	LVDS1_D2_N	LVDS1_DATA2_N	No	
S22/43	GND			
S23/45	LVDS1_D1_P	LVDS1_DATA1_P	No	
S24/47	LVDS1_D1_N	LVDS1_DATA1_N	No	
S25/49	GND			
S26/51	LVDS1_D0_P	LVDS1_DATA0_P	No	
S27/53	LVDS1_D0_N	LVDS1_DATA0_N	No	
S28/55	GND			
S29/57	LVDS1_CLK_P	LVDS1_CLK_P	No	
S30/59	LVDS1_CLK_N	LVDS1_CLK_N	No	
S31/61	GND			
S32/63	LVDS0_D3_P	LVDS0_DATA3_P	No	
S33/65	LVDS0_D3_N	LVDS0_DATA3_N	No	
S34/67	GPIO8	EIM_ADDR25	Yes	
S35/69	LVDS0_D2_P	LVDS0_DATA2_P	No	
S36/71	LVDS0_D2_N	LVDS0_DATA2_N	No	
S37/73	GND			

S38/75	LVDS0_D1_P	LVDS0_DATA1_P	No	
S39/77	LVDS0_D1_N	LVDS0_DATA1_N	No	
S40/79	GND			
S41/81	LVDS0_D0_P	LVDS0_DATA0_P	No	
S42/83	LVDS0_D0_N	LVDS0_DATA0_N	No	
S43/85	GND			
S44/87	LVDS0_CLK_P	LVDS0_CLK_P	No	
S45/89	LVDS0_CLK_N	LVDS0_CLK_N	No	
S46/91	I2C-A_SDA	CSI0_DATA08	Yes	Controlled by alternative pin function I2C1_SDA
S47/93	I2C-A_SCL	CSI0_DATA09	Yes	Controlled by alternative pin function I2C1_SCL
S48/95	I2C-B_SDA	GPIO_6	Yes	Controlled by alternative pin function I2C3_SDA
S49/97	I2C-B_SCL	GPIO_5	Yes	Controlled by alternative pin function I2C3_SCL
S50/99	HDMI/I2C-C_SDA	KEY_ROW3	Yes	Controlled by alternative pin function I2C2_SDA
S51/101	HDMI/I2C-C_SCL	KEY_COL3	Yes	Controlled by alternative pin function I2C2_SCL
S52/103	TP_RST	EIM_AD14	Yes	Controlled by alternative pin function GPIO3_IO14
S53/105	TP_IRQ	EIM_AD13	Yes	Controlled by alternative pin function GPIO3_IO13
S54/107	DISP_PWR_EN	EIM_BCLK	Yes	Controlled by alternative pin function GPIO6_IO31
S55/109	BL_PWR_EN	EIM_WAIT	Yes	Controlled by alternative pin function GPIO5_IO00
S56/111	BL_PWM	SD1_DATA2	Yes	Controlled by alternative pin function PWM2_OUT
S57/113	GND			
S58/115	LCD_R0	DISP0_DATA16	Yes	Controlled by alternative pin function DISP0_DATA16
S59/117	LCD_R1	DISP0_DATA17	Yes	Controlled by alternative pin function DISP0_DATA17
S60/119	LCD_R2	DISP0_DATA18	Yes	Controlled by alternative pin function DISP0_DATA18
S61/121	LCD_R3	DISP0_DATA19	Yes	Controlled by alternative pin function DISP0_DATA19
S62/123	LCD_R4	DISP0_DATA20	Yes	Controlled by alternative pin function DISP0_DATA20
S63/125	LCD_R5	DISP0_DATA21	Yes	Controlled by alternative pin function DISP0_DATA21
S64/127	LCD_R6	DISP0_DATA22	Yes	Controlled by alternative pin function DISP0_DATA22
S65/129	LCD_R7	DISP0_DATA23	Yes	Controlled by alternative pin function DISP0_DATA23
S66/131	LCD_G0	DISP0_DATA08	Yes	Controlled by alternative pin function DISP0_DATA08
S67/133	LCD_G1	DISP0_DATA09	Yes	Controlled by alternative pin function DISP0_DATA09
S68/135	LCD_G2	DISP0_DATA10	Yes	Controlled by alternative pin function DISP0_DATA10
S69/137	LCD_G3	DISP0_DATA11	Yes	Controlled by alternative pin function DISP0_DATA11
S70/139	LCD_G4	DISP0_DATA12	Yes	Controlled by alternative pin function DISP0_DATA12
S71/141	LCD_G5	DISP0_DATA13	Yes	Controlled by alternative pin function DISP0_DATA13
S72/143	LCD_G6	DISP0_DATA14	Yes	Controlled by alternative pin function DISP0_DATA14
S73/145	LCD_G7	DISP0_DATA15	Yes	Controlled by alternative pin function DISP0_DATA15
S74/147	GND			
S75/149	LCD_B0	DISP0_DATA00	Yes	Controlled by alternative pin function DISP0_DATA00
151	Non existing pin			
153	Non existing pin			
155	Non existing pin			
S76/157	LCD_B1	DISP0_DATA01	Yes	Controlled by alternative pin function DISP0_DATA01

S77/159	LCD_B2	DISP0_DATA02	Yes	Controlled by alternative pin function DISP0_DATA02
S78/161	LCD_B3	DISP0_DATA03	Yes	Controlled by alternative pin function DISP0_DATA03
S79/163	LCD_B4	DISP0_DATA04	Yes	Controlled by alternative pin function DISP0_DATA04
S80/165	LCD_B5	DISP0_DATA05	Yes	Controlled by alternative pin function DISP0_DATA05
S81/167	LCD_B6	DISP0_DATA06	Yes	Controlled by alternative pin function DISP0_DATA06
S82/169	LCD_B7	DISP0_DATA07	Yes	Controlled by alternative pin function DISP0_DATA07
S83/171	LCD_CLK	DISP0_DISP_CLK	Yes	Controlled by alternative pin function DISP0_DISP_CLK
S84/173	GPIO7	DISP0_PIN04	Yes	GPIO7 controlled by alternative pin function GPIO4_IO20
S85/175	LCD_HSYNC	DISP0_PIN02	Yes	Controlled by alternative pin function DISP0_HSYNC
S86/177	LCD_VSYNC	DISP0_PIN03	Yes	Controlled by alternative pin function DISP0_VSYNC
S87/179	LCD_ENABLE	DISP0_PIN15	Yes	Controlled by alternative pin function DISP0_DEN
S88/181	GND			
S89/183	AIN_VREF	CSI0_PIXCLK	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S90/185	AIN7	CSI0_HSYNC	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S91/187	AIN6	EIM_AD06	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S92/189	AIN5	EIM_AD07	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S93/191	AIN4	EIM_AD08	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S94/193	AIN3	EIM_AD09	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S95/195	AIN2	EIM_AD15	Yes	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs.
S96/197	AIN1	DSI_D1M	No	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs. Allocated for MIPI-DSI interface.
S97/199	AIN0	DSI_D1P	No	Non-standard pin allocation. The i.MX 6 does not have any AIN inputs. Allocated for MIPI-DSI interface.
S98/201	GND			
S99/203	COM board specific	DSI_D0M	No	
S100/205	COM board specific	DSI_D0P	No	
S101/207	GND			
S102/209	COM board specific	DSI_CLKM	No	
S103/211	COM board specific	DSI_CLKP	No	
S104/213	GND			
S105/215	COM board specific	EIM_AD10	Yes	
S106/217	COM board specific	EIM_AD05	Yes	
S107/219	COM board specific	EIM_AD04	Yes	
S108/221	COM board specific	EIM_AD03	Yes	
S109/223	COM board specific	EIM_AD02	Yes	
S110/225	COM board specific	EIM_AD01	Yes	
S111/227	COM board specific	EIM_AD00	Yes	
S112/229	COM board specific	EIM_EB1	Yes	
S113/231	COM board specific	EIM_EB0	Yes	

S114/233	CSI_HSYNC	EIM_AD11	Yes	Controlled by alternative pin function IPU2_CSI1_HSYNC
S115/235	CSI_VSYNC	EIM_AD12	Yes	Controlled by alternative pin function IPU2_CSI1_YSYNC
S116/237	CSI_MCLK	NAND_CS2	Yes	Controlled by alternative pin function PCAM_MCLK
S117/239	CSI_PCLK	EIM_ADDR16	Yes	Controlled by alternative pin function IPU2_CSI1_PIXCLK
S118/241	GND			
S119/243	CSI_D0	EIM_ADDR17	Yes	Controlled by alternative pin function IPU2_CSI1_DATA12
S120/245	CSI_D1	EIM_ADDR18	Yes	Controlled by alternative pin function IPU2_CSI1_DATA13
S121/247	CSI_D2	EIM_ADDR19	Yes	Controlled by alternative pin function IPU2_CSI1_DATA14
S122/249	CSI_D3	EIM_ADDR20	Yes	Controlled by alternative pin function IPU2_CSI1_DATA15
S123/251	CSI_D4	EIM_ADDR21	Yes	Controlled by alternative pin function IPU2_CSI1_DATA16
S124/253	CSI_D5	EIM_ADDR22	Yes	Controlled by alternative pin function IPU2_CSI1_DATA17
S125/255	CSI_D6	EIM_ADDR23	Yes	Controlled by alternative pin function IPU2_CSI1_DATA18
S126/257	CSI_D7	EIM_ADDR24	Yes	Controlled by alternative pin function IPU2_CSI1_DATA19
S127/259	GND			
S128/261	CSI_D3_M	CSI_D3_M	No	
S129/263	CSI_D3_P	CSI_D3_P	No	
S130/265	GND			
S131/267	CSI_D2_M	CSI_D2_M	No	
S132/269	CSI_D2_P	CSI_D2_P	No	
S133/271	GND			
S134/273	CSI_D1_M	CSI_D1_M	No	
S135/275	CSI_D1_P	CSI_D1_P	No	
S136/277	GND			
S137/279	CSI_D0_M	CSI_D0_M	No	
S138/281	CSI_D0_P	CSI_D0_P	No	
S139/283	GND			
S140/285	CSI_CLK_M	CSI_CLK_M	No	
S141/287	CSI_CLK_P	CSI_CLK_P	No	
S142/289	GND			
S143/291	SATA_TX_P	SATA_TX_P	No	
S144/293	SATA_TX_N	SATA_TX_N	No	
S145/295	GND			
S146/297	SATA_RX_N	SATA_RX_N	No	
S147/299	SATA_RX_P	SATA_RX_P	No	
S148/301	GND			
S149/303	GND			
S150/305	PCIE_CLK_P	CCM_CLK1_P	No	100 MHz PCIE clock signal generated by CCM_CLK1 outputs.
S151/307	PCIE_CLK_N	CCM_CLK1_N	No	100 MHz PCIE clock signal generated by CCM_CLK1 outputs.
S152/309	GND			
S153/311	PCIE_TX_P	PCIE_TX_P	No	
S154/313	PCIE_TX_N	PCIE_TX_N	No	

S155/315	GND		
S156/317	PCIE_RX_P	PCIE_RX_P	No
S157/319	PCIE_RX_N	PCIE_RX_N	No
S158/321	GND		

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 6 SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leave great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like PCIe, SATA, HDMI, MIPI and LVDS. The i.MX 6 pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between EACOM boards the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX6 COM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM board is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 6 pin. For more information about the register settings, see the *i.MX 6Dual/6Quad Applications Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings, see the *i.MX 6Dual/6Quad Applications Processor Reference Manual* from NXP.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. Reset state (typically GPIO, ALT5 function, except for two pins) is shown as well as the EACOM function allocation.

4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 6 pin. For more information about the register settings, see the *i.MX 6Dual/6Quad Applications Processor Reference Manual* from NXP.

Note that most pins are configured as GPIO inputs, with a 100Kohm pull-down resistor, after reset. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

5 Interface Description

This chapter lists details about all different interfaces. The **i.MX 6 datasheet and user manual should always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously.

Note that this chapter do not list all peripheral functions available on the i.MX6 SoC. Only the ones related to the EACOM specification. For all available interfaces, consult *Chapter 4 - External Signals and Pin Multiplexing, Section 4.1.2 Muxing Options* in NXP's *i.MX 6Dual/Quad Applications Processor Reference Manual* (document id: IMX6DQRM).

Example of peripheral blocks **not** listed in this chapter are listed below (see document IMX6DQRM for details). Some of the blocks have multiple instances.

- ASRC - Asynchronous Sample Rate Converter
- CCM - Clock Controller Module
  Besides internal clocks, this peripheral can generate external clocks.
- EIM - External Interface Module
  This peripheral provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-Flash-like or PSRAM-like interface.
- EPIT - Enhanced Periodic Interrupt Timer
  This peripheral is a 32-bit timer that provides precise interrupts.
- GPT - General Purpose Timer
  This peripheral is a 32-bit general purpose timer with capture and trigger functions.
- KPP - Keypad Port
  This peripheral provides a keypad matrix interface.
- SDMA - Smart Direct Memory Access Controller
  This peripheral provides fast data transfers between peripheral I/O devices and internal/external memories
- WDOG - Watchdog Timer
  This peripheral implements a watchdog timer.

There is an accompanying Excel document that lists all alternative functions for each available I/O pin.

5.1 Camera Interfaces

This section lists signals related to CMOS Sensor Interface (CSI) functions.

There are two parallel camera interfaces, one to each IPU. There is also a serial camera interface, MIPI-CSI2 that is connected (in parallel) to both IPUs. The picture below illustrate the multiplexing options and where the EACOM allocated interfaces are connected.

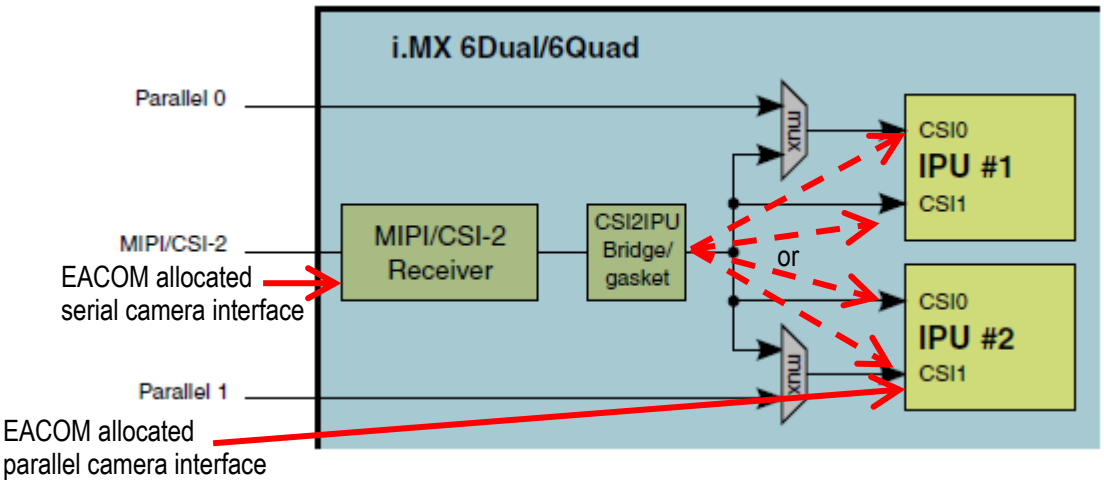


Figure 4 – Camera Port Multiplexing Scheme

5.1.1 Parallel Camera Interface

This section lists signals for the parallel camera interface.

The *EACOM Board specification* defines an 8-bit parallel camera interface. It is connected to IPU2, port 1. Note the difference in pin numbering and internal data bus numbering. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S116/237	CSI_MCLK	NAND_CS2_B	O	CMOS Sensor Master Clock	Signal called CCM_CLKO2 internally
S117/239	CSI_PIXCLK	EIM_ADDR16	I	Pixel Clock	Signal called IPU2_CSI1_PIXCLK internally
S114/233	CSI_HSYNC	EIM_AD11	I	Horizontal Sync	Signal called IPU2_CSI1_HSYNC internally
S115/235	CSI_VSYNC	EIM_AD12	I	Vertical Sync (Start Of Frame)	Signal called IPU2_CSI1_VSYNC internally
S119/243	CSI_D0	EIM_ADDR17	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA12 internally.
S120/245	CSI_D1	EIM_ADDR18	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA13 internally.
S121/247	CSI_D2	EIM_ADDR19	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA14 internally.
S122/249	CSI_D3	EIM_ADDR20	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA15 internally.
S123/251	CSI_D4	EIM_ADDR21	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA16 internally.
S124/253	CSI_D5	EIM_ADDR22	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA17 internally.
S125/255	CSI_D6	EIM_ADDR23	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA18 internally.
S126/257	CSI_D7	EIM_ADDR24	I	Data Sensor Signal	Signal called IPU2_CSI1_DATA19 internally.

The table below lists the alternative pin locations for the parallel camera interface to IPU1, port 0. Note that IPU1_CSI0_DATA08 and IPU1_CSI0_DATA09 are not available because these pins are allocated to I2C channel A. This means that typically only an 8-bit interface is available, via IPU1_CSI0_DATA12-19.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P109/226	COM specific	EIM_D27	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA00
P110/228	COM specific	EIM_D26	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA01
P105/218	COM specific	EIM_D31	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA02
P106/220	COM specific	EIM_D30	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA03
S6/11	AUDIO_TXC	CSI0_DAT4	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA04
S7/13	AUDIO_TXD	CSI0_DAT5	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA05
S4/7	AUDIO_TXFS	CSI0_DAT6	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA06
S5/9	AUDIO_RXD	CSI0_DAT7	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA07
P129/266	UART-C_TXD	CSI0_DAT10	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA10
P128/264	UART-C_RXD	CSI0_DAT11	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA11
P137/282	UART-A_TXD	CSI0_DAT12	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA12
P134/276	UART-A_RXD	CSI0_DAT13	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA13
P133/274	UART-B_TXD	CSI0_DAT14	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA14
P130/268	UART-B_RXD	CSI0_DAT15	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA15
P136/280	UART-A_RTS	CSI0_DAT16	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA16
P135/278	UART-A_CTS	CSI0_DAT17	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA17
P132/272	UART-B_RTS	CSI0_DAT18	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA18
P131/270	UART-B_CTS	CSI0_DAT19	I	Data Sensor Signal	Alternative location for IPU1_CSI0_DATA19
P90/188	USB_H2_DP	CSI0_DATA_EN	I	Data Enable Signal	Alternative location for IPU1_CSI0_DATA_EN
S90/185	AIN7	CSI0_MCLK	I	Horizontal Sync	Alternative location for IPU1_CSI0_HSYNC
S89/183	AIN_VREF	CSI0_PIXCLK	I	Pixel Clock	Alternative location for IPU1_CSI0_PIXCLK
P89/186	USB_H2_DN	CSI0_VSYNC	I	Vertical Sync	Alternative location for IPU1_CSI0_VSYNC

The table below lists the alternative pin locations for the parallel camera interface to IPU2, port 1.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S94/193	AIN3	EIM_DA9	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA00
S93/191	AIN4	EIM_DA8	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA01
S92/189	AIN5	EIM_DA7	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA02
S91/187	AIN6	EIM_DA6	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA03
S106/217	COM specific	EIM_DA5	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA04
S107/219	COM specific	EIM_DA4	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA05
S108/221	COM specific	EIM_DA3	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA06
S109/223	COM specific	EIM_DA2	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA07
S110/225	COM specific	EIM_DA1	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA08
S111/227	COM specific	EIM_DA0	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA09
P73/146	USB_O1_PWR_EN	EIM_D22	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA10

S112/229	COM specific	EIM_EB1	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA10
P74/148	USB_O1_OC	EIM_D21	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA11
S113/231	COM specific	EIM_EB0	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA11
P108/224	COM specific	EIM_D28	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA12
P109/226	COM specific	EIM_D27	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA13
P110/228	COM specific	EIM_D26	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA14
P116/240	COM specific	EIM_D20	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA15
P117/242	COM specific	EIM_D19	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA16
P81/170	USB_H1_SSTXP	EIM_D18	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA17
P84/176	USB_H1_SSRXP	EIM_D16	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA18
P80/168	USB_H1_SSTXN	EIM_EB2	I	Data Sensor Signal	Alternative location for IPU2_CSI1_DATA19
S105/215	COM specific	EIM_DA10	I	Data Enable Signal	Alternative location for IPU2_CSI1_DATA_EN
P113/234	COM specific	EIM_D23	I	Data Enable Signal	Alternative location for IPU2_CSI1_DATA_EN
S114/233	CSI_HSYNC	EIM_DA11	I	Horizontal Sync	Alternative location for IPU2_CSI1_HSYNC
P114/236	COM specific	EIM_EB3	I	Horizontal Sync	Alternative location for IPU2_CSI1_HSYNC
P83/174	USB_H1_SSRXN	EIM_D17	I	Pixel Clock	Alternative location for IPU2_CSI1_PIXCLK
P107/222	COM specific	EIM_D29	I	Vertical Sync	Alternative location for IPU2_CSI1_VSYNC

The CSI can support connection with the sensor as follows.

- To connect with one 8-bit sensor, the sensor data interface should connect to CSI_DATA[19:12]. This is the method that is supported by the *EACOM Board specification*.
- To connect with one 16-bit sensor, the sensor data interface should connect to CSI_DATA[19:40].
- To connect with one 20-bit sensor, the sensor data interface should connect to CSI_DATA[19:0].

The CSI input data format mapping is shown in the table below.

Internal IPUx CSIx Signal Name	EACOM Board Name	RGB565 8 bits 2 cycles	RGB565 8 bits 3 cycles	RGB666 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr 8 bits 2 cycles	RGB565 16 bits 2 cycles	YCbCr 16 bits 1 cycle	YCbCr 16 bits 1 cycle	YCbCr 20 bits 1 cycle
IPUx_CSIx_DATA00									0	C0
IPUx_CSIx_DATA01									0	C1
IPUx_CSIx_DATA02									C0	C2
IPUx_CSIx_DATA03									C1	C3
IPUx_CSIx_DATA04							B0	C0	C2	C4
IPUx_CSIx_DATA05							B1	C1	C3	C5
IPUx_CSIx_DATA06							B2	C2	C4	C6
IPUx_CSIx_DATA07							B3	C3	C5	C7
IPUx_CSIx_DATA08							B4	C4	C6	C8
IPUx_CSIx_DATA09							G0	C5	C7	C9
IPUx_CSIx_DATA10							G1	C6	0	Y0
IPUx_CSIx_DATA11							G2	C7	0	Y1
IPUx_CSIx_DATA12	**CSI_D0**	B0/G3	R2/G4/B2	R4/G4/B4	R0/G0/B0	Y0/C0	G3	Y0	Y0	Y2

IPUx_CSIx_DATA13	**CSI_D1**	B1/G4	R3/G5/B3	R5/G5/B5	R1/G1/B1	Y1/C1	G4	Y1	Y1	Y3
IPUx_CSIx_DATA14	**CSI_D2**	B2/G5	R4/G0/B4	R0/G0/B0	R2/G2/B2	Y2/C2	G5	Y2	Y2	Y4
IPUx_CSIx_DATA15	**CSI_D3**	B3/R0	R0/G1/B0	R1/G1/B1	R3/G3/B3	Y3/C3	R0	Y3	Y3	Y5
IPUx_CSIx_DATA16	**CSI_D4**	B4/R1	R1/G2/B1	R2/G2/B2	R4/G4/B4	Y4/C4	R1	Y4	Y4	Y6
IPUx_CSIx_DATA17	**CSI_D5**	G0/R2	R2/G3/B2	R3/G3/B3	R5/G5/B5	Y5/C5	R2	Y5	Y5	Y7
IPUx_CSIx_DATA18	**CSI_D6**	G1/R3	R3/G4/B3	R4/G4/B4	R6/G6/B6	Y6/C6	R3	Y6	Y6	Y8
IPUx_CSIx_DATA19	**CSI_D7**	G2/R4	R4/G5/B4	R5/G5/B5	R7/G7/B7	Y7/C7	R4	Y7	Y7	Y9

5.1.2 Serial Camera Interface

This section lists signals for the serial camera interface, also called MIPI-CSI2.

The *EACOM Board specification* defines an serial camera interface, MIPI-CSI2 with up to 4 lanes. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S141/287	CSI_CLK_P	CSI_CLK0P	I	Positive D-Phy differential clock line Receiver input	
S140/285	CSI_CLK_N	CSI_CLK0N	I	Negative D-Phy differential clock line Receiver input	
S138/281	CSI_D0_P	CSI_D0P	I	Positive D-Phy differential data line Receiver input , Lane 0	
S137/279	CSI_D0_N	CSI_D0N	I	Negative D-Phy differential data line Receiver input , Lane 0	
S135/275	CSI_D1_P	CSI_D1P	I	Positive D-Phy differential data line Receiver input , Lane 1	
S134/273	CSI_D1_N	CSI_D1N	I	Negative D-Phy differential data line Receiver input , Lane 1	
S132/269	CSI_D2_P	CSI_D2P	I	Positive D-Phy differential data line Receiver input , Lane 2	
S131/267	CSI_D2_N	CSI_D2N	I	Negative D-Phy differential data line Receiver input , Lane 2	
S129/263	CSI_D3_P	CSI_D3P	I	Positive D-Phy differential data line Receiver input , Lane 3	
S128/261	CSI_D3_N	CSI_D3N	I	Negative D-Phy differential data line Receiver input , Lane 3	

5.2 Display Interfaces

This section lists signals related to display output interfaces, like parallel RGB (Enhanced LCD Interface - eLCDIF), LVDS Display Bridge (LDB), HDMI and MIPI-DSI transmitters.

Chapter 9 - Multimedia in the IMX6DQRM presents an overview of the video graphics subsystem.

The i.MX 6X SoC has an advanced, feature rich display and video graphics subsystem with several key components:

- Video Processing Unit (VPU): a multi-standard high performance video/image CODEC
- Three Graphics Processing Units (GPUs)
    - 3D GPU: accelerating the generation of 3D graphics (OpenGL/ES) and vector graphics (OpenVG)
    - 2D GPU: acceleration the generation of 2D graphics (BitBLT)
    - OpenVG: acceleration of vector graphics (OpenVG)
- Two (identical) Image Processing Units (IPUs): providing connectivity to cameras and displays, related processing, synchronization and control
- Display interface bridges: providing optional translation from the digital display interface supported by the IPU to other interfaces:
    - LVDS bridge (LDB): providing up to two LVDS interfaces
    - HDMI transmitter
    - MIPI-DSI transmitter
- Two (identical) Display Content Integrity Checker (DCIC) are used to authenticate sensitive displayed data.
- A Video Data Order Adapter (VDOA): used to re-order video data from the "tiled" order used by the VPU to the conventional raster-scan order needed by the IPU.
- MIPI-CSI2 receiver
  This interface is presented in section 5.1.2 .

The picture below illustrates the display port multiplexing scheme.

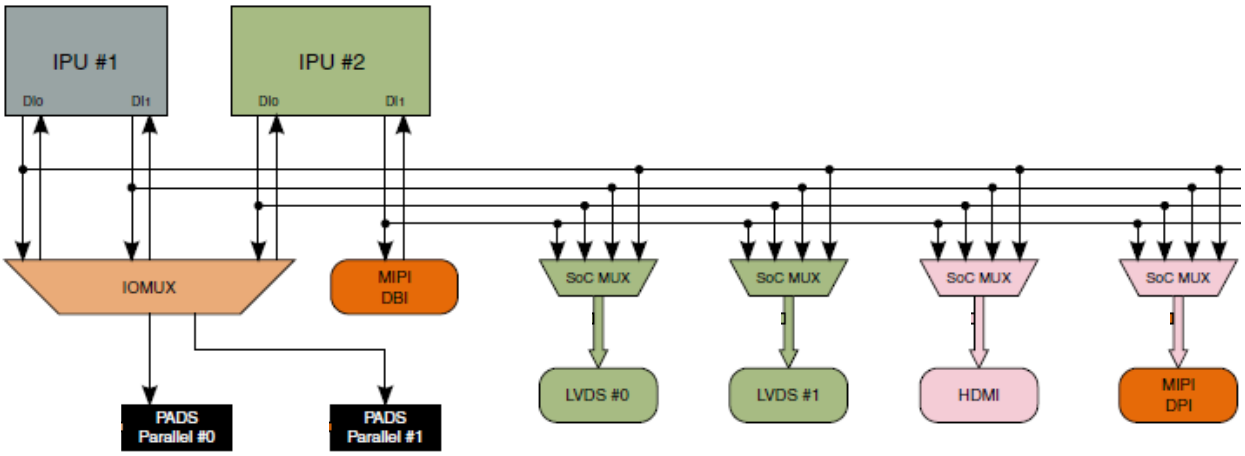


Figure 5 – Display Port Multiplexing Scheme

Four display ports exist, two per IPU. These can either be connected directly (2x parallel RGB interfaces) or via bridges (2x LVDS, HDMI and MIPI-DSI). Up to four displays can be active at the same time. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp.

The *EACOM Board specification* has allocated some additional support signals that are typically needed to implement a display interface. The table below list these signals. These are common for all display interfaces.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S56/111	BL_PWM	SD1_DATA2	O	PWM signal to control backlight contrast.	Signal is connected to PWM2_OUT
S55/109	BL_PWR_EN	EIM_WAIT	O	Power control for backlight. Active high	
S54/107	DISP_PWR_EN	EIM_BCLK	O	Power control for LCD power supply. Active high	Signal is connected to GPIO6_IO31
S53/105	TP_IRQ	EIM_AD13	I	Interrupt from touch controller	Signal is connected to GPIO3_IO13
S52/103	TP_RST	EIM_AD14	O	Reset signal to touch controller. Active low	Signal is connected to GPIO3_IO14
S47/93	I2C-A_SCL	CSI0_DATA09	I/O	Clock signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
S46/91	I2C-A_SDA	CSI0_DATA08	I/O	Data signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
S49/97	I2C-B_SCL	GPIO05	I/O	Clock signal of I2C channel B	It is recommended to connect the LVDS touch controller (if I2C interface) to this channel.
S48/95	I2C-B_SDA	GPIO06	I/O	Data signal of I2C channel B	It is recommended to connect the LVDS touch controller (if I2C interface) to this channel.
S51/101	I2C-C_SCL	KEY_COL3	I/O	Clock signal of I2C channel C	It is recommended to connect a HDMI interface to this channel. **Note:** signal must be level shifted when connected to HDMI connector.
S50/99	I2C-C_SDA	KEY_ROW3	I/O	Data signal of I2C channel C	It is recommended to connect a HDMI interface to this channel. **Note:** signal must be level shifted when connected to HDMI connector.

5.2.1 Parallel RGB LCD Interface

This section lists signals for the parallel RGB LCD interface.

The parallel RGB LCD interface, with 24-bit color, can support pixel data rates up to (about) 225 Mpixels/sec. That can drive for example:

- 1080p (1920x1080 pixel) at 60 fps (and 35% blanking intervals)
- WUXGA (1920x1200 pixels) at 60 fps
- WXGA+ (1680x1050 pixels) at 60 fps

The parallel RGB LCD interface is ideal for smaller, lower resolution displays. Note that due to EMI, LVDS, HDMI and MIPI-DSI might be better choices of interface for high resolution displays.

The *EACOM Board specification* defines a 24-bit parallel LCD interface. The table below lists the pin assignment according to *EA COM Board specification*. For best portability it is recommended to always

have the LCD interface running in 24-bit mode. If less bits are needed in a specific LCD implementation the LSB bits of each color is just ignored, see the three rightmost columns.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Color Config. for 16-bit 565RGB	Color Config. for 18-bit 666RGB	Color Config. for 16-bit 565RGB if interface set to 24-bit	Color Config. for 18-bit 666RGB if interface set to 24-bit	Color Config. for 24-bit 888RGB
S75/149	LCD_DATA00	DISP0_DATA00	O	B0	B0			B0
S76/157	LCD_DATA01	DISP0_DATA01	O	B1	B1			B1
S77/159	LCD_DATA02	DISP0_DATA02	O	B2	B2		B2	B2
S78/161	LCD_DATA03	DISP0_DATA03	O	B3	B3	B3	B3	B3
S79/163	LCD_DATA04	DISP0_DATA04	O	B4	B4	B4	B4	B4
S80/165	LCD_DATA05	DISP0_DATA05	O	G0	B5	B5	B5	B5
S81/167	LCD_DATA06	DISP0_DATA06	O	G1	G0	B6	B6	B6
S82/169	LCD_DATA07	DISP0_DATA07	O	G2	G1	B7	B7	B7
S66/131	LCD_DATA08	DISP0_DATA08	O	G3	G2			G0
S67/133	LCD_DATA09	DISP0_DATA09	O	G4	G3			G1
S68/135	LCD_DATA10	DISP0_DATA10	O	G7	G4	G2	G2	G2
S69/137	LCD_DATA11	DISP0_DATA11	O	R0	G5	G3	G3	G3
S70/139	LCD_DATA12	DISP0_DATA12	O	R1	R0	G4	G4	G4
S71/141	LCD_DATA13	DISP0_DATA13	O	R2	R1	G5	G5	G5
S72/143	LCD_DATA14	DISP0_DATA14	O	R3	R2	G6	G6	G6
S73/145	LCD_DATA15	DISP0_DATA15	O	R4	R3	G7	G7	G7
S58/115	LCD_DATA16	DISP0_DATA16	O		R4			R0
S59/117	LCD_DATA17	DISP0_DATA17	O		R5			R1
S60/119	LCD_DATA18	DISP0_DATA18	O				R2	R2
S61/121	LCD_DATA19	DISP0_DATA19	O			R3	R3	R3
S62/123	LCD_DATA20	DISP0_DATA20	O			R4	R4	R4
S63/125	LCD_DATA21	DISP0_DATA21	O			R5	R5	R5
S64/127	LCD_DATA22	DISP0_DATA22	O			R6	R6	R6
S65/129	LCD_DATA23	DISP0_DATA23	O			R7	R7	R7
S85/175	LCD_HSYNC	DI0_PIN02	O	Horizontal (line) synchronization				
S86/177	LCD_VSYNC	DI0_PIN03	O	Vertical (frame) synchronization				
S87/179	LCD_ENABLE	DI0_PIN15	O	Data enable				
S83/171	LCD_CLK	DI0_DISP_CLK	O	Pixel (dot) clock				

5.2.2 LVDS Interfaces

This section lists signals for the two LVDS interfaces.

The purpose of the LVDS interface is to serialize the parallel RGB and control signals to an external display. The parallel RGB data stream can be either 18 or 24 bits wide. The three control signals; HSYNC, VSYNC and ENABLE along with the pixel/dot clock are also serialized.

The LVDS ports may be used as follows:

- One single channel output
- One dual channel output: single input, split to two output channels

- Two identical outputs: single input sent to both output channels
- Two independent outputs: two inputs sent, each, to a different output channel

For single channel output, the LVDS interface supports resolutions up to WXGA 1366x768 pixels @ 60 frames per second (85MHz pixel clock maximum)

For dual channel output, the LVDS interfaces supports resolutions up to UXGA 1600x1200 pixels @ 60 frames per second (170MHz pixel clock maximum)

Two signal mappings are supported. Below is the so called *SPWG/PSWG/VESA 18/24 bpp Data Mapping*.

Serializer Input	Slot 0	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6
LVDS_DATA0	G0	R5	R4	R3	R2	R1	R0
LVDS_DATA1	B1	B0	G5	G4	G3	G2	G1
LVDS_DATA2	DE	VS	HS	B5	B4	B3	B2
LVDS_DATA3 (only in 24-bit data)	N/A	B7	B6	G7	G6	R7	R6

The other signal mapping is called *JEIDA 24bpp Data Mapping*.

Serializer Input	Slot 0	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6
LVDS_DATA0	G2	R7	R6	R5	R4	R3	R2
LVDS_DATA1	B3	B2	G7	G6	G5	G4	G3
LVDS_DATA2	DE	VS	HS	B7	B6	B5	B4
LVDS_DATA3	N/A	B1	B0	G1	G0	R1	R0

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S42/83	LVDS0_D0_N	LVDS0_TX0_N	O	Differential data pair #0, negative signal	
S41/81	LVDS0_D0_P	LVDS0_TX0_P	O	Differential data pair #0, positive signal	
S39/77	LVDS0_D1_N	LVDS0_TX1_N	O	Differential data pair #1, negative signal	
S38/75	LVDS0_D1_P	LVDS0_TX1_P	O	Differential data pair #1, positive signal	
S36/71	LVDS0_D2_N	LVDS0_TX2_N	O	Differential data pair #2, negative signal	
S35/69	LVDS0_D2_P	LVDS0_TX2_P	O	Differential data pair #2, positive signal	
S33/65	LVDS0_D3_N	LVDS0_TX3_N	O	Differential data pair #3, negative signal	Pair not used in 18-bit color depth.
S32/63	LVDS0_D3_P	LVDS0_TX3_P	O	Differential data pair #3, positive signal	Pair not used in 18-bit color depth.
S45/89	LVDS0_CLK_N	LVDS0_CLK_N	O	Differential clock pair, negative signal	
S44/87	LVDS0_CLK_P	LVDS0_CLK_P	O	Differential clock pair, positive signal	
S27/53	LVDS1_D0_N	LVDS1_TX0_N	O	Differential data pair #0, negative signal	
S26/51	LVDS1_D0_P	LVDS1_TX0_P	O	Differential data pair #0, positive signal	
S24/47	LVDS1_D1_N	LVDS1_TX1_N	O	Differential data pair #1, negative signal	
S23/45	LVDS1_D1_P	LVDS1_TX1_P	O	Differential data pair #1, positive signal	
S21/41	LVDS1_D2_N	LVDS1_TX2_N	O	Differential data pair #2, negative signal	
S20/39	LVDS1_D2_P	LVDS1_TX2_P	O	Differential data pair #2, positive signal	
S18/35	LVDS1_D3_N	LVDS1_TX3_N	O	Differential data pair #3, negative signal	Pair not used in 18-bit

					color depth.
S17/33	LVDS1_D3_P	LVDS1_TX3_P	O	Differential data pair #3, positive signal	Pair not used in 18-bit color depth.
S30/59	LVDS1_CLK_N	LVDS1_CLK_N	O	Differential clock pair, negative signal	
S29/57	LVDS1_CLK_P	LVDS1_CLK_P	O	Differential clock pair, positive signal	

5.2.3 HDMI Interface

This section lists signals for the High Definition Multimedia Interface - HDMI interface.

HDMI is capable of transferring uncompressed video, audio, and data with video pixel rates typically between 25 MHz and (up to) 266 MHz. HDMI uses Transition-minimized differential signaling (TMDS) with three data pairs and one clock pair. An optional Consumer Electronics Control (CEC) protocol provides high-level control functions between all of the various audiovisual products in a user's environment.

The interface supports all CEA-861-E video formats up to 1080p at 60Hz and 720p/1080i at 120Hz.

Note that the I/O pins of the i.MX 6 are not 5V tolerant. In order not to damage the i.MX 6 SoC and for proper functionality the I2C, Hot Plug Detect and the CEC signals **must** be correctly level shifted.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P23/46	HDMI_TX_CLK_N	HDMI_CLKM	O	Differential clock pair, negative signal	
P24/48	HDMI_TX_CLK_P	HDMI_CLKP	O	Differential clock pair, positive signal	
P26/52	HDMI_D0M	HDMI_D0M	O	Differential data pair #0, negative signal	
P27/54	HDMI_D0P	HDMI_D0P	O	Differential data pair #0, positive signal	
P29/58	HDMI_D1M	HDMI_D1M	O	Differential data pair #1, negative signal	
P30/60	HDMI_D1P	HDMI_D1P	O	Differential data pair #1, positive signal	
P32/64	HDMI_D2M	HDMI_D2M	O	Differential data pair #2, negative signal	
P33/66	HDMI_D2P	HDMI_D2P	O	Differential data pair #2, positive signal	
P34/68	HDMI_CEC	EIM_A25	I/O	Alternative function HDMI_TX_CEC_LINE	**Note:** signal must be level shifted when connected to HDMI connector.
P28/56	HDMI_HPD	HDMI_HPD	I	Hot Plug Detect input	**Note:** signal must be level shifted when connected to HDMI connector.

The HDMI interface carries a VESA Data Display Channel (DDC). It is an I2C channel and channel C has been allocated for this. The DDC is used for configuration and status exchange with the display.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S51/101	I2C-C_SCL	KEY_COL3	I/O	Clock signal of I2C channel C	**Note:** signal must be level shifted when connected to HDMI connector. Can also be connected to alternative signal: HDMI_TX_DDC_SCL
S50/99	I2C-C_SDA	KEY_ROW3	I/O	Data signal of I2C channel C	**Note:** signal must be level shifted when connected to HDMI connector. Can also be connected to alternative signal: HDMI_TX_DDC_SDA

5.2.4 MIPI-DSI Interface

This section lists signals for the MIPI-DSI interface. The interface supports display resolutions up to 1280x768 pixels (XVGA) with 24-bit resolution.

The *EACOM Board specification* has not allocated pins for this interface, since it is mostly used in very high volume applications (where COM boards are not so commonly used). The MIPI-DSI interface supports two data lanes and together with the clock signal, six pins as been used.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S102/209	COM specific	DSI_CLK0M	O	Differential clock pair, negative signal	
S103/211	COM specific	DSI_CLK0P	O	Differential clock pair, positive signal	
S99/203	COM specific	DSI_D0M	I/O	Differential data pair #0, negative signal	
S100/205	COM specific	DSI_D0P	I/O	Differential data pair #0, positive signal	
S96/197	AIN1	DSI_D1M	O	Differential data pair #1, negative signal	
S97/199	AIN0	DSI_D1P	O	Differential data pair #1, positive signal	

5.3 Digital Audio Interfaces: Synchronous Serial Interface and AUDMUX

This section lists signals related to the Synchronous Serial Interfaces (SSI) and Digital Audio Mux (AUDMUX) functions.

The i.MX 6 SoC contains an audio subsystem. It consists of three Synchronous Serial Interfaces (SSI1-SSI3). The SSI block is a full-duplex serial port that allows communication with external devices using a variety of serial protocols (like SSI normal/network, I2S and AC-97), up to 24-bits per word and different clock/frame options.

The three SSI interfaces are not directly connected to the IOMUX, but instead to a block called Digital Audio Mux (AUDMUX). The AUDMUX routes audio data (it does not decode or process the data) and can be operational even when the SoC is in a low-power mode.

The picture below illustrates the programmable interconnect fabric that AUDMUX implements. There are four ports that are connected to IOMUX; AUD3, AUD4, AUD5, AUD6.

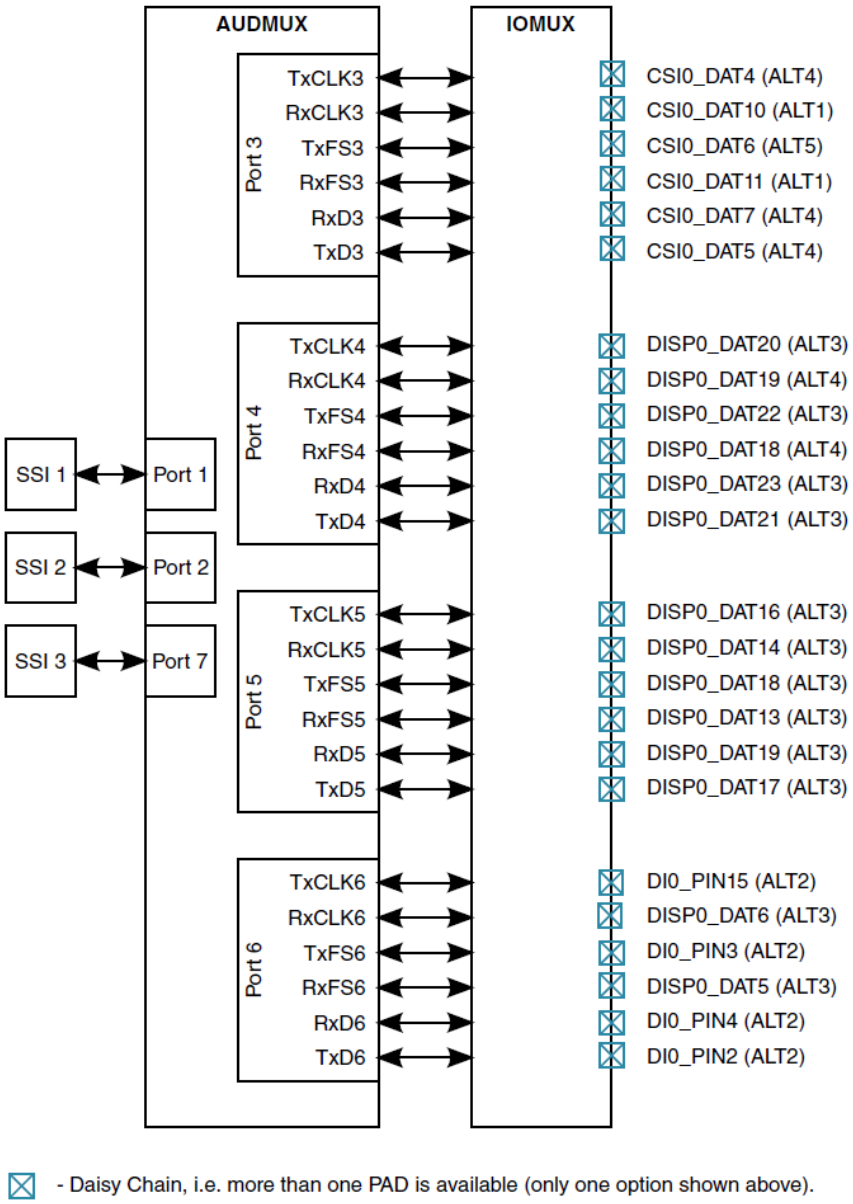


Figure 6 – i.MX 6 AUDMUX System Block Diagram

The table below lists pins that have been allocated according to the *EACOM Board specification*. AUDMUX port #3 (AUD3) is used with **synchronous** transmit and receive sections (meaning that transmit and receive share the clock and frame synch signals).

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S5/9	AUDIO_RXD	CSI0_DATA07	I	Data receive signal Ch#3	Alternative function AUD3_RXD
S6/11	AUDIO_TXC	CSI0_DATA04	O	Transmit clock signal Ch#3. Also work as Receive clock signal Ch#3	Alternative function AUD3_TXC
S7/13	AUDIO_TXD	CSI0_DATA05	O	Data transmit signal Ch#3	Alternative function AUD3_TXD
S4/7	AUDIO_TXFS	CSI0_DATA06	O	Transmit Frame sync signal Ch#3. Also work as Receive Frame sync signal Ch#3	Alternative function AUD3_TXFS
S8/15	AUDIO_MCLK	GPIO_19	O	Clock output signal	Alternative function CCM_CLKO1

The signal AUDIO_MCLK is included in the digital audio interface since a codec often requires this clock (but not always). Signal CCM_CLKO1 is setup to generate the clock signal. Alternative locations for this signals are listed below.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S90/185	AIN7	CSI0_HSYNC	O	Clock output signal	Alternative function CCM_CLKO1
P75/158	USB_H1_PWR_EN	GPIO00	O	Clock output signal	Alternative function CCM_CLKO1

Besides the AUDMUX port 3 signals allocated in the *EACOM Board specification* there are more (alternative) pins for the AUDMUX port 3 (AUD3) interface. The table below lists these pins.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P129/266	UART-C_TXD	CSI0_DATA10	I	Receive clock signal Ch#3	Alternative function AUD3_RXC
P128/264	UART-C_RXD	CSI0_DATA11	I	Receive Frame sync signal Ch#3	Alternative function AUD3_RXFS

The table below lists pins available for the AUDMUX port 4 (AUD4) interface.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S61/121	LCD_R3	DISP0_DATA19	I	Receive clock signal Ch#4	Alternative function AUD4_RXC
P8/16	SD_CMD	SD2_CMD	I	Receive clock signal Ch#4	Alternative function AUD4_RXC
S65/129	LCD_R7	DISP0_DATA23	I	Data receive signal Ch#4	Alternative function AUD4_RXD
P6/12	SD_D0	SD2_DATA0	I	Data receive signal Ch#4	Alternative function AUD4_RXD
S60/119	LCD_R2	DISP0_DATA18	I	Receive Frame sync signal Ch#4	Alternative function AUD4_RXFS
P7/14	SD_CLK	SD2_CLK	I	Receive Frame sync signal Ch#4	Alternative function AUD4_RXFS
S62/123	LCD_R4	DISP0_DATA20	O	Transmit clock signal Ch#4	Alternative function AUD4_TXC
P9/18	SD_D3	SD2_DATA3	O	Transmit clock signal Ch#4	Alternative function AUD4_TXC
S63/125	LCD_R5	DISP0_DATA21	O	Data transmit signal Ch#4	Alternative function AUD4_TXD
P10/20	SD_D2	SD2_DATA2	O	Data transmit signal Ch#4	Alternative function AUD4_TXD
S64/127	LCD_R6	DISP0_DATA22	O	Transmit Frame sync signal Ch#4	Alternative function AUD4_TXFS
P5/10	SD_D1	SD2_DATA1	O	Transmit Frame sync signal Ch#4	Alternative function AUD4_TXFS

The table below lists pins available for the AUDMUX port 5 (AUD5) interface.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S72/143	LCD_G6	DISP0_DATA14	I	Receive clock signal Ch#5	Alternative function AUD5_RXC
P111/230	COM specific	EIM_D25	I	Receive clock signal Ch#5	Alternative function AUD5_RXC
S61/121	LCD_R3	DISP0_DATA19	I	Data receive signal Ch#5	Alternative function AUD5_RXD
P92/192	COM specific	KEY_ROW1	I	Data receive signal Ch#5	Alternative function AUD5_RXD
S71/141	LCD_G5	DISP0_DATA13	I	Receive Frame sync signal Ch#5	Alternative function AUD5_RXFS
P112/232	COM specific	EIM_D24	I	Receive Frame sync signal Ch#5	Alternative function AUD5_RXFS
S58/115	LCD_R0	DISP0_DATA16	O	Transmit clock signal Ch#5	Alternative function AUD5_TXC
P95/198	COM specific	KEY_COL0	O	Transmit clock signal Ch#5	Alternative function AUD5_TXC
S59/117	LCD_R1	DISP0_DATA17	O	Data transmit signal Ch#5	Alternative function AUD5_TXD

P93/194	COM specific	KEY_ROW0	O	Data transmit signal Ch#5	Alternative function AUD5_TXD
S60/119	LCD_R2	DISP0_DATA18	O	Transmit Frame sync signal Ch#5	Alternative function AUD5_TXFS
P94/196	COM specific	KEY_COL1	O	Transmit Frame sync signal Ch#5	Alternative function AUD5_TXFS

The table below lists pins available for the AUDMUX port 6 (AUD6) interface.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S81/167	LCD_B6	DISP0_DATA6	I	Receive clock signal Ch#6	Alternative function AUD6_RXC
S84/173	GPIO7	DI0_PIN4	I	Data receive signal Ch#6	Alternative function AUD6_RXD
S80/165	LCD_B5	DISP0_DATA5	I	Receive Frame sync signal Ch#6	Alternative function AUD6_RXFS
S87/179	LCD_ENABLE	DI0_PIN15	O	Transmit clock signal Ch#6	Alternative function AUD6_TXC
S85/175	LCD_HSYNC	DI0_PIN2	O	Data transmit signal Ch#6	Alternative function AUD6_TXD
S86/177	LCD_VSYNC	DI0_PIN3	O	Transmit Frame sync signal Ch#6	Alternative function AUD6_TXFS

5.4 Digital Audio Interfaces: ESAI

This section lists signals related to the Enhanced Serial Audio Interface (ESAI) function.

EASI is part of the i.MX 6 SoC audio subsystem. It provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, Sony/Phillips Digital Interface (SPDIF) transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.

There are no specific ESAI pins defined in the *EACOM Board specification*. ESAI pins are only available as alternative functions on certain pins. The table below lists the available pins.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P139/286	GPIO2	GPIO_1	I/O	RX serial bit clock	Alternative function ESAI_RX_CLK
P66/132	USB_O1_OTG_ID	ENET_RX_ER	I/O	RX high frequency clock	Alternative function ESAI_RX_HF_CLK
P76/160	USB_H1_OC	GPIO_3	I/O	RX high frequency clock	Alternative function ESAI_RX_HF_CLK
S116/237	CSI_MCLK	NANDF_CS2	I/O	ESAI_TX0 serial transmit data	Alternative function ESAI_TX0
P104/216	COM specific	NANDF_CS3	I/O	ESAI_TX1 serial transmit data	Alternative function ESAI_TX1
S49/97	I2C-B_SCL	GPIO_5	I/O	ESAI_TX2 serial transmit data or ESAI_RX3 serial receive data	Alternative function ESAI_TX2_RX3 Note that the pin is pre-allocated as I2C2_SCL and has on-board 2.2Kohm pull-up resistor. It is possible to use this pin but not recommended.
S10/19	SPDIF_IN	GPIO_16	I/O	ESAI_TX3 serial transmit data or ESAI_RX2 serial receive data	Alternative function ESAI_TX3_RX2
S2/3	MQS_LEFT	GPIO_7	I/O	ESAI_TX4 serial transmit data or ESAI_RX1 serial receive data	Alternative function ESAI_TX4_RX1
S1/1	MQS_RIGHT	GPIO_8	I/O	ESAI_TX5 serial transmit data or ESAI_RX0 serial receive data	Alternative function ESAI_TX5_RX0
S48/95	I2C-B_SDA	GPIO_6	I/O	TX serial bit clock	Alternative function ESAI_TX_CLK Note that the pin is pre-allocated as I2C2_SCL and has on-board 2.2Kohm pull-up resistor. It is possible to use this pin but not recommended.
P140/288	GPIO1	GPIO_4	I/O	TX high frequency clock	Alternative function ESAI_TX_HF_CLK

5.5 Digital Audio Interfaces: S/PDIF

This section lists signals related to the Sony/Philips Digital Interface (SPDIF) function.

The i.MX 6 SoC has one SPDIF interface, which is a stereo transceiver that allows the processor to receive and transmit digital audio according to the AES/EBU IEC 60958 standard.

The *EACOM Board specification* defines one input and one output SPDIF interface. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S10/19	SPDIF_IN	GPIO_16	I	Input line	
S11/21	SPDIF_OUT	ENET_RXD0	O	Output line signal	

There are alternative locations for the SPDIF pins as well as some clock signals that are not used very often. The table below lists these alternative pin locations.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P74/148	USB_O1_OC	EIM_D21	I	Input line	Alternative function SPDIF_IN
P66/132	USB_O1_OTG_ID	ENET_RX_ER	I	Input line	Alternative function SPDIF_IN
S51/101	I2C-C_SCL	KEY_COL3	I	Input line	Alternative function SPDIF_IN Note that the pin is pre-allocated as I2C2_SCL and has on-board 2.2Kohm pull-up resistor. It is possible to use this pin but not recommended.
P73/146	USB_O1_PWR_EN	EIM_D22	O	Output line signal	Alternative function SPDIF_OUT
S8/15	AUDIO_MCLK	GPIO_19	O	Output line signal	Alternative function SPDIF_OUT
S1/1	MQS_RIGHT	GPIO_8	O	Output line signal	Alternative function SPDIF_SR_CLK
S2/3	MQS_LEFT	GPIO_7	O	Lock signal	Alternative function SPDIF_LOCK

5.6 Ethernet

This section lists signals related to the Ethernet interface.

The i.MX 6 has one Gigabit Ethernet controllers (10/100/1000Mbps) that is IEEE1588 compliant. There is one 10/100/1000 Mbps Ethernet interfaces on the board. Atheros AR8031 Integrated 10/100/1000 Mbps Ethernet Transceiver is used as external PHY and is connected via the RGMII interface to the i.MX 6 SoC.

The *EACOM Board Specification* defines two Ethernet interfaces. The i.MX 6 SoC Ethernet interface is assigned to ETH1. ETH2 is left unconnected.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals plus three link indicator activity signals. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

EACOM Board Pin	EACOM Board Name	AR8031 Pin	I/O	Description	Remarks
P39/78	ETH1_TRXP0	AR8031 #1 pin 11	I/O	Media Dependent Interface	
P40/80	ETH1_TRXN0	AR8031 #1 pin 12	I/O	Media Dependent Interface	
P36/72	ETH1_TRXP1	AR8031 #1 pin 14	I/O	Media Dependent Interface	

P37/74	ETH1_TRXN1	AR8031 #1 pin 15	I/O	Media Dependent Interface	
P48/96	ETH1_TRXP2	AR8031 #1 pin 17	I/O	Media Dependent Interface	
P47/94	ETH1_TRXN2	AR8031 #1 pin 18	I/O	Media Dependent Interface	
P45/90	ETH1_TRXP3	AR8031 #1 pin 20	I/O	Media Dependent Interface	
P44/88	ETH1_TRXN3	AR8031 #1 pin 21	I/O	Media Dependent Interface	
P42/84	ETH1_LED_ACT	AR8031 #1 pin 23	O	LED indicator output	Signal toggles during TX/RX activity.
P43/86	ETH1_LED_LINK	AR8031 #1 pin 26	O	LED indicator output	Signal high when 100M link is active.
P41/82	ETH1_LED_LINK1000	AR8031 #1 pin 24	O		Signal high when 1000M link is connected or active.
P53/106	ETH2_TRXP0				ETH2 interface not connected
P54/108	ETH2_TRXN0				ETH2 interface not connected
P50/100	ETH2_TRXP1				ETH2 interface not connected
P51/102	ETH2_TRXN1				ETH2 interface not connected
P62/124	ETH2_TRXP2				ETH2 interface not connected
P61/122	ETH2_TRXN2				ETH2 interface not connected
P59/118	ETH2_TRXP3				ETH2 interface not connected
P58/116	ETH2_TRXN3				ETH2 interface not connected
P56/112	ETH2_LED_ACT				ETH2 interface not connected
P57/114	ETH2_LED_LINK100				ETH2 interface not connected
P55/110	ETH2_LED_LINK1000				ETH2 interface not connected

The external PHYs can be powered down in order to lower the power consumption to a minimum.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected.

Below is a list of suggested magnetics for 10/100/1000 Mbps Gigabit Ethernet operation:

Vendor	P/N	Package	Temp	Configuration
HanRun	HR911060C	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
Halo	HFJ11-1G02E	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
Pulse Electronics (Recommended by Atheros)	H5007	24-pin SOIC-W	0 - 70° Celsius	HP Auto-MDIX
Halo	TG1G-S002NZRL	24-pin SOIC-W	-40 - 85° Celsius	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	-40 - 85° Celsius	HP Auto-MDIX
Halo	TG1G-E012NZRL	24-pin SOIC-W	-40 - 85° Celsius	HP Auto-MDIX

5.7 FlexCAN

This section lists signals related to the Controller Area Network (CAN) interface.

The i.MX 6 SoC has two Flexible Controller Area Network (FlexCAN) interfaces that supports bitrates of up to 1Mbps each. The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification, which supports both standard and extended message frames.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S15/29	CAN1_RX	KEY_ROW2	I	CAN port 1 receive signal	Default location for EACOM Board spec.
S14/27	CAN1_TX	KEY_COL2	O	CAN port 1 transmit signal	Default location for EACOM Board spec.
S13/25	CAN2_RX	KEY_ROW4	I	CAN port 2 receive signal	Default location for EACOM Board spec.
S12/23	CAN2_TX	KEY_COL4	O	CAN port 2 transmit signal	Default location for EACOM Board spec.
S1/1	MQS_RIGHT	GPIO_8	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal
P16/32	MMC_CLK	SD3_CLK	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal
S2/3	MQS_LEFT	GPIO_7	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
P18/36	MMC_CMD	SD3_CMD	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
P12/24	MMC_D1	SD3_DAT1	I	CAN port 2 receive signal	Alternative location for CAN2_RX signal
P13/26	MMC_D0	SD3_DAT0	O	CAN port 2 transmit signal	Alternative location for CAN2_TX signal

5.8 GPIOs

This section lists signals related to General Purpose Input/Output (GPIO) functionality.

Many pins have GPIO functionality that can be enabled (via pin multiplexing). All GPIO pins can be used to generate interrupts as well as be wakeup sources.

The *EACOM Board specification* defines only a few GPIOs and they are listed in the table below. The pins that cannot be configured as GPIOs are Ethernet, USB, PCIe, LVDS, HDMI, SATA, MIPI-CSI and MIPI-DSI. I2C pins can be GPIOs but are unsuitable since I2C-A is used on-board and I2C-B and I2C-C have 2.2Kohm on-board pull-up resistors.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P140/288	GPIO1	GPIO_4	I/O	GPIO	GPIO1 controlled by alternative pin function GPIO1_IO04
P139/286	GPIO2	GPIO_1	I/O	GPIO	GPIO2 controlled by alternative pin function GPIO1_IO01
P4/8	GPIO3	SD3_RESET	I/O	GPIO	GPIO3 controlled by alternative pin function GPIO7_IO08
P3/6	GPIO4	NAND_WP	I/O	GPIO	GPIO4 controlled by alternative pin function GPIO6_IO09
P2/4	GPIO5	NAND_READY	I/O	GPIO	GPIO5 controlled by alternative pin function GPIO6_IO10
P1/2	GPIO6	NAND_CS0	I/O	GPIO	GPIO6 controlled by alternative pin function GPIO6_IO11
S84/173	GPIO7	DI0_PIN04	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO4_IO20
S34/67	GPIO8	EIM_ADDR25	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO5_IO02
S19/37	GPIO9	NAND_CLE	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO6_IO07

5.9 I2C

This section lists signals related to the Inter-Integrated Circuit (I2C) interface.

The i.MX 6 SoC has three I2C interfaces. All of these are assigned in the *EACOM Board Specification*. i.MX 6 I2C channel #1 is assigned to EACOM I2C channel A. I2C channel #3 is assigned to EACOM I2C channel B. I2C channel #2 is assigned to EACOM I2C channel C.

Pin assignment for I2C channel A cannot be changed since this channel is used on the *iMX6 COM board* (for PMIC and E2PROM communication). It is recommended not to change pin assignment since for EACOM I2C channel B and C (I2C channel #3 and #2, respectively) since these pins have 2.2Kohm pull-up resistors.

The table below lists the pin assignment as well as alternative pin locations.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S47/93	I2C-A_SCL	CSI0_DATA09	I/O	Clock signal of I2C channel #1	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S46/91	I2C-A_SDA	CSI0_DATA08	I/O	Data signal of I2C channel #1	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S49/97	I2C-B_SCL	GPIO_5	I/O	Clock signal of I2C channel #3	Signal has on-board 2.2Kohm pullup resistor.
S48/95	I2C-B_SDA	GPIO_6	I/O	Data signal of I2C channel #3	Signal has on-board 2.2Kohm pullup resistor.
S51/101	I2C-C_SCL	KEY_COL3	I/O	Clock signal of I2C channel #2	Signal has on-board 2.2Kohm pullup resistor.
S50/99	I2C-C_SDA	KEY_ROW3	I/O	Data signal of I2C channel #2	Signal has on-board 2.2Kohm pullup resistor.

Note that the following two positions for I2C interfaces are not allowed:

- I2C1_SCL on i.MX 6 pin EIM_D21 should not be used. I2C channel #1 is allocated on another pin.
- I2C1_SDA on i.MX 6 pin EIM_D28 should not be used. I2C channel #1 is allocated on another pin.

i.MX 6 I2C interface #2 can are located on the following pins (as alternative functions), but note that these locations are not recommended since the *EACOM Board specification* has allocated this function on another pin, see above.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P80/168	USB_H1_SSTXN	EIM_EB2	I/O	Clock signal of I2C channel #2	I2C2_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
P84/176	USB_H1_SSRXP	EIM_D16	I/O	Data signal of I2C channel #2	I2C2_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.

i.MX 6 I2C interface #3 can are located on the following pins (as alternative functions).

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P83/174	USB_H1_SSRXN	EIM_D17	I/O	Clock signal of I2C channel #3	I2C3_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
P76/160	USB_H1_OC	GPIO_3	I/O	Clock signal of I2C channel #3	I2C3_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
P81/170	USB_H1_SSTXP	EIM_D18	I/O	Data signal of I2C channel #3	I2C3_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
S10/19	SPDIF_IN	GPIO_16	I/O	Data signal of I2C channel #3	I2C3_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.

5.10 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 6 SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the four/two ARM Cortex-A9 cores. The SJC complies with JTAG TAP standards. The i.MX 6 SoC use the JTAG port for production, testing, and system debugging.

The JTAG signals are not available on the MXM3 edge connector. Instead the signals are available via a 10 pos FPC connector, see picture below for location and orientation.

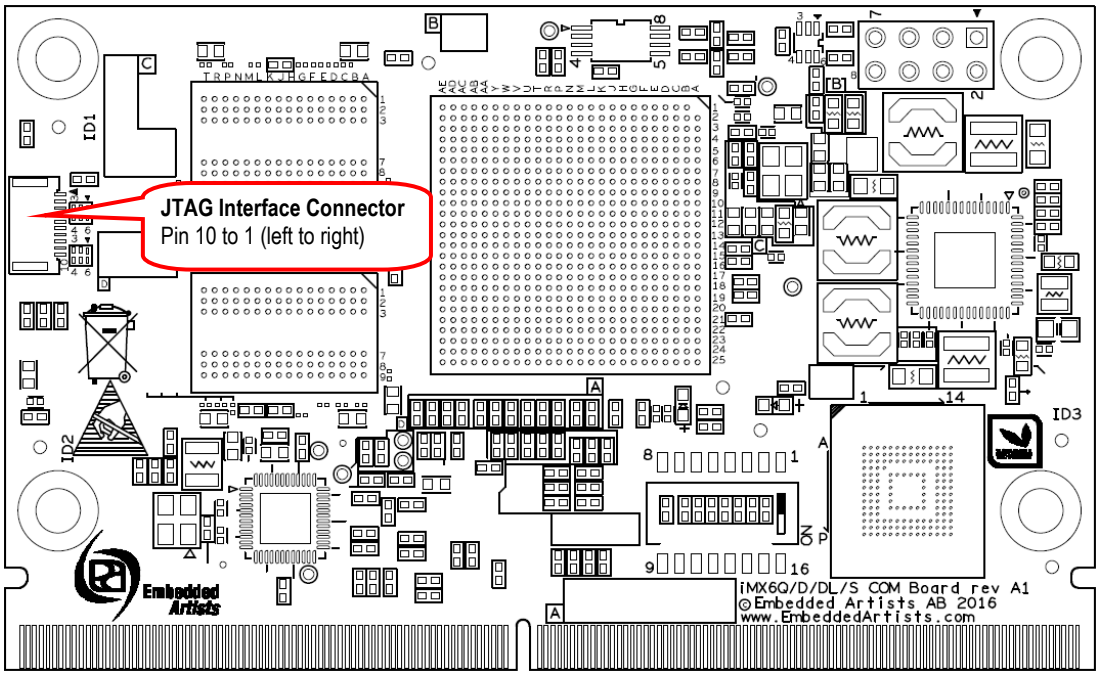


Figure 7 – iMX6 COM Board, Top Side

The table below lists the 10 signals on the JTAG connector.

J1 Pin Number	Connected to i.MX 6 Ball Name	I/O	Description	Remarks
1	NVCC_JTAG	O	Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.3V.
2	JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	JTAG_TCK	I	JTAG signal TCK	
5			Ground	
6	JTAG_TDO	O	JTAG signal TDO	
7	JTAG_MOD	I		Signal shall always be connected to ground. Signal has a 1Kohm pulldown resistor and can be left floating.
8	JTAG_TDI	I	JTAG signal TDI	
9	JTAG_TRST	I	JTAG signal TRST	Signal has a 10Kohm pullup resistor.
10	JTAG_SRST	I	System reset	Signal is active low and controls internal system, reset via buffer. Signal has a 10K ohm pullup resistor.

The *iMX6 Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

5.11 PCI Express

This section lists signals related to the PCI Express interface.

The i.MX 6 SoC has a single lane PCI Express (PCIe) interface. The interface is compliant with the PCIe 2.0 specification that supports 5Gbit/s data rate. PCIe 2.0 is backward compatible with the PCIe 1.1 standard that supports 2.5Gbit/s data rate.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S150/305	PCIE_CLK_P	CCM_CLK1_P	O	100 MHz reference clock, positive signal in differential pair	
S151/307	PCIE_CLK_N	CCM_CLK1_N	O	100 MHz reference clock, negative signal in differential pair	
S153/311	PCIE_TX_P	PCIE_TX_P	O	Transmit data, positive signal in differential pair	
S154/313	PCIE_TX_N	PCIE_TX_N	O	Transmit data, negative signal in differential pair	
S156/317	PCIE_RX_P	PCIE_RX_P	I	Receive data, positive signal in differential pair	
S157/319	PCIE_RX_N	PCIE_RX_N	I	Receive data, negative signal in differential pair	

A typical PCIe interface also has a USB Host, a I2C interface and (typically) three control signals; wakeup (input to iMX6), disable and reset (outputs from iMX6). These interfaces and control signals are not specifically defined in the *EACOM Board specification* and is up to each carrier board design to assign/allocate.

5.12 Power Management

This section lists signals related to power management, i.e., reset and external power supplies.

EACOM Board Pin	EACOM Board Name	I/O	Description	Remarks
P143/294	RESET_OUT	O	Reset output, active low	Open drain output. Driven low during reset. 1.5K pull-up resistor to VIN.
P142/292	RESET_IN	I	Reset input, active low	Pull signal low to activate reset. No need to pull signal high externally. Connected to cathode of series diode, so logic level of driving signal can be anywhere between 1.5-5 V.
P141/290	PERI_PWR_EN	O	Enable signal (active high) for carrier board peripheral power supplies.	Uses pin GPIO_17 on the i.MX 6. More information about carrier board design can be found in *EACOM Board specification*.

5.13 Power Supply Signals

This section lists signals related to power supply.

EACOM Board Pin	EACOM Board Name	I/O	Description	Remarks
P147/302, P148/304, P149/306, P150/308, P151/310, P152/312, P153/314, P154/316, P155/318, P156/320	VIN	A	3.3V supply voltage	See technical specification for details about valid range.
P22/44, P25/50, P31/62, P35/70, P38/76, P46/92, P49/98, P52/104, P60/120, P63/126, P69/138, P77/162, P82/172, P88/184, P91/190, P118/244, P127/262, P144/296, S3/5, S9/17, S16/31, S22/43, S25/49, S28/55, S31/61, S37/73, S40/79, S43/85, S57/113, S74/147, S88/181, S98/201, S101/207, S104/213, S118/241, S127/259, S130/265, S133/271, S136/277, S139/283, S142/289, S145/295, S148/301, S149/303, S152/309, S155/315, S158/321	GND	A	Ground	
P145/298	VBAT	AI/AO	Power supply for MMPF0100 PMIC and i.MX 6 on-chip RTC. Connect to external primary (= non rechargeable) or secondary (= rechargeable) coin cell battery.	Connected to MMPF0100 PMIC, pin 42, LICELL. PMIC can be programmed to charge a secondary coin cell.

5.14 SATA

This section lists signals related to the Serial Advanced Technology Attachment (SATA) interface. The interface is also known as Serial ATA. Typically, the interface is used to connect/attach an SSD, mSATA SSD or hard drive.

The i.MX 6 SoC has a single link, Gen 2 SATA interface (compliant with the SATA rev 2.5 specification). The maximum transfer rate is 3Gbps. Gen 2 SATA is backward compatible with the Gen 1 standard that supports 1.5Gbit/s data rate.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S143/291	SATA_TX_P	SATA_TX_P	O	SATA transmit data, positive signal in differential pair	
S144/293	SATA_TX_N	SATA_TX_N	O	SATA transmit data, negative signal in differential pair	
S146/297	SATA_RX_N	SATA_RX_N	I	SATA receive data, negative signal in differential pair	
S147/299	SATA_RX_P	SATA_RX_P	I	SATA receive data, positive signal in differential pair	

5.15 PWM

This section lists signals related to Pulse Wide Modulators (PWM).

The i.MX 6 SoC has four PWM channels that are available via pin multiplexing. The generated signals has 16-bit resolution. PWM signals can be used to generate analogue signals (emulate a DAC) and also control intensity / brightness in display applications.

There are two PWM signals defined in the *EACOM Board specification*. One general PWM signal and one that is intended for backlight intensity control for displays. The latter can however be used as a general PWM signals also if backlight intensity control is not needed or control is arranged differently. The remaining PWM signals are available as alternative functions on certain pins.

The table below lists the pin assignment as well as alternative pin locations.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P138/284	PWM1	SD1_DATA3	O	PWM1_OUT signal	
S56/111	BL_PWM	SD1_DATA2	O	PWM2_OUT signal	
S66/131	LCD_G0	DISP0_DATA8	O	PWM1_OUT signal	Available as alternative signal. Note that PWM1_OUT is assigned by the EACOM Board specification to another location.
S67/133	LCD_G1	DISP0_DATA9	O	PWM2_OUT signal	Available as alternative signal. Note that PWM2_OUT is assigned by the EACOM Board specification to another location.
P139/286	GPIO2	GPIO_1	O	PWM2_OUT signal	Available as alternative signal. Note that PWM2_OUT is assigned by the EACOM Board specification to another location.
P119/246	SPI-B_SSEL	SD1_DATA1	O	PWM3_OUT signal	Available as alternative signal.
P120/248	SPI-B_MOSI	SD1_CMD	O	PWM4_OUT signal	Available as alternative signal.

5.16 SD/MMC

This section lists signals related to Ultra Secured Digital Host Controller (uSDHC) functions.

The i.MX 6 SoC has 4 uSDHC interfaces. One, uSDHC4, is allocated (on-board) for interface to eMMC Flash. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The features of the uSDHC module include the following:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The *EACOM Board specification* defines one 4-databit uSDHC interface (uSDHC2) and one 8-databit uSDHC interface (uSDHC4). The remaining uSDHC signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P7/14	SD_CLK	SD2_CLK	O	Clock for MMC/SD/SDIO card	
P8/16	SD_CMD	SD2_CMD	I/O	CMD line connect to card	
P6/12	SD_D0	SD2_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
P5/10	SD_D1	SD2_DATA1	I/O	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	
P10/20	SD_D2	SD2_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
P9/18	SD_D3	SD2_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	
P16/32	MMC_CLK	SD3_CLK	O	Clock for MMC/SD/SDIO card	
P18/36	MMC_CMD	SD3_CMD	I/O	CMD line connect to card	
P13/26	MMC_D0	SD3_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
P12/24	MMC_D1	SD3_DATA1	I/O	DATA1 line in 4/8-bit mode Also used to detect interrupt in 1/4-bit mode	
P10/20	MMC_D2	SD3_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
P20/40	MMC_D3	SD3_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	
P19/38	MMC_D4	SD3_DATA4	I/O	DATA4 line in 8-bit mode, not used in other modes	
P17/34	MMC_D5	SD3_DATA5	I/O	DATA5 line in 8-bit mode, not used in other modes	
P15/30	MMC_D6	SD3_DATA6	I/O	DATA6 line in 8-bit mode, not used in other modes	
P14/28	MMC_D7	SD3_DATA7	I/O	DATA7 line in 8-bit mode, not used in other modes	

The table below lists of alternative pin locations for uSDHC1 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P122/252	SPI-B_CLK	SD1_CLK	O	Clock for MMC/SD/SDIO card	Alternative function SD1_CLK.
P120/248	SPI-B_MOSI	SD1_CMD	I/O	CMD line connect to card	Alternative function SD1_CMD
P121/250	SPI-B_MISO	SD1_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	Alternative function SD1_DATA0
P119/246	SPI-B_SSEL	SD1_DATA1	I/O	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	Alternative function SD1_DATA1
S56/111	BL_PWM	SD1_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	Alternative function SD1_DATA2
P138/284	PWM	SD1_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	Alternative function SD1_DATA3
P103/214	COM specific	NANDF_D0	I/O	DATA4 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA4
P102/212	COM specific	NANDF_D1	I/O	DATA5 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA5
P101/210	COM specific	NANDF_D2	I/O	DATA6 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA6
P100/208	COM specific	NANDF_D3	I/O	DATA7 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA7
P139/286	GPIO2	GPIO_1	I	Card detection pin	Alternative function SD1_CD_B.
P94/196	COM specific	KEY_COL1	O	IO power voltage selection signal	Alternative function SD1_VSELECT
S50/99	I2C-C_SDA	KEY_ROW3	O	IO power voltage selection signal	Alternative function SD1_VSELECT

					Note that the pin is pre-allocated as I2C2_SCL and has on-board 2.2Kohm pull-up resistor. It is possible to use this pin but not recommended.
S10/19	SPDIF_IN	GPIO_16	O	LED control used to drive an external LED Active high	Alternative function SD1_LCTL
S84/173	GPIO7	DI0_PIN4	I	Card write protect detect	Alternative function SD1_WP

The table below lists of alternative pin locations for uSDHC2 signals as well as data signals 4-7 (for full 8-bit MMC interface).

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P140/288	GPIO1	GPIO_4	I	Card detection pin	Alternative function SD2_CD_B
P99/206	COM specific	NANDF_D4	I/O	DATA4 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA4
P98/204	COM specific	NANDF_D5	I/O	DATA5 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA5
P97/202	COM specific	NANDF_D6	I/O	DATA6 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA6
P96/200	COM specific	NANDF_D7	I/O	DATA7 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA7
S48/95	I2C-B_SDA	GPIO_6	O	LED control used to drive an external LED Active high	Alternative function SD2_LCTL
P92/192	COM specific	KEY_ROW1	O	IO power voltage selection signal	Alternative function SD2_VSELECT
S15/29	CAN1_RX	KEY_ROW2	O	IO power voltage selection signal	Alternative function SD2_VSELECT

The table below list the pin location for an additional uSDHC3 signal.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P4/8	GPIO3	SD3_RST	O	Card hardware reset signal, both active LOW and HIGH version of the signal exist	Alternative function SD3_RESET

There are no accessible pins for uSDHC4 signals since these are connected to the on-board eMMC Flash.

5.17 ECSPI / SPI

This section lists signals related to Enhanced Configurable Serial Peripheral Interface (ECSPI) functions.

The i.MX 6 SoC has 5 ECSPI block that are capable of full-duplex, synchronous, four-wire serial communication. The *EACOM Board specification* defines two 4-signal ECSPI interfaces. The remaining ECSPI signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P125/258	SPI-A_MISO	EIM_OE	I/O	Master data in, slave data out	ECSPI2_MISO
P124/256	SPI-A_MOSI	EIM_CS1	I/O	Master data out, slave data in	ECSPI2_MOSI
P126/260	SPI-A_SCLK	EIM_CS0	I/O	SPI clock signal	ECSPI2_SCLK
P123/254	SPI-A_SS0	EIM_RW	I/O	Chip select signal	ECSPI2_SS0
P121/250	SPI-B_MISO	SD1_DATA0	I/O	Master data in, slave data out	ECSPI5_MISO
P120/248	SPI-B_MOSI	SD1_CMD	I/O	Master data out, slave data in	ECSPI5_MOSI
P122/252	SPI-B_SCLK	SD1_CLK	I/O	SPI clock signal	ECSPI5_SCLK
P119/246	SPI-B_SS0	SD1_DATA1	I/O	Chip select signal	ECSPI5_SS0

The table below lists of alternative pin locations for ECSPI1 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S4/7	AUDIO_TXFS	CSI0_DATA6	I/O	Master data in, slave data out	ECSPI1_MISO
S64/127	LCD_R6	DISP0_DATA22	I/O	Master data in, slave data out	ECSPI1_MISO
P83/174	USB_H1_SSRXN	EIM_D17	I/O	Master data in, slave data out	ECSPI1_MISO
P94/196	COM specific	KEY_COL1	I/O	Master data in, slave data out	ECSPI1_MISO
S7/13	AUDIO_TXD	CSI0_DATA5	I/O	Master data out, slave data in	ECSPI1_MOSI
S63/125	LCD_R5	DISP0_DATA21	I/O	Master data out, slave data in	ECSPI1_MOSI
P81/170	USB_H1_SSTXP	EIM_D18	I/O	Master data out, slave data in	ECSPI1_MOSI
P93/194	COM specific	KEY_ROW0	I/O	Master data out, slave data in	ECSPI1_MOSI
S8/15	AUDIO_MCLK	GPIO_19	I/O	SPI data ready signal	ECSPI1_RDY
S6/11	AUDIO_TXC	CSI0_DATA4	I/O	SPI clock signal	ECSPI1_SCLK
S62/123	LCD_R4	DISP0_DATA20	I/O	SPI clock signal	ECSPI1_SCLK
P84/176	USB_H1_SSRXP	EIM_D16	I/O	SPI clock signal	ECSPI1_SCLK
P95/198	COM specific	KEY_COL0	I/O	SPI clock signal	ECSPI1_SCLK
S5/9	AUDIO_RXD	CSI0_DATA7	I/O	Chip select signal	ECSPI1_SS0
S65/129	LCD_R7	DISP0_DATA23	I/O	Chip select signal	ECSPI1_SS0
P80/168	USB_H1_SSTXN	EIM_EB2	I/O	Chip select signal	ECSPI1_SS0
P92/192	COM specific	KEY_ROW1	I/O	Chip select signal	ECSPI1_SS0
S73/145	LCD_G7	DISP0_DATA15	I/O	Chip select signal	ECSPI1_SS1
P117/242	COM specific	EIM_D19	I/O	Chip select signal	ECSPI1_SS1
S14/27	CAN1_TX	KEY_COL2	I/O	Chip select signal	ECSPI1_SS1
P112/232	COM specific	EIM_D24	I/O	Chip select signal	ECSPI1_SS2
S15/29	CAN1_RX	KEY_ROW2	I/O	Chip select signal	ECSPI1_SS2
P111/230	COM specific	EIM_D25	I/O	Chip select signal	ECSPI1_SS3
S51/101	I2C-C_SCL	KEY_COL3	I/O	Chip select signal	ECSPI1_SS3 Note that the pin is pre-allocated as I2C2_SCL and has on-board 2.2Kohm pull-up resistor. It is possible to use this pin but not recommended.

The table below lists of alternative pin locations for ECSPI2 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P129/266	UART-C_TXD	CSI0_DATA10	I/O	Master data in, slave data out	ECSPI2_MISO
S59/117	LCD_R1	DISP0_DATA17	I/O	Master data in, slave data out	ECSPI2_MISO
S58/115	LCD_R0	DISP0_DATA16	I/O	Master data out, slave data in	ECSPI2_MOSI
S34/67	GPIO8	EIM_A25	I/O	SPI data ready signal	ECSPI2_RDY
S61/121	LCD_R3	DISP0_DATA19	I/O	SPI clock signal	ECSPI2_SCLK
P128/264	UART-C_RXD	CSI0_DATA11	I/O	Chip select signal	ECSPI2_SS0
S60/119	LCD_R2	DISP0_DATA18	I/O	Chip select signal	ECSPI2_SS0
S73/145	LCD_G7	DISP0_DATA15	I/O	Chip select signal	ECSPI2_SS1
P115/238	COM specific	EIM_LBA	I/O	Chip select signal	ECSPI2_SS1
P112/232	COM specific	EIM_D24	I/O	Chip select signal	ECSPI2_SS2
P111/230	COM specific	EIM_D25	I/O	Chip select signal	ECSPI2_SS3

The table below lists of alternative pin locations for ECSPI3 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
S77/159	LCD_B2	DISP0_DATA2	I/O	Master data in, slave data out	ECSPI3_MISO
S76/157	LCD_B1	DISP0_DATA1	I/O	Master data out, slave data in	ECSPI3_MOSI
S82/169	LCD_B7	DISP0_DATA7	I/O	SPI data ready signal	ECSPI3_RDY
S75/149	LCD_B0	DISP0_DATA0	I/O	SPI clock signal	ECSPI3_SCLK
S78/161	LCD_B0	DISP0_DATA3	I/O	Chip select signal	ECSPI3_SS0
S79/163	LCD_B4	DISP0_DATA4	I/O	Chip select signal	ECSPI3_SS1
S80/165	LCD_B5	DISP0_DATA5	I/O	Chip select signal	ECSPI3_SS2
S81/167	LCD_B6	DISP0_DATA6	I/O	Chip select signal	ECSPI3_SS3

The table below lists of alternative pin locations for ECSPI4 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P73/146	USB_O1_PWR_EN	EIM_D22	I/O	Master data in, slave data out	ECSPI4_MISO
P108/224	COM specific	EIM_D28	I/O	Master data out, slave data in	ECSPI4_MOSI
P114/236	COM specific	EIM_EB3	I/O	SPI data ready signal	ECSPI4_RDY
P74/148	USB_O1_OC	EIM_D21	I/O	SPI clock signal	ECSPI4_SCLK
P116/240	COM specific	EIM_D20	I/O	Chip select signal	ECSPI4_SS0
P107/222	COM specific	EIM_D29	I/O	Chip select signal	ECSPI4_SS0
S34/67	GPIO8	EIM_A25	I/O	Chip select signal	ECSPI4_SS1
P112/232	COM specific	EIM_D24	I/O	Chip select signal	ECSPI4_SS2
P111/230	COM specific	EIM_D25	I/O	Chip select signal	ECSPI4_SS3

The table below lists of alternative pin locations for ECSPI5 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P6/12	SD_D0	SD2_DATA0	I/O	Master data in, slave data out	ECSPI5_MISO
P8/16	SD_CMD	SD2_CMD	I/O	Master data out, slave data in	ECSPI5_MOSI
S2/3	MQS_LEFT	GPIO_7	I/O	SPI data ready signal	ECSPI5_RDY
P7/14	SD_CLK	SD2_CLK	I/O	SPI clock signal	ECSPI5_SCLK
P5/10	SD_D1	SD2_DATA1	I/O	Chip select signal	ECSPI5_SS0
S56/111	BL_PWM	SD1_DATA2	I/O	Chip select signal	ECSPI5_SS1
P10/20	SD_D2	SD2_DATA2	I/O	Chip select signal	ECSPI5_SS1
P138/284	PWM	SD1_DATA3	I/O	Chip select signal	ECSPI5_SS2
P9/18	SD_D3	SD2_DATA3	I/O	Chip select signal	ECSPI5_SS3

5.18 UART

This section lists signals related to Universal Asynchronous Receiver/Transmitter (UART) functions.

The i.MX 6 SoC has fivex UARTs, supporting bitrates up to 5Mbps each. The *EACOM Board specification* defines two 4-signal UARTs and one 2-signal UART. The remaining UART signals are available as alternative functions on certain pins.

Note that the chip-level IOMUX modifies the direction and routing of the UART signals based on whether the UART is operating in DCE mode or DTE mode. See section 64.2 in IMX6DQRM for details.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P137/282	UART-A_TXD	CSI0_DATA12	I/O	UART4 Transmit Data	
P134/276	UART-A_RXD	CSI0_DATA13	I/O	UART4 Receive Data	
P136/280	UART-A_RTS	CSI0_DATA16	I/O	UART4 Request to Send	
P135/278	UART-A_CTS	CSI0_DATA17	I/O	UART4 Clear to Send	
P133/274	UART-B_TXD	CSI0_DATA14	I/O	UART5 Transmit Data	
P130/268	UART-B_RXD	CSI0_DATA15	I/O	UART5 Receive Data	
P132/272	UART-B_RTS	CSI0_DATA18	I/O	UART5 Request to Send	
P131/270	UART-B_CTS	CSI0_DATA19	I/O	UART5 Clear to Send	
P129/266	UART-C_TXD	CSI0_DATA10	I/O	UART1 Transmit Data	
P128/264	UART-C_RXD	CSI0_DATA11	I/O	UART1 Receive Data	

The table below lists of alternative pin locations for UART1 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P14/28	MMC_D7	SD3_DATA7	I/O	UART1 Transmit Data	Alternative function is UART1_TXD
P15/30	MMC_D6	SD3_DATA6	I/O	UART1 Receive Data	Alternative function is UART1_RXD
P12/24	MMC_D1	SD3_DATA1	I/O	UART1 Request to Send	Alternative function is UART1_RTS_B
P116/240	COM specific	EIM_D20	I/O	UART1 Request to Send	Alternative function is UART1_RTS_B
P13/26	MMC_D0	SD3_DATA0	I/O	UART1 Clear to Send	Alternative function is UART1_CTS_B
P117/242	COM specific	EIM_D19	I/O	UART1 Clear to Send	Alternative function is UART1_CTS_B
P113/234	COM specific	EIM_D23	I/O	UART1 DCD	Alternative function is UART1_DCD_B
P111/230	COM specific	EIM_D25	I/O	UART1 DSR	Alternative function is UART1_DSR_B
P112/232	COM specific	EIM_D24	I/O	UART1 DTR	Alternative function is UART1_DTR_B
P114/236	COM specific	EIM_EB3	I/O	UART1 RI	Alternative function is UART1_RI_B

The table below lists of alternative pin locations for UART2 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P110/228	COM specific	EIM_D26	I/O	UART2 Transmit Data	Alternative function is UART2_TXD.
S2/3	MQS_LEFT	GPIO_7	I/O	UART2 Transmit Data	Alternative function is UART2_TXD.
P17/34	MMC_D5	SD3_DATA5	I/O	UART2 Transmit Data	Alternative function is UART2_TXD.
P109/226	COM specific	EIM_D27	I/O	UART2 Receive Data	Alternative function is UART2_RXD.
S1/1	MQS_RIGHT	GPIO_8	I/O	UART2 Receive Data	Alternative function is UART2_RXD.
P19/38	MMC_D4	SD3_DATA4	I/O	UART2 Receive Data	Alternative function is UART2_RXD.
P107/222	COM specific	EIM_D29	I/O	UART2 Request to Send	Alternative function is UART2_RTS_B.
P16/32	MMC_CLK	SD3_CLK	I/O	UART2 Request to Send	Alternative function is UART2_RTS_B.
P108/224	COM specific	EIM_D28	I/O	UART2 Clear to Send	Alternative function is UART2_CTS_B.
P18/36	MMC_CMD	SD3_CMD	I/O	UART2 Clear to Send	Alternative function is UART2_CTS_B.

The table below lists of alternative pin locations for UART3 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P112/232	COM specific	EIM_D24	I/O	UART3 Transmit Data	Alternative function is UART3_TXD.
P111/230	COM specific	EIM_D25	I/O	UART3 Receive Data	Alternative function is UART3_RXD.
P105/218	COM specific	EIM_D31	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
P114/236	COM specific	EIM_EB3	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
P4/8	GPIO3	SD3_RST	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
P113/234	COM specific	EIM_D23	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.
P106/220	COM specific	EIM_D30	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.
P20/40	MMC_D3	SD3_DATA3	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.

The table below lists of alternative pin locations for UART4 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P95/198	COM specific	KEY_COL0	I/O	UART4 Transmit Data	Alternative function is UART4_TXD.
P93/194	COM specific	KEY_ROW0	I/O	UART4 Receive Data	Alternative function is UART4_RXD.

The table below lists of alternative pin locations for UART5 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P94/196	COM specific	KEY_COL1	I/O	UART5 Transmit Data	Alternative function is UART5_TXD.
P92/192	COM specific	KEY_ROW1	I/O	UART5 Receive Data	Alternative function is UART5_RXD.
S12/23	CAN2_TX	KEY_COL4	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B.
S13/25	CAN2_RX	KEY_ROW4	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B.

5.19 USB

This section lists signals related to the USB interfaces.

The *EACOM Board Specification* has one USB 3.0 OTG port, one USB 3.0 Host port and one USB 2.0 Host port. The i.MX 6 has one USB 2.0 OTG port and one USB 2.0 Host port. Further, USB 3.0 is backward compatible with USB 2.0. The pins that are specific for USB 3.0 are just left unconnected and are for future upgrade.

The carrier board must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P64/128	USB_O1_DN	USB_OTG_DN	I/O	Negative Differential USB Signal, OTG compatible	
P65/130	USB_O1_DP	USB_OTG_DP	I/O	Positive Differential USB Signal, OTG compatible	
P66/132	USB_O1_ID	ENET_RX_ER	I	USB OTG ID pin	
P67/134	USB_O1_SSTXN			Not connected	
P68/136	USB_O1_SSTXP			Not connected	
P70/140	USB_O1_SSRXN			Not connected	
P71/142	USB_O1_SSRXP			Not connected	
P72/144	USB_O1_VBUS	USB_OTG_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.
P73/146	USB_O1_PWR_EN	EIM_DATA22	O	Enable external USB voltage supply. Active high output.	
P74/148	USB_O1_OC	EIM_DATA21	I	Signals an over-current condition on the USB voltage supply. Active low input.	
P75/158	USB_H1_PWR_EN	GPIO_0	O	Enable external USB voltage supply. Active high output.	
P76/160	USB_H1_OC	GPIO_3	I	Signals an over-current condition on the USB voltage supply. Active low input.	
P78/164	USB_H1_DN	USB_H1_DN	I/O	Negative Differential USB Signal	
P79/166	USB_H1_DP	USB_H1_DP	I/O	Positive Differential USB Signal	
P80/168	USB_H1_SSTXN	EIM_EB2	I/O	Not standard pin allocation.	Not connected for USB functionality

P81/170	USB_H1_SSTXP	EIM_DATA18	I/O	Not standard pin allocation.	Not connected for USB functionality
P83/174	USB_H1_SSRXN	EIM_DATA17	I/O	Not standard pin allocation.	Not connected for USB functionality
P84/176	USB_H1_SSRXP	EIM_DATA16	I/O	Not standard pin allocation.	Not connected for USB functionality
P85/178	USB_H1_VBUS	USB_H1_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.

The table below lists of alternative pin locations for USB signals.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P139/286	GPIO2	GPIO_1	I	USB OTG ID	
S12/23	CAN2_TX	KEY_COL4	I	USB OTG OC	Signals an over-current condition on the USB voltage supply. Active low input.
S13/25	CAN2_RX	KEY_ROW4	O	USB OTG PWR EN	Enable external USB voltage supply. Active high output.
P106/220	COM specific	EIM_D30	I	USB H1 OC	Signals an over-current condition on the USB voltage supply. Active low input.
P105/218	COM specific	EIM_D31	O	USB H1 PWR EN	Enable external USB voltage supply. Active high output.

Note that EACOM USB Host port #2 is not connected to a USB port on the i.MX 6. Some other signals are connected to these pins in a non-standard way, see table below.

EACOM Board Pin	EACOM Board Name	i.MX 6 Ball Name	I/O	Description	Remarks
P86/180	USB_H2_PWR_EN	SNVS_TAMPER signal, i.MX 6 ball E11		Not connected for USB functionality	
P87/182	USB_H2_OC	ONOFF signal, i.MX 6 ball D12		Not connected for USB functionality	
P89/186	USB_H2_DN	CSI0_YSYNC		Not connected for USB functionality	
P90/188	USB_H2_DP	CSI0_DATA_EN		Not connected for USB functionality	

6 Boot Options

This chapter presents the different boot settings that the *iMX6 COM Board* supports. This chapter will only present how the different options are controlled. Other documents discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The *iMX6 COM Board* supports booting (i.e., from where the i.MX 6 SoC starts downloading code to start executing from) from different sources:

- On-board eMMC Flash (signal E2PROM_WP high/floating - default)
- USB OTG download (also called 'serial download'), (signal E2PROM_WP low)
- Other sources, like SATA, external SD/MMC memory cards, etc.
  Note that the OTP fuses must be programmed to set these sources, see below.

Signal E2PROM_WP controls the booting source. If signal E2PROM_WP is high/floating, which is the default, booting takes place from eMMC. If Signal EPROM_WP is low, the i.MX 6 SoC boots into USB OTG mode. This latter mode it typically only used during production when the program images shall be downloaded the first time.

There are three main boot **modes** that controls which boot **source** to use.

- Boot according to on-board configuration pull-up/pull-down resistors
  - eMMC is set as default boot source.
  - **Note that signals EIM_DA0-DA15, EIM_A24, EIM_WAIT, EIM_LBA, EIM_RW, EIM_EB0-EB3 must not be driven externally**. The reason why the pins must not be driven externally is that on-board resistors pull these signals high/low to select eMMC booting. Driving any of these signals can change this default behavior.
    If any of the signals are driven externally the on-chip OTP fuses must be programmed to force eMMC booting instead.
- Boot according to how internal (i.MX 6 on-chip) OTP fuses have been programmed
  - Any boot mode supported by the i.MX 6 SoC and the hardware connected to it can be selected. See *i.MX 6Dual/6Quad Applications Processor Reference Manual* for details about available sources and OTP fuse settings.
  - Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to override the default setting to boot from eMMC and to have OTP fuse settings controlling boot source instead.
  - Note that the ***iMX6 COM Boards* have not programmed the on-chip OTP fuses**. Users have full control over these. This mode can only be used after having programmed the OTP fuses.
  - Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery.
- Boot from USB OTG interface
  - This mode is used in production to download the first stage bootloader and is typically not used by *iMX6 COM Board* integrators. Sometimes this mode is called "Recovery mode".
  - This mode is activated by pulling signal E2PROM_WP low.

To summarize, the *iMX6 COM board* is setup to boot from eMMC as default. If another source is needed, program the OTP fuses.

If using the default setup (boot from eMMC), make sure the boot control pins (EIM_DA0-DA15, EIM_A24, EIM_WAIT, EIM_LBA, EIM_RW, EIM_EB0-EB3) are not driven externally.

An optional USB OTG boot mode can be enables by pulling signal E2PROM_WP low.

7 Technical Specification

7.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.3	3.6	V
VBAT	Coin cell voltage	-0.3	3.6	V
VIO	Vin/Vout (I/O VDD + 0.3)	-0.5	3.6	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

7.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage Ripple with frequency content < 10 MHz Ripple with frequency content ≥ 10 MHz	3.2	3.3	3.4 50 10	V mV mV
VBAT	Coin cell voltage **Note:** This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC). **Note:** if the backup battery is rechargeable, the board provides a backup battery charger function.	2.8	3.3	3.6	V
USB_xx_VBUS	USB VBUS signals	4.4	5	5.25	V

7.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

7.4 Electrical Characteristics

For DC electrical characteristics, see *i.MX 6Dual/6Quad Applications Processor Datasheet*. Depending on internal VDD operating point, OVDD is 3.25V (50 mV under typical recommended VIN, 3.3V).

7.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN.

7.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 20 uS minimum. The internal reset pulse will be 140-280 mS long, before the i.MX 6 boot process starts.

7.5 Power Consumption

There are several factors that determine power consumption of the *iMX6 COM Board*, like input voltage, operating temperature, DDR3L activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

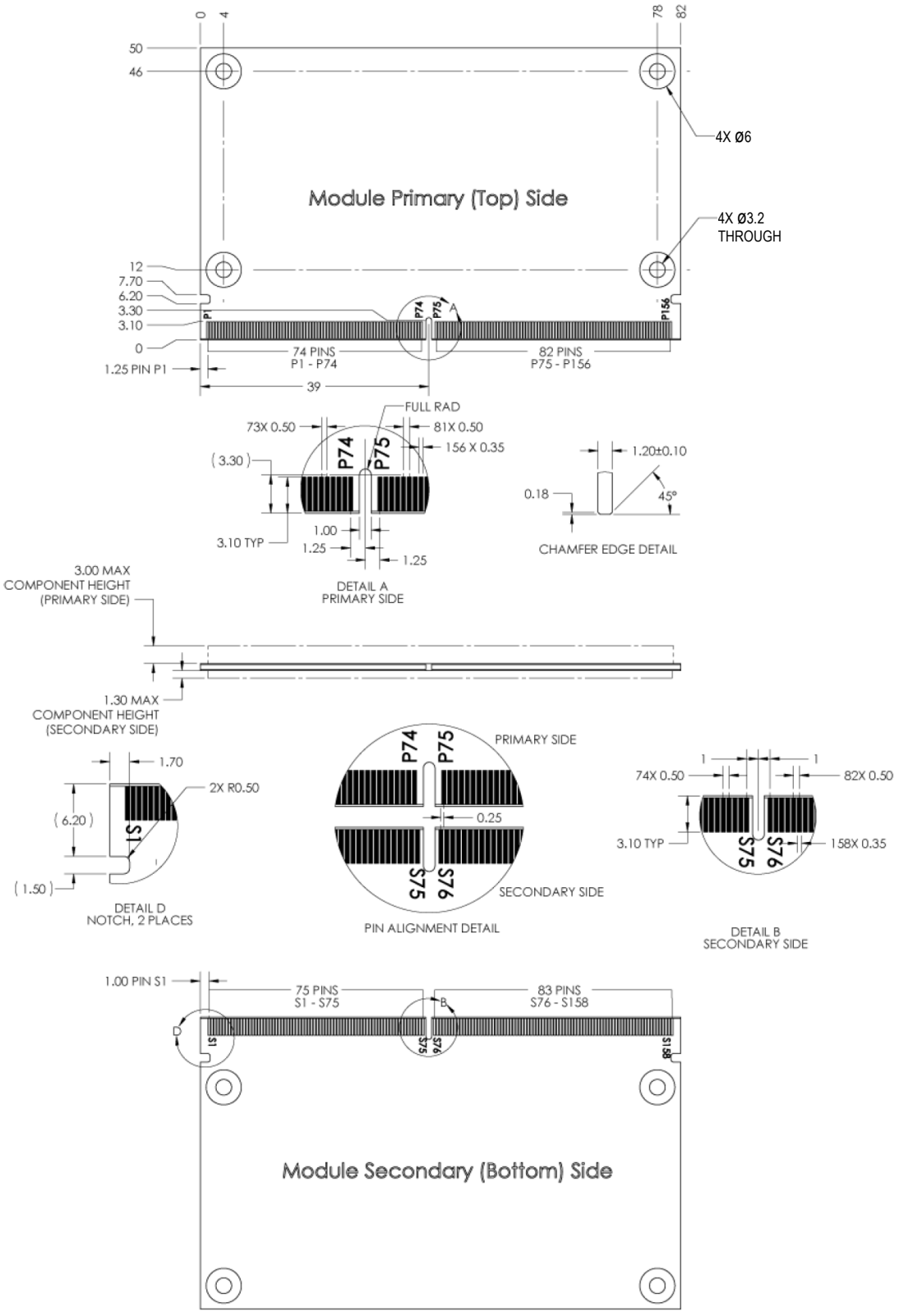
Symbol	Description (VIN = 3.3V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_**DSM**	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD	TBD	mA
I_{VIN}_**IDLE**	CPU idle	TBD	TBD	mA
I_{VIN}_**xxx**	Maximum CPU load, 996MHz ARM frequency	TBD	TBD	mA
I_{VIN}_**xxx**	Suspend state	TBD	TBD	mA
I_{VIN}_**xxx**	Dhrystone benchmark on Cortex-A9 (996 MHz)	TBD	TBD	mA
I_{VBAT}_**BACKUP**	Current consumption to keep internal RTC running	TBD	TBD	uA

7.6 Mechanical Dimensions

The board use the SMARC mechanical form factor.

Dimension	Value (±0.1 mm)	Unit
Module width	82	mm
Module height	50	mm
Module top side height	3.0	mm
Module bottom side height	1.3	mm
PCB thickness	1.2	mm
Mounting hole diameter **Note:** This measurement is not identical with SMARC specification.	3.2	mm
Module weight	16 ±1 gram	gram

The picture below show the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification and show pin numbering in the Px and Sx format.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 8 – iMX6 COM Board Mechanical Outline

7.6.1 MXM3 Socket

The board has 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE should not be used since this specific connector lack some of the pins. It is however possible to use the connector if it is acceptable for the project to not use the following pins:

- P146/300 E2PROM_WP This pin is also used to select USB OTG as boot mode (when pulled low), also known as "factory recovery" mode. Not having access to this pin means that USB OTG mode cannot be enabled from the carrier board.
- P147/302 VIN This is not any problem since there are many VIN pins.
- S149/303 GND This is not any problem since there are many GND pins.
- S148/301 GND This is not any problem since there are many GND pins.

Embedded Artists use connector AS0B826-S78B from Foxconn on the COM Carrier board. This connector gives a board to board stacking height of 5.0 mm. This space allows some components to also be placed right under the COM board.

Always check available component height before placing components on the carrier board under the COM board, see picture below.

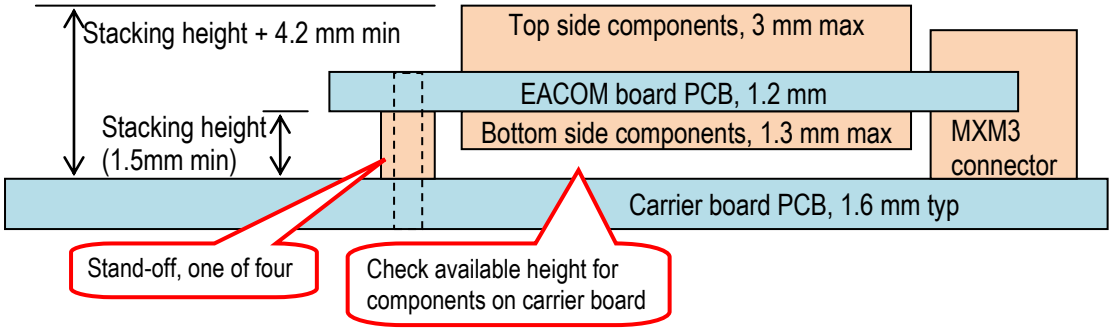


Figure 9 – COM Board Mounting in MXM3 Connector, Stacking Height

7.6.2 Module Assembly Hardware

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". 5 mm height is standard so for simplicity select an MXM3 connector with 5 mm stacking height.

6-8 mm M3 screws are typically used.

7.7 Environmental Specification

7.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range industrial temperature range	0 -40	70[1] 85[1]	°C °C
Storage temperature range		-40	85	°C
Junction temperature i.MX 6 SoC, operating:	comm. temp. range ind. temp. range.	0 -40	105 105	°C °C

[1] Depends on cooling solution.

7.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 60°C, non-condensing	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing	5	90	%

7.8 Thermal Design Considerations

Heat dissipation from the i.MX 6 SoC depending on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat is in the region of 2 Watt max. DDR3L memories can account for another 0.5 Watt, also increasing ambient temperature.

If external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In many cases it is possible to operate the *iMX6 COM board* without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 6 SoC.

The i.MX 6 SoC and PMIC (MMPF0100) together implement DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general this result in higher performance at lower average power consumption.

The i.MX 6 SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affect several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: AN4724, i.MX 6Dual/6Quad/6DualPlus/6QuadPlus Product Usage Lifetime Estimates.
- A lower die temperature will result in lower power consumption due to lower leakage current.

7.8.1 Thermal Management

Embedded Artists provides a general heat spreader solution for EACOM boards. Note that a heat spreader is not a complete thermal solution. It provides a standardized surface for mounting a heat sink or for transporting heat to the housing.

The cooling solution must maintain an ambient air and heat spreader temperature of 60° Celsius, or less.

7.8.2 Thermal Parameters

The i.MX 6 SoC thermal parameters are listed in the table below.

Parameter	Temp. Range	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$)	Comm. Ind.	22 15	°C/W °C/W
Thermal Resistance, CPU Junction to case, top ($R_{\theta JCtop}$)	Comm. Ind.	0.1 1	°C/W °C/W

7.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2, Conflict Minerals, REACH, etc.

8 Functional Verification and RMA

There is a separate document that presents a number of functional tests that can be performed on the *iMX6 COM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX6 Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

9 Things to Note

This chapter presents a number of issues and considerations that users must note.

9.1 Shared Pins and Multiplexing

The i.MX 6 SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the iMX6 COM board design. Check if the needed interfaces are available to allocation before starting a design. See section 3.2 and chapter 5 for details.

9.2 Only Use EA Board Support Package (BSP)

The *iMX6 COM board* use multiple on-board interfaces for the internal design, for example PMIC, eMMC, Ethernet and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX6 COM Boards because of improper interface initialization and/or improper pin assignment.

9.3 OTP Fuse Programming

The i.MX 6 SoC has on-chip OTP fuses that can be programmed, see NXP documents *i.MX 6Dual/6Quad Applications Processor Datasheet* and *i.MX 6Dual/6Quad Applications Processor Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX6 COM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and in that case, which ones.

Note that Embedded Artists does not replace iMX6 COM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

9.4 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory calibration settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write protected if signal E2PROM_WR (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal E2PROM_WR has dual functions. By pulling the signal low, the i.MX 6 SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

9.5 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards

- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX6 COM Board* targets a wide range of applications, such as:

- Industrial controllers and HMI systems
- Home automation and facility management
- Audiovisual equipment
- Instrumentation and measuring equipment
- Vending machines
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- HMI/GUI solutions
- Smart Toll Systems
- Connected vending machines
- Digital signage
- Point-of-Sale (POS) applications
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- Portable systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX6 COM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX6 COM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX6 COM Board*.

9.6 ESD Precaution when Handling iMX6 COM Board

Please note that the *iMX6 COM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch one of the four mounting holes (these are grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board, connecting the JTAG cable or when changing boot slider switches.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

9.7 EMC / ESD

The *iMX6 COM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless depending on the target system, additional anti-interference measurement may still be necessary to adherence to the limits for the overall system.

The *iMX6 COM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only makes sense on the complete solution.

No specific ESD protection has been implemented on the *iMX6 COM Board*, except on the JTAG interface signals, which all have suppressor diodes. ESD protection on board level is the same as what is specified in the i.MX 6 SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

10 Custom Design

This document specify the standard *iMX6 COM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Different application processor version mounted.
- Different memory sizes on DDR3L SDRAM and eMMC Flash.
- Different mounting options, for example mount SPI-flash and remove Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different I/O voltage levels on all or parts of the pins.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range, for example 5V input.
- Single Board Computer solutions, where the core design of the *iMX6 COM Board* is integrated together with selected interfaces.
- Replace eMMC Flash with (unmanaged) MLC/SLC NAND Flash.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

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