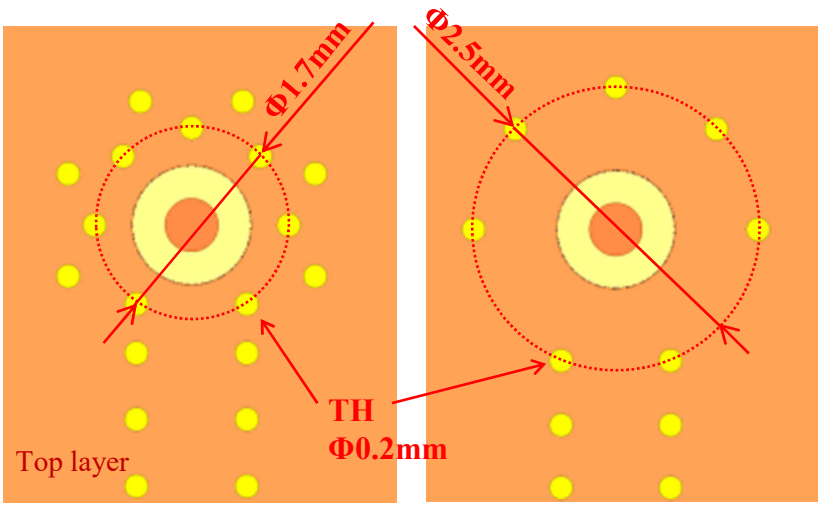
PCB Board Design

As the needs for high frequency measurement is increasing due to the high speed transmission inside equipment, the level of difficulty for designing is getting higher. When designing RF board, engineers should consider different factors including power dissipation, board size and noises etc.

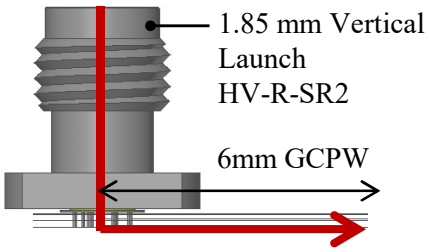
The following board guidance shows the points to keep in mind when using our Vertical Launch connector. Hirose highly recommends to optimize PCB pattern and the ground via position to match the specific connectors you will be using. In the case you need to optimize PCB with Hirose, please visit our website for more details at https://www.hirose.com/product/en/pr/mmwave/ *and contact us.*

Ground via optimization to avoid resonance

◆ Please design ground vias in the vicinity of the signal via, as shown in the example below, so that resonance will not occur below 65GHz.



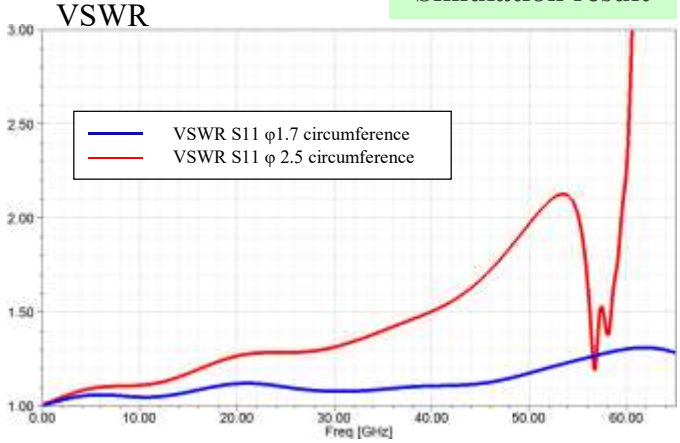
Φ1.7 mm circumference Φ2.5 mm circumference



MEGTRON6
R-5775K (Dk : 3.4, Df : 0.006)

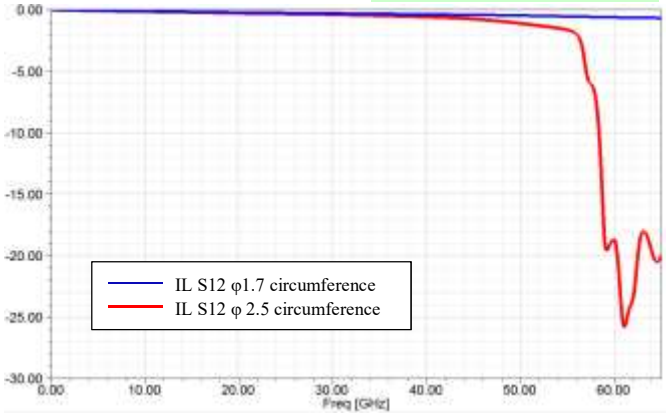
Simulation result

VSWR



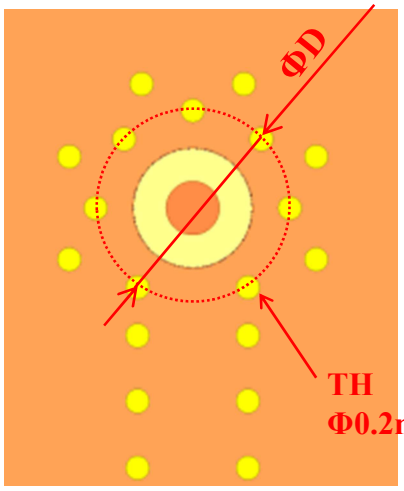
Simulation result

Insertion loss

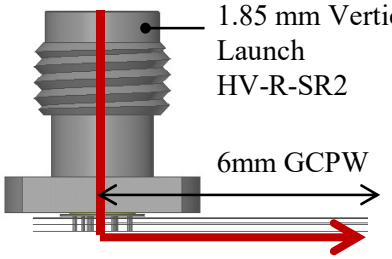


Ground Via Optimization to Match Impedance

◆ Please design ground vias in the vicinity of the signal via as shown in example below to optimize impedance matching.

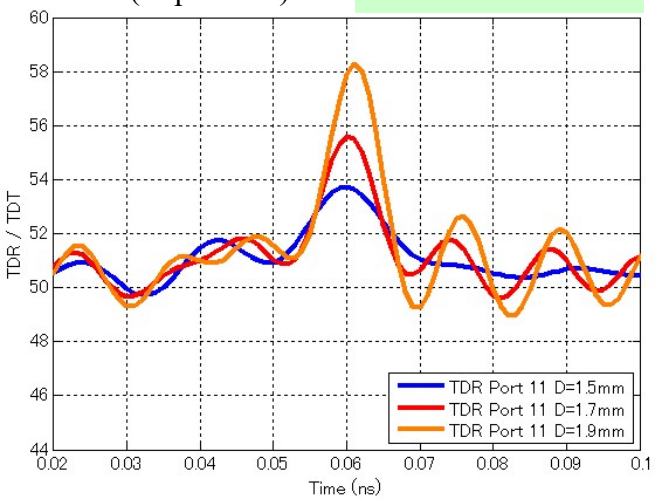


Top layer

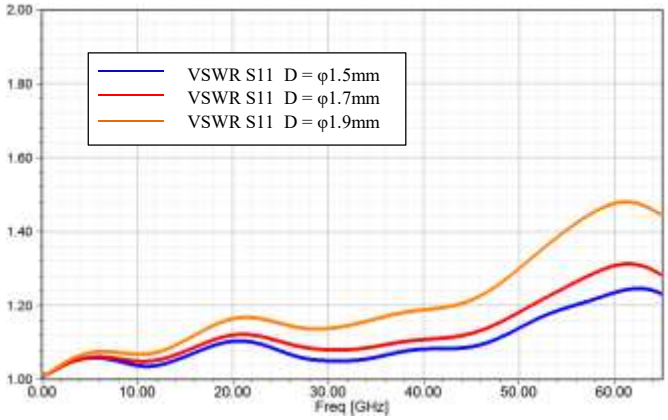


MEGTRON6 R-5775K (Dk : 3.4, Df : 0.006)

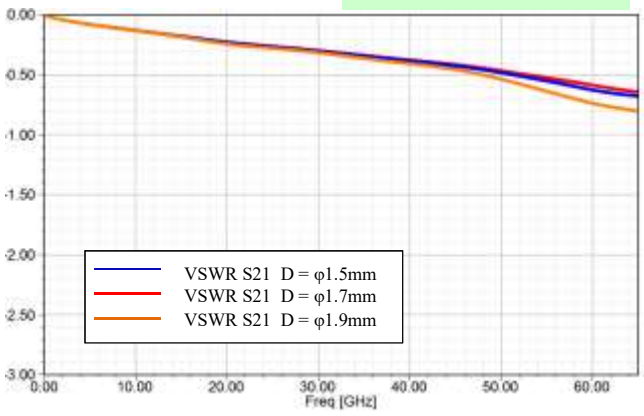
TDR(Impedance) **Simulation result**



VSWR **Simulation result**

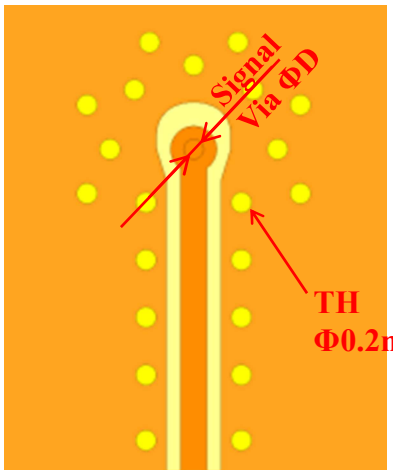


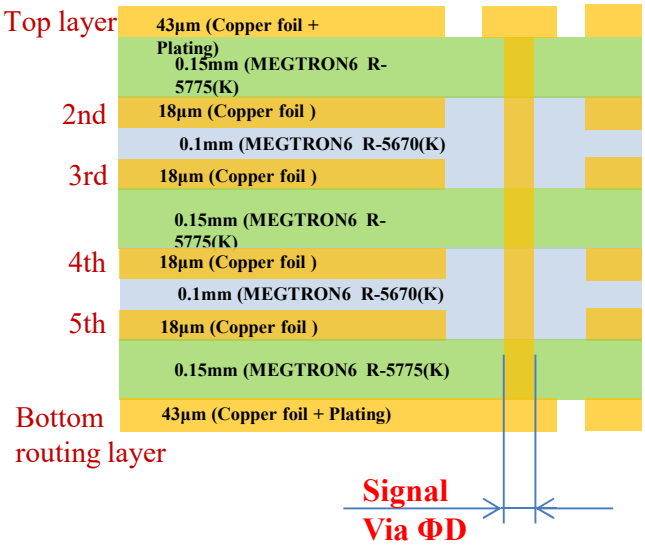
Insertion loss **Simulation result**

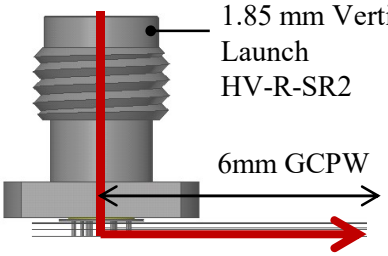


Signal Via Optimization

◆ Please design appropriate signal via to optimize impedance matching.



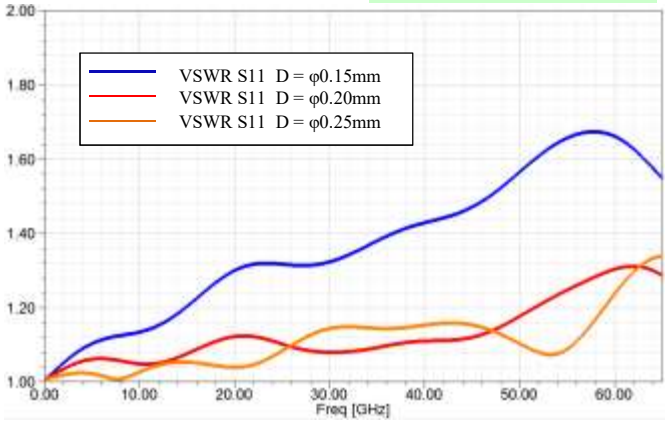




MEGTRON6 R-5775K (Dk : 3.4, Df : 0.006)

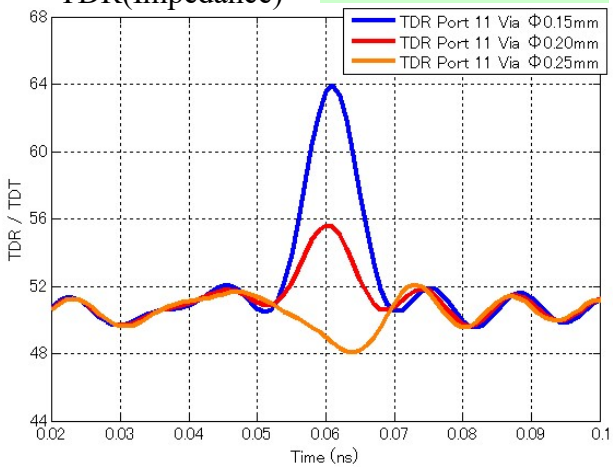
VSWR

Simulation result



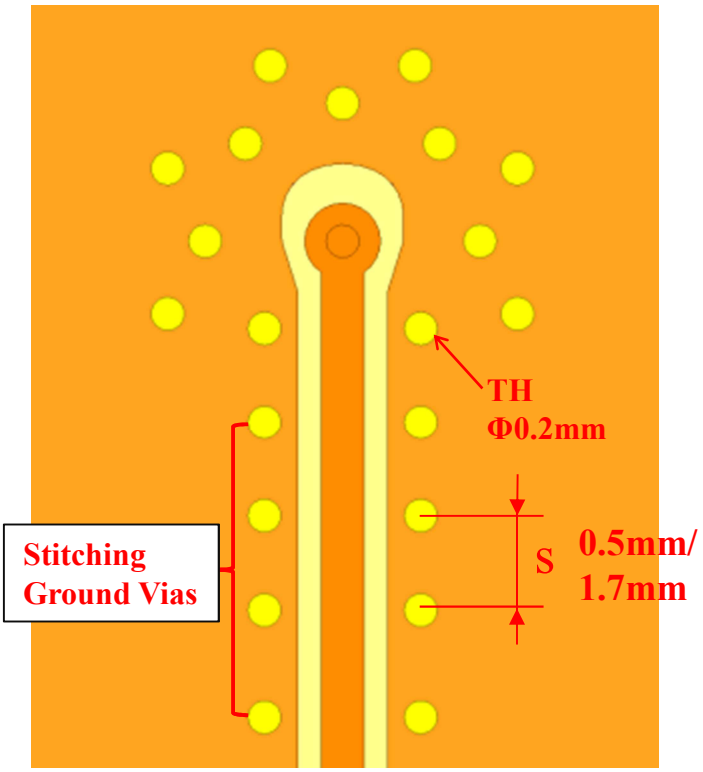
TDR(Impedance)

Simulation result



CPWG Recommended Via Pitch Stitching

◆ In order to prevent resonance in the structure of the coplanar line, we recommend a stitching via pitch of less than ¼ wavelength on both sides of the ground as shown below.



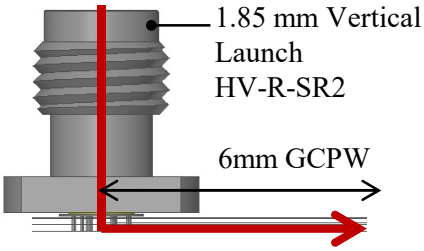
Bottom layer

$$s < \frac{\lambda_0}{4\sqrt{\varepsilon_{eff}}}$$

S : Via pitch interval

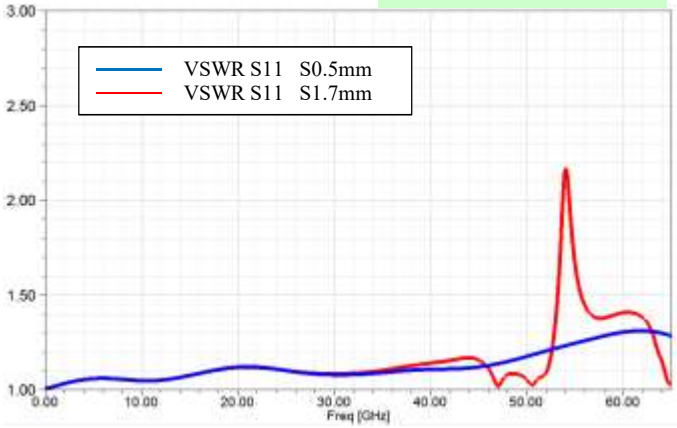
λo : Electric wavelength

ε_{eff} : Effective dielectric constant

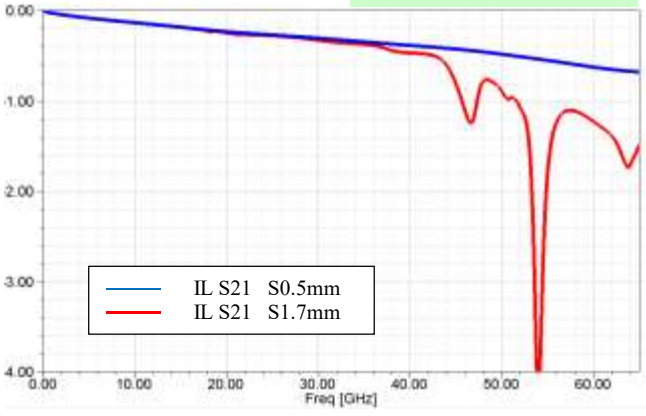


MEGTRON6 R-5775K (Dk : 3.4, Df : 0.006)

VSWR **Simulation result**

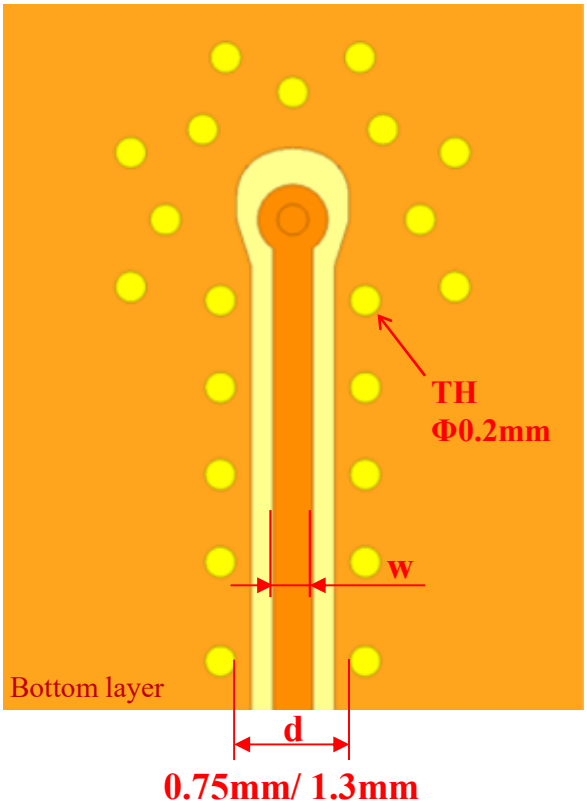


Insertion loss **Simulation result**



CPWG recommended Via to Signal Trace Spacing

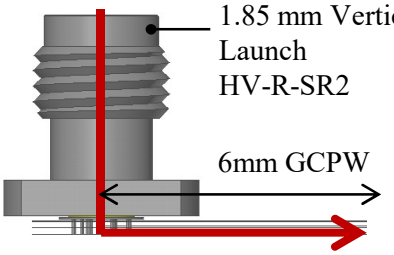
◆ For the interval of the stitching via on the side of the signal trace, width of either more than three times of the signal trace width or less than one-half wavelength is recommended. If vias are too close to signal trace, there is an opportunity that impedance will be affected. When the vias are too far from the signal trace, unintended propagation modes may occur and there is a risk of affecting the RF performance.



$$d < \frac{\lambda_0}{2\sqrt{\varepsilon_{eff}}}$$

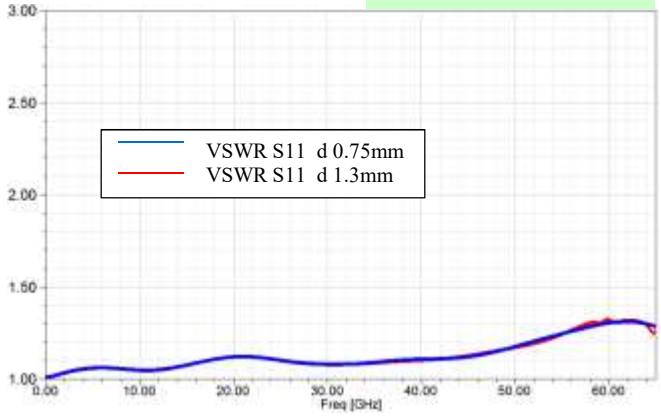
$$d > 3w$$

d Via interval
w Signal line width
λ_0 : Electric wavelength
ε_{eff} : Effective dielectric constant

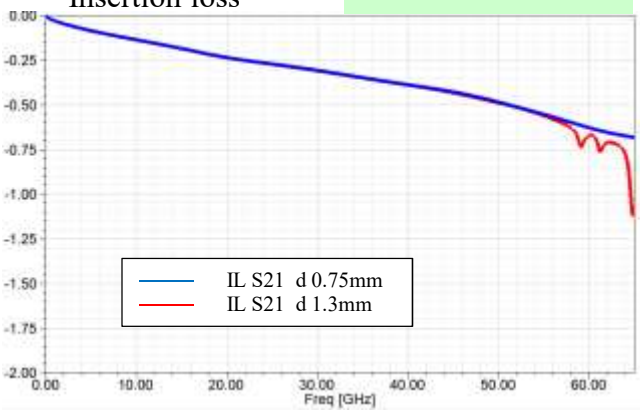


MEGTRON6 R-5775K (Dk : 3.4, Df : 0.006)

VSWR **Simulation result**



Insertion loss **Simulation result**

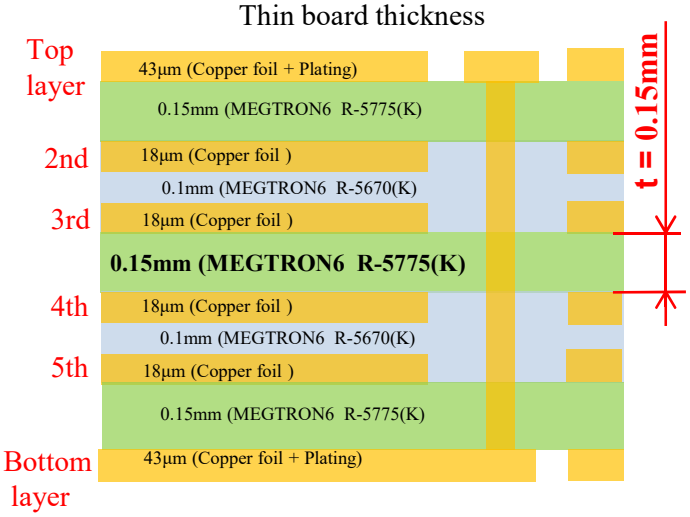


2 Board thickness between two grounds

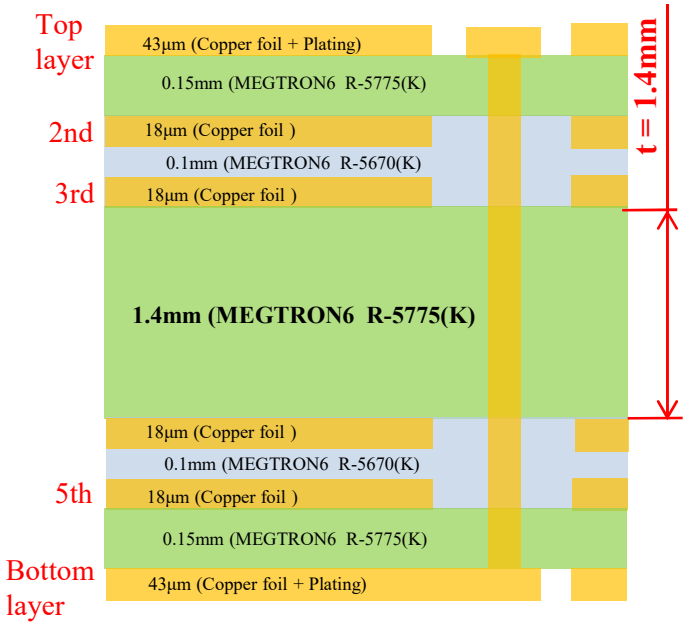
◆ If the board is too thick, extraneous reflection may occur and affect the signal transmission of the circuit. We recommend that the one layer thickness is less than a half wave length of the requested test frequency.

Board thickness between two grounds

Thin board thickness



Thick board thickness



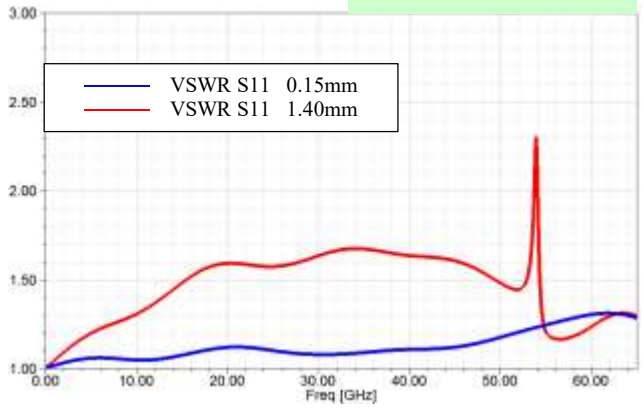
$$t < \frac{\lambda_0}{2\sqrt{\varepsilon_{eff}}}$$

t : Board thickness

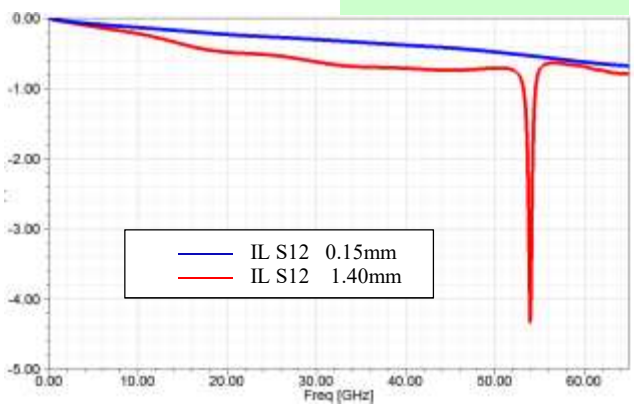
λ_0 : Electric wavelength

ε_{eff} : Effective dielectric constant

VSWR **Simulation result**



Insertion loss **Simulation result**



Others

The introduced design information herein are generally depends on the board permittivity, thickness and layer structure. The higher frequency used, the more difficult the design is. Depending on whether the connector and the mounting areas are optimized or not, there will be a significant difference in performance.

If you have any questions about designing high-frequency circuit board, please contact us.

https://www.hirose.com/

To optimize the performance of the board, we can provide electromagnetic field simulation models of connectors and various kinds of information.

https://www.hirose.com/product/en/pr/mmwave/board_test/